Novel Cascode NCLSCR/PCLSCR Design with Tunable Holding Voltage for Safe Whole-Chip ESD Protection

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Abstract

A novel design has been proposed to safely apply the NCLSCR (NMOS-controlled lateral SCR) and PCLSCR (PMOS-controlled lateral SCR) devices for whole-chip ESD (electrostatic discharge) protection in CMOS IC's without causing the unexpected operation errors or the VDD-to-VSS latchup issue. By using the cascode configuration, the ESD protection circuit with the cascode NCLSCR's or PCLSCR's has a tunable holding voltage greater than VDD of the IC's. Such cascode NCLSCR's (or PCLSCR's) can provide the CMOS IC's with effective ESD protection but without accidentally triggering on by the overshooting (undershooting) noise pulses in the system applications. This novel cascode NCLSCR's (PCLSCR's) design has been practically applied to protect the IC's in a 0.35-μm silicide CMOS technology with the HBM ESD robustness above 3KV.

Introduction

The LVTSCR (low-voltage triggering SCR) device had been well known as one of the most effective ESD-protection elements for input and output pins in CMOS IC's [1]-[3]. The trigger voltage (current) of LVTSCR in the submicron CMOS technology had been lowered to be about ~10V (~10mA) [1]-[2]. The typical I-V characteristics of an LVTSCR in a 0.6-μm CMOS technology is shown in Fig.1. Due to the low holding voltage, the LVTSCR can sustain high ESD voltage with only occupying a much smaller layout area in the CMOS IC's. To avoid the unexpected ESD damages on the internal circuits beyond the input or output ESD protection circuits [4]-[7], the effective ESD clamp circuit has to be placed between the VDD and VSS power lines of an IC to provide the real whole-chip ESD protection [8]-[10]. Thus, the area- efficient lateral SCR devices had been used in the VDD-to-VSS ESD clamp circuits to effectively bypass the ESD current away from the internal circuits [11]-[12].

With a low trigger voltage and current, the LVTSCR in the ESD protection circuit is easily triggered on by the external noise pulses while the CMOS IC is in the normal operating conditions. Because the holding voltage of the LVTSCR is only around 1V, the voltage levels of the input or output signals can be destroyed if the LVTSCR in the input or output ESD protection circuits is accidentally turned on when the IC is in the normal operating conditions. This will cause some unexpected operation errors on the input or output signals and may generate failure or malfunction in the system applications.

Recently, due to the request of the "*CE*" mark from the *European Community*, an ESD gun with the ESD voltage of 8~15 KV is used to test the electromagnetic compatibility (EMC) of the electronic products [13]-[15]. During such system-level ESD/EMC testing, the power lines of the IC's in the system board can be coupled with an overstress voltage even up to several hundreds volts. Such a system-level ESD/EMC event easily causes the transient-induced latchup failure in the CMOS IC's [16]-[17]. If the lateral SCR or the LVTSCR are used as the ESD clamp devices between the VDD and VSS power lines of an IC [11]-[12], such ESD-protection SCR devices are easily triggered on by the system-level ESD/EMC transient pulses to cause very serious latchup problem in the CMOS IC's.

Although the LVTSCR can provide very effective ESD-protection capability within a much small layout area, the LVTSCR still can not be safely used in the input and output ESD protection circuits or the VDD-to-VSS ESD clamp circuits. In this paper, the novel cascode NCLSCR and PCLSCR devices with the holding voltage greater than VDD are proposed to safely apply the area-efficient SCR devices for whole-chip ESD protection but without the danger of VDD-to-VSS latchup problem.

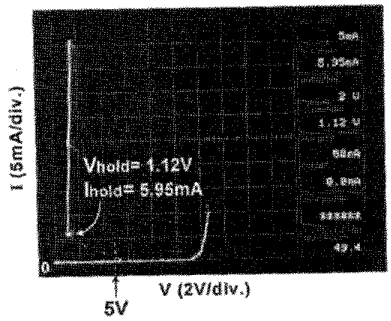

Fig.1 The typical I-V characteristics of an LVTSCR in a 0.6-μm CMOS technology.

The Cascode NCLSCR's and PCLSCR's

To avoid the accidental trigger-on and the VDD-to-VSS latchup problem, the holding voltage of the LVTSCR has to

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be greater than VDD of the IC. Using the double guard rings to surround both the anode and the cathode of an LVTSCR device can break the latching path and increase its holding voltage. The schematic I-V characteristics of the LVTSCR with an increased holding voltage is illustrated in Fig.2. But, increasing the holding voltage of an LVTSCR leads to more power dissipation (Power ≅ IESD×Vhold) located on the LVTSCR during the ESD transition. This will cause a lower ESD robustness of the LVTSCR. Moreover, to increase the holding voltage of an LVTSCR greater than VDD in the bulk CMOS process often needs to occupy much more layout area by using the latchup guard rings with the wider layout spacing.

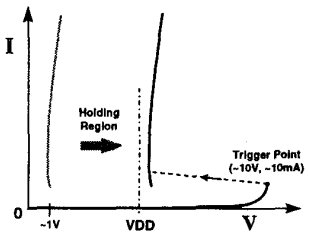


Fig.2 The schematic I-V characteristics of an LVTSCR device with an increased holding voltage to overcome the VDD-to-VSS latchup problem.

To increase the holding voltage of the LVTSCR but without increasing the power dissipation on the LVTSCR, a novel cascode configuration is proposed to realize such specification for both high ESD protection robustness and safe application without the latchup problem during the system-level ESD/EMC testing. The device structures of the proposed cascode NCLSCR's and PCLSCR's are shown in Fig.3(a) and 3(b), respectively, which are demonstrated in a p-substrate CMOS process. In Fig.3, the cathode of the NCLSCR1 (PCLSCR1) is connected to the anode of the NCLSCR2 (PCLSCR2), and the cathode of the NCLSCR2 is connected to the anode of the next NCLSCR (PCLSCR) device to configure the cascode NCLSCR's (PCLSCR's). All the gates of the NCLSCR's (PCLSCR's) are connected together and controlled by a control gate.

By using the cascode configuration, the total voltage drop across the cascode NCLSCR's (PCLSCR's) is the sum of the voltage drop across every NCLSCR (PCLSCR) device. Therefore, the holding voltage of the cascode NCLSCR's (PCLSCR's) become tunable by changing the number of the NCLSCR's (PCLSCR's) in the cascode configuration. If the cascode NCLSCR's include 6 NCLSCR devices, its total holding voltage can be greater than the 5-V VDD. Because each NCLSCR device still has a holding voltage of ~1V, the ESD power dissipation located on each NCLSCR device in the cascode NCLSCR's is still the same as that of an LVTSCR. The ESD robustness of the cascode NCLSCR's can be as well as that of the LVTSCR, but the cascode NCLSCR's have a holding voltage greater than VDD. So, the proposed cascode NCLSCR's (PCLSCR's) design can safely apply the advantages of the LVTSCR for whole-chip ESD protection but without causing the accidental trigger-on or the latchup problem in the CMOS IC's.

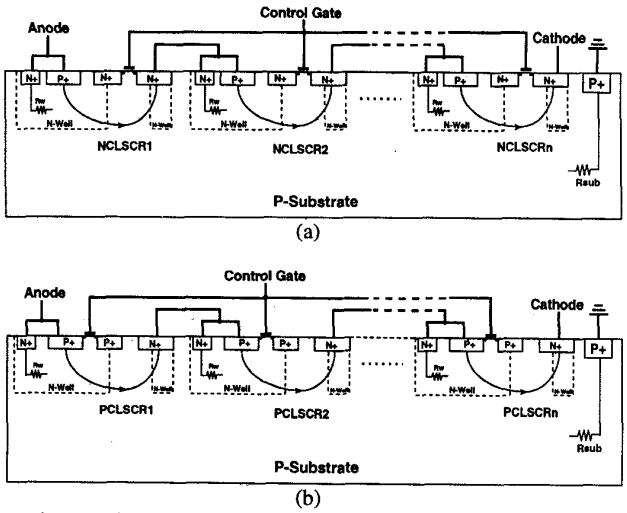


Fig.3 The schematic cross-sectional view of (a) the cascode NCLSCR device, and (b) the cascode PCLSCR device.

Characteristics of the Cascode NCLSCR's

The cascode NCLSCR's with different number of NCLSCR devices have been designed and fabricated in a 0.6-μm bulk CMOS process. The setup to measure the I-V characteristics of the cascode NCLSCR's is shown in Fig.4, where the *Tektronix* curve tracer 370A is used to generate the step gate voltage (VG) to the control gate and to measure the I-V curves of the cascode NCLSCR's.

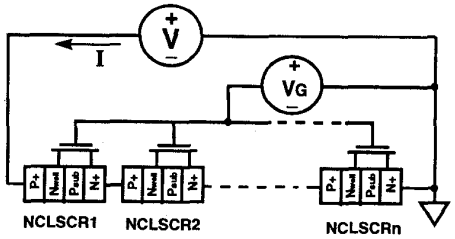


Fig.4 The setup to measure the I-V characteristics of the cascode NCLSCR's.

A. I-V Characteristics of the Cascode NCLSCR's :

The I-V curves of a single NCLSCR are shown in Fig.5 with different gate biases. The trigger voltage of the NCLSCR is significantly reduced as its gate voltage is increased. The holding voltage of a single NCLSCR is as low as 0.99V, which is much lower than the VDD of CMOS IC's. Such an NCLSCR in the ESD protection circuit is easily triggered on during the system-level ESD/EMC test or the high-temperature high-voltage reliability test to cause failures or malfunctions in the application systems.

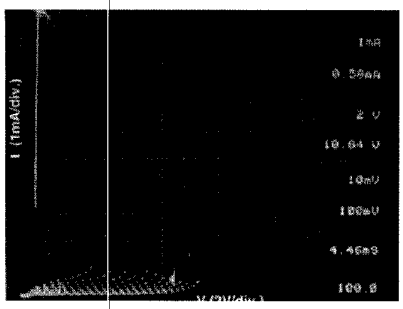
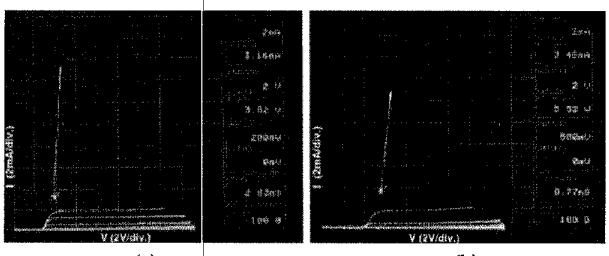


Fig.5 The I-V curves of a single NCLSCR device with different gate biases.

The I-V curves of the cascode NCLSCR's with four NCLSCR's and six NCLSCR's are shown in Fig.6(a) and 6(b), respectively, under different gate biases. With a positive gate voltage, the cascode NCLSCR's are easily triggered into the holding region. The holding voltage (current) of the 4-cascode NCLSCR's is 3.82V (3.16mA), whereas the holding voltage (current) of the 6-cascode NCLSCR's is 5.52V (3.48mA). The dependence of the holding voltage (current) of the cascode NCLSCR's on the number of the cascode NCLSCR devices is shown in Fig.7. The holding current of the cascode NCLSCR's is only slightly increased as the number of the cascode NCLSCR's is increased. But, the holding voltage of the cascode NCLSCR's is almost linearly increased as the number of the cascode NCLSCR's is increased. By adjusting the number of the cascode NCLSCR devices, the holding voltage of the cascode NCLSCR's becomes tunable to meet the different applications. For example, to safely apply the cascode NCLSCR's for ESD protection in the 5-V (3-V) CMOS IC's, six (four) NCLSCR devices have to be used in the ESD protection circuit without causing the accidental trigger-on or the latchup problem in the CMOS IC's. This cascode-NCLSCR's design provides a practical and useful solution to safely apply the LVTSCR for effective on-chip ESD protection.



(a) (b)

Fig.6 The I-V curves of the cascode NCLSCR's with (a) four NCLSCR devices, (b) six NCLSCR devices, under different gate biases.

B. Turn-on Verification of the Cascode NCLSCR's :

To verify the turn-on behavior of the cascode NCLSCR's, an experimental setup is shown in Fig.8, where the 4-cascode NCLSCR's is used to provide the safe ESD protection in the 3-V CMOS IC's. The ESD-like voltage pulse generated from a pulse generator (*hp*8118A) with a pulse width of 400ns and a rise time about 5.5ns is applied to the 4-cascode NCLSCR's. The pulse height (Vp) of the voltage pulse is adjusted to observe the turn-on behavior of the 4-cascode NCLSCR's. The control gate of the 4-cascode NCLSCR's is connected to the applied voltage pulse through a series resistor to turn on the NMOS's in the cascode NCLSCR's and also to prevent the overstress voltage on the gate oxide.

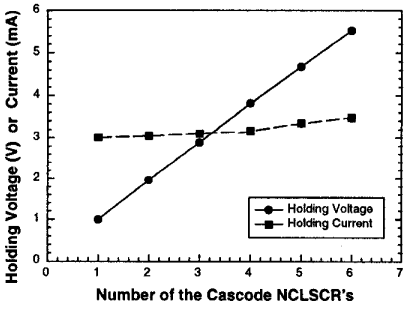


Fig.7 Dependence of the holding voltage (current) of the cascode NCLSCR's on the number of the cascode NCLSCR devices.

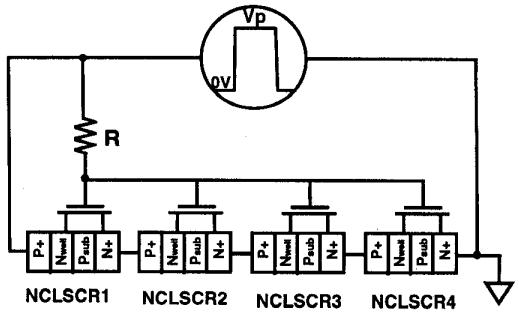
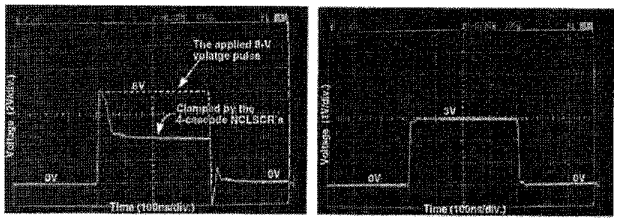


Fig.8 The setup to measure the turn-on behavior of the 4-cascode NCLSCR's.

The 4-cascode NCLSCR's have a holding voltage of 3.82V. When the applied voltage pulse has a pulse height greater than the holding voltage, the 4-cascode NCLSCR's will be triggered on to clamp the applied voltage pulse to the voltage level around the holding voltage. The clamped voltage waveform due to the triggering of a 8-V voltage pulse is shown by the solid line in Fig.9(a), where the originally generated 8-V voltage pulse is shown by the dashed line. The 8-V voltage pulse is clamped to about 3.9V by the turned-on 4-cascode NCLSCR's. So, the ESD pulse can be effective clamped by the proposed cascode NCLSCR's. If the applied voltage pulse has a pulse height of only 3V, the measured voltage waveform across the 4-cascode NCLSCR's is shown in Fig.9(b). The 3-V voltage pulse is not degraded by the 4-csacode NCLSCR's, because the 4-cascode NCLSCR's are not triggered on by the 3-V voltage pulse even if their control gates are biased at 3V. So, the voltage waveform in Fig.9(b) is still kept as a square

shape. With a holding voltage greater than VDD of the IC, the cascode NCLSCR's can provide effective on-chip ESD protection but also really keep off when the IC is in the normal operating conditions with the power supplies. This has practically verified the safe application of the cascode NCLSCR's for ESD protection in the CMOS IC's.

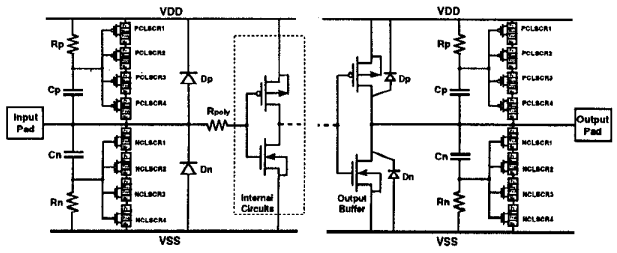


(a) (b)

Fig.9 The voltage waveform clamped by the 4-cascode NCLSCR's due to the triggering of a (a) 8-V, or (b) 3-V, voltage pulse.

Applications for Whole-Chip ESD Protection

The cascode NCLSCR's (PCLSCR's) have been applied in a 0.35-μm CMOS technology to sustain an HBM ESD level greater than 3KV. The typical input and output ESD protection circuits using the 4-cascode NCLSCR's and 4-cascode PCLSCR's with the gate-coupled technique [3] for 3-V CMOS IC's are shown in Fig.10(a) and 10(b), respectively. The gate-coupled technique is used to earlier trigger on the cascode NCLSCR's (PCLSCR's) for more effective ESD protection. The VDD-to-VSS ESD clamp circuits using the cascode NCLSCR's and the cascode PCLSCR's with the RC-based control circuit [8]-[10] are shown in Fig.11(a) and 11(b), respectively. The number of the cascode NCLSCR's (PCLSCR's) is dependent on the voltage level of VDD in the CMOS IC's. For the 5-V CMOS IC's, the 6-cascode NCLSCR's (6-cascode PCLSCR's) are used in the VDD-to-VSS ESD clamp circuits to effective clamp the ESD voltage across the VDD and VSS power lines but without causing the VDD-to-VSS latchup problem.

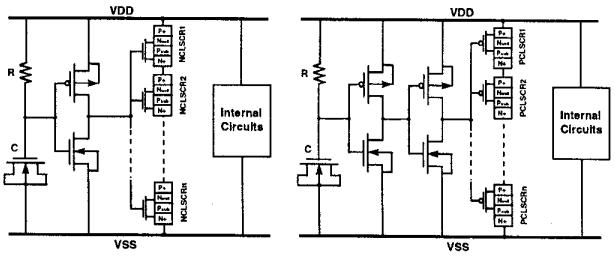


(a) (b)

Fig.10 The (a) input, and (b) output, ESD protection circuits using the cascode NCLSCR's and PCLSCR's with the gate-coupled technique.

Conclusion

A novel cascode NCLSCR's and PCLSCR's design has been successfully used to linearly adjust the holding voltage of the LVTSCR in the ESD protection circuit. With a holding voltage greater than VDD of the CMOS IC's, the proposed cascode NCLSCR's and PCLSCR's can provide effective ESD protection with the ESD level as high as that of the LVTSCR device. But, the cascode NCLSCR's (PCLSCR's) are free to the unexpected trigger-on or the VDD-to-VSS latchup problem when the IC's is in the normal operating conditions or in the system-level ESD/EMC reliability tests.



(a) (b)

Fig.11 The VDD-to-VSS ESD clamp circuit using (a) the cascode NCLSCR's, and (b) the cascode PCLSCR's, with the RC-based control circuit.

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