ESD Protection Design and Verification in a 0.35-μm CMOS ASIC Library

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Abstract — In this paper, ESD protection design on the I/O cells of a CMOS ASIC library in a 0.35-μm silicide CMOS technology is proposed with practical verification on the experimental testchips. The whole-chip ESD robustness of such I/O cells in the 0.35-μm CMOS ASIC library has been practically investigated by four 40-pins testchips with internal core circuits. By applying the efficient VDD-to-VSS ESD clamp circuit and the ESD-related process modifications, the whole-chip human-body-model (machine-model) ESD level of this 0.35-μm CMOS ASIC library can be greater than 6kV (1kV). By including the clamp devices into the input stage, the charged-device-model ESD level of the input pin can be greater than 2kV.

I. Introduction

Due to the scaled-down device dimensions, such as the thinner gate oxide and shallower junction depth in deep-submicron CMOS technologies, ESD protection has become one of the hottest issues on CMOS IC reliabilities. For commercial IC products, the human-body-model (HBM) [1] and machine-model (MM) [2] ESD specifications are generally defined as 2000V and 200V, respectively. The charged-device-model (CDM) [3] ESD specification is often defined as 1000V. Therefore, the I/O cells in a CMOS cell library should be designed with the considerations on both circuit functions and ESD robustness.

Due to the trend of system-on-a-chip (SOC), more circuit functions are integrated into a single chip. Such SOC IC's fabricated in the deep-submicron CMOS technologies with more metal layers (4 metal layers in the typical 0.35-μm CMOS process, 5 metal layers in the 0.25-μm CMOS process, and so on) often have high I/O pin counts. In the high-pin-count communication or chip-set IC's, the die sizes are mainly decided by the pitch of I/O cells with the bond pads. To reduce the die size, the total layout area for an I/O cell with a bond pad, the I/O function devices, and ESD clamp devices is seriously limited for applications in such high-pin-count IC's.

In this paper, an area-efficient design on the I/O cells with high ESD robustness is proposed. Four testchips including the internal core circuits of a 16-bit counter and four different ring oscillators have been especially designed to practically verify the efficiency of such I/O cells in a 0.35-μm CMOS process.

II. Design of the I/O Cells

The basic circuits for the input, output, and bi-directional cells are shown in Fig.1. The cell layout of every I/O cell in the 0.35-μm CMOS ASIC library has the same cell height and cell width. The cell width of 98 μm is decided by the pad pitch from the bonding specification for high-pin-count applications, which includes the square bond-pad metal layers of 93×93 μm^2. To improve ESD robustness, an additional RPO mask layer is used in the 0.35-μm CMOS process [4] to block the silicided diffusion in the drain/source regions of the I/O devices. Therefore, the clearance from the drain (source) contact to the poly gate of the output PMOS and NMOS is drawn as 3.0 (1.15) μm, whereas the RPO layer in the drain (source) region has a silicide-blocking spacing of 2.6 (0.75) μm. Under such a cell width of 98 μm, 14 finger-type poly gates can be drawn in parallel to form the PMOS and NMOS in the I/O cells.

The cell height is mainly decided from the device dimensions in the output buffer which provides the required maximum driving/sinking current. In this 3-V 0.35-μm CMOS ASIC library, the driving/sinking currents in the output cells are specified as 4, 8, 10, 14, 18, and 24mA for different ASIC applications. A PMOS (NMOS) device with a dimension of W/L=35μm/0.5μm, under the biases of Vds=-0.6V and Vgs=-3V (Vds=0.4V and Vgs=3V) in the pseudo-worst simulation condition at the temperature of 85°C with the typical-case *HSPICE* parameters, can provide 2mA (4mA) driving (sinking) current to (from) the pad. Therefore, the channel width of the unit-finger in the finger-type output PMOS and NMOS is selected as 35μm in the cell layout. For output cells with different current specifications, different numbers of the poly gates in the finger-type layout are connected to the pre-buffer circuits. The non-used poly gates in the finger-type PMOS (NMOS) layout are connected to VDD (VSS) through an N-well resistor of 2 kΩ. Including the layout spacing and width for the guard rings to prevent latchup, the total cell height is only 245 μm which has included the square bond-pad metal layers of 93×93 μm^2.

The input cell is designed by connecting all poly gates in the finger-type layout of the output devices to VDD or VSS through the N-well resistor (Rw1 and Rw2 in Fig.1) of 2 kΩ to turn off the devices. A poly resistor (Rpoly in Fig.1) of 325Ω is connected between the pad and the input stage to avoid the overstress on the gate oxide of the input stage. The finger numbers for the I/O cells with different current specifications are listen in Table I. By using such circuit

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design and layout arrangement, the input, output, and bi-directional cells have the same layout style and area. The practical layout examples of the input cell (I00H), the tri-state output cell (T10H), and the bi-directional I/O cell (BU10H) in this CCL's 0.35-μm CMOS ASIC library are demonstrated in Fig.2.

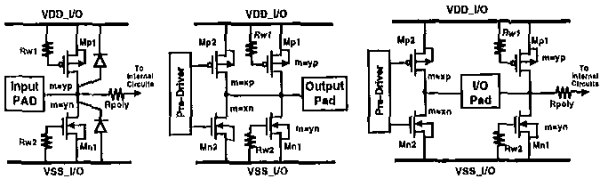


Fig.1 The schematic circuit diagrams of the (a) input, (b) output, and (c) bi-directional I/O cells in a 0.35-μm CMOS ASIC library.

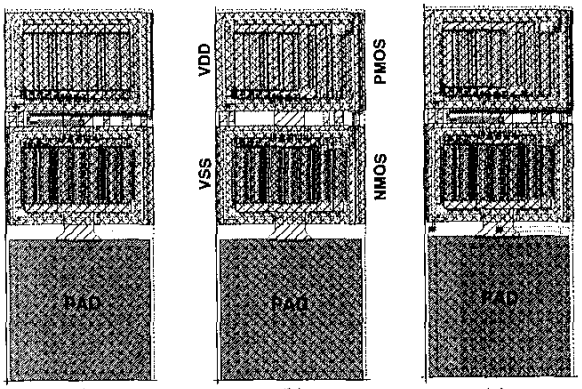


Fig.2 The practical layout examples of the (a) input cell (I00H), (b) tri-state output cell (T10H), and (c) bi-directional I/O cell (BU10H) in a 0.35-μm CMOS ASIC library.

TABLE I
The relations between the finger numbers and the driving/sinking currents in the I/O cells

W/L= 35/0.5 for each Finger		Finger Number			
		xp	xn	yp	yn
Current Specification	Input cell	0	0	14	14
	4mA	2	1	12	13
	8mA	4	2	10	12
	10mA	5	3	9	11
	14mA	7	4	7	10
	18mA	9	5	5	9
	24mA	12	6	2	8

III. DESIGN OF THE VDD AND VSS CELLS

In the cell library, the VDD and VSS pads to provide power supplies for the I/O cells are generally separated from those for the internal circuits. Such VDD/VSS cells also occupy the same layout area as that of an I/O cell. To improve ESD robustness of the I/O cells and to achieve the whole-chip ESD protection [5], the VDD-to-VSS ESD clamp circuits are inserted into the VDD/VSS cells. In the CCL's ASIC library, an area-efficient VDD-to-VSS ESD clamp circuit is added into the power pads. The VDD and VSS cells with the area-efficient VDD-to-VSS ESD clamp circuit are shown in Fig.3, where a *RC*-based ESD-detection circuit is used to turn on the substrate-triggered field-oxide device (STFOD) [6]-[7] during the ESD-stress condition. Such a design is also applied to the VDD cell which is used to supply the power for internal circuits. To provide the ESD current discharging path between the I/O VSS and internal VSS cells to avoid the unexpected ESD damage on the internal circuits, an NMOS is added into the VSS cell for internal circuits. The circuit diagrams for the VDD and VSS cells used to supply the power for internal circuits are shown in Fig.4. The layout examples of the power cells are demonstrated in Fig.5, where every cell has the same layout area as that of an I/O cell.

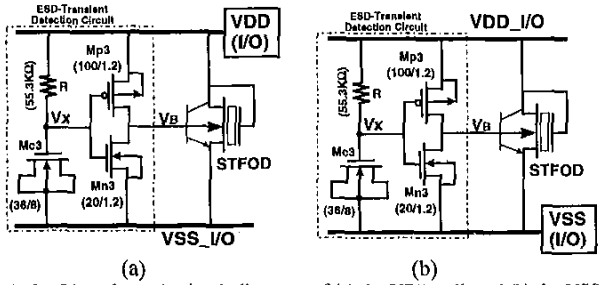


Fig.3 The schematic circuit diagrams of (a) the VDD cell, and (b) the VSS cell, to supply the power for the I/O cells.

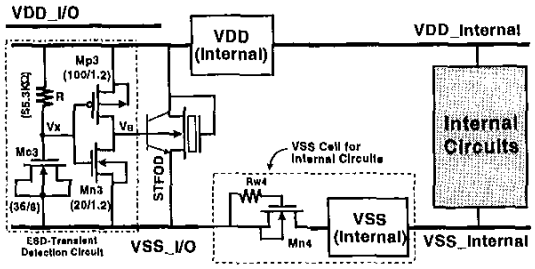


Fig.4 The schematic circuit diagrams of the VDD and VSS cells to supply the power for the internal circuits.

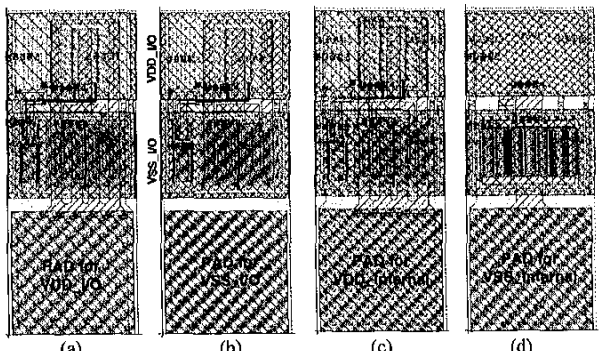


Fig.5 Layout examples of the (a) VDD_I/O, (b) VSS_I/O, (c) VDD_internal, and (d) VSS_internal cells in the 0.35-μm CMOS ASIC library.

IV. WHOLE-CHIP ESD PROTECTION

While an IC has a large chip size, the parasitic capacitance and resistance along the VDD/VSS power lines which surrounding the whole chip easily cause the unexpected ESD failure located on the internal circuits [8]-[10]. Therefore, the area-efficient VDD-to-VSS ESD clamp circuit is added into the corner cell to improve the whole-chip ESD level. Moreover, an ESD cell with only the VDD-to-VSS ESD clamp circuit is especially designed for placing between the VDD_I/O and VSS_I/O power rails. Such an ESD cell is empirically suggested to be inserted between the I/O cells in every 2000-μm distance in the whole-chip ESD protection scheme. The VDD-to-VSS ESD clamp circuit in the corner cell and the ESD cell is the same as that used in the VDD_I/O or VSS_I/O cells but without including the bond pads. The practical layout examples of the corner cell and the ESD cell are shown in Fig.6.

The whole-chip ESD protection scheme in a chip is illustrated in Fig.7, where the ESD clamps are added into the corner, the power cells, and the center of each I/O side. With the effective VDD-to-VSS ESD clamp circuit, the ESD current path during the I/P-to-VSS ESD-stress condition is illustrated in Fig.8. The ESD current path during the pin-to-pin ESD-stress condition is illustrated in Fig.9. As seen in Figs. 8 and 9, the VDD-to-VSS ESD clamp circuit can provide effective conducting path to discharge ESD current. Therefore, the ESD level on the I/O cells can be significantly increased by the VDD-to-VSS ESD clamp circuits. The ESD-protection strategy in CCL's ASIC library is to fully use the VDD-to-VSS ESD clamp circuits across the VDD and VSS power lines but without increasing the device dimensions in the input or output cells. Therefore, the layout area of the I/O cell can be drawn as small as possible to only meet the maximum driving/sinking current specification. The ESD level of the I/O cells is mainly sustained by the added VDD-to-VSS ESD clamp circuits between the power lines. Moreover, the VDD-to-VSS ESD clamp circuits can really provide the effective protection for the internal circuits to avoid the internal ESD failure issues [8]-[10].

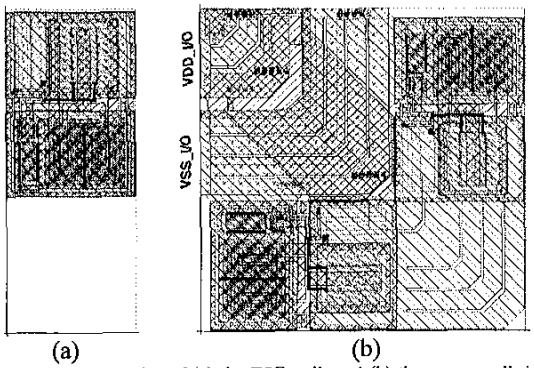


Fig.6 Layout examples of (a) the ESD cell, and (b) the corner cell, in the 0.35-μm CMOS ASIC library.

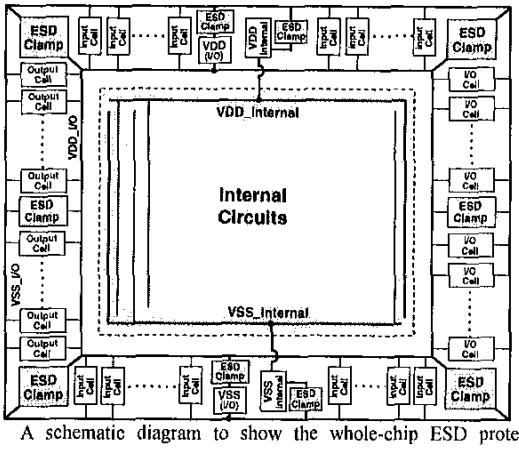


Fig.7 A schematic diagram to show the whole-chip ESD protection scheme.

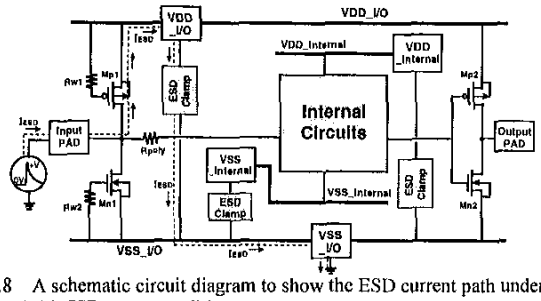


Fig.8 A schematic circuit diagram to show the ESD current path under the I/P-to-VSS ESD-stress condition.

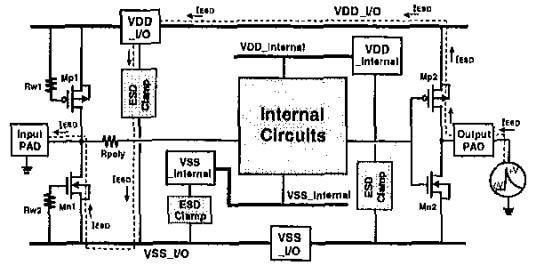


Fig.9 A schematic circuit diagram to show the ESD current path under the pin-to-pin ESD-stress condition.

V. CDM ESD PROTECTION

Due to the thinner gate-oxide thickness of only 70_ in the 0.35-μm CMOS process, the input stage of CMOS IC's is more sensitive to ESD damages caused by the charged-device-model (CDM) ESD events [11]-[12]. In the CDM ESD events, the electrostatic charges are initially stored in the body of the IC's. When the pins of the charged IC's touch to ground, the electrostatic charges in the charged IC's are conducted from the IC's to the external ground and therefore generate the discharging current. Such CDM ESD events with an ESD voltage of 1000V can generate a peak discharging current of ~15A within a rise time of below 150ps [13].

Such a fast and large ESD discharging current will cause the burned-out phenomenon on the output devices. But, if the output NMOS and PMOS have enough device dimensions, they can still sustain the 1000-V CDM ESD stress in the deep-submicron CMOS technologies [14]-[15]. But in the input pin, the gate oxide of the input stage had been found to be ruptured by the CDM ESD stress even if the input pin can sustain a high HBM ESD stress [12]. The schematic diagram to show the negative electrostatic charges stored in a p-substrate CMOS IC and discharged through an input pin is illustrated in Fig.10, whereas the equivalent circuit of such a CDM ESD event is drawn in Fig.11. The CDM ESD current discharging paths are indicated by the dashed lines in Figs. 10 and 11. The well-designed input ESD protection circuit located around the input pad can effectively clamp the HBM ESD voltage across the gate oxide of the internal input stage, but such an HBM input ESD protection circuit can not protect the gate oxide of the input stage in the CDM ESD events even if there is a series resistance connected between the input pad and the input stage. In the CDM ESD events, the ESD current comes from the substrate body of the IC itself, therefore the HBM ESD protection circuit around the input pad can not protect the IC against such CDM ESD stress.

To clamp such CDM ESD stress across the gate oxide of the input stage, the additional ESD clamp devices are added into the internal input stage, as shown in Fig.12. The additional NMOS Mn1b (PMOS Mp1a) with a device dimension of only 14.8μm/0.35μm is used to locally limit the ESD voltage across the gate oxide of the input stage. The VSS (VDD) power line connected to the Mn1b (Mp1a) has to be the same VSS (VDD) power line that is connected to the Mn5 (Mp5) of the input stage. Moreover, the Mn1b and Mp1a have to be drawn as close as possible to the gate oxide of the Mn5 and Mp5 in the cell layout of the input stage. The typical cell layout of the input stage in this 0.35-μm ASIC library is shown in Fig.13, where the drains of Mn1b and Mp1a still have a suitable layout spacing from the drain contact to the poly gate to avoid damage during the HBM ESD stress.

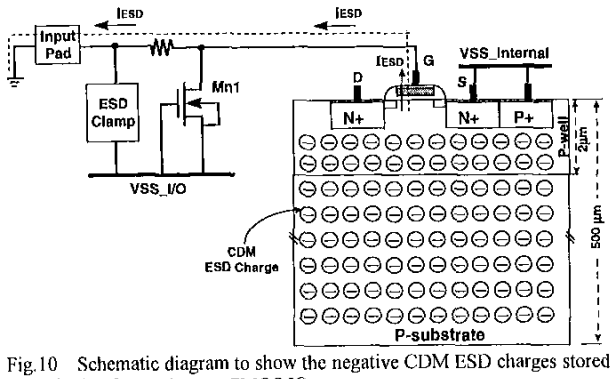


Fig.10 Schematic diagram to show the negative CDM ESD charges stored in the body of a p-substrate CMOS IC.

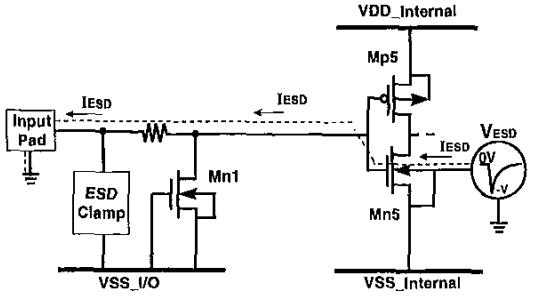


Fig.11 Equivalent circuit diagram to show the ESD discharging current path in a p-substrate CMOS IC during the negative CDM ESD stress.

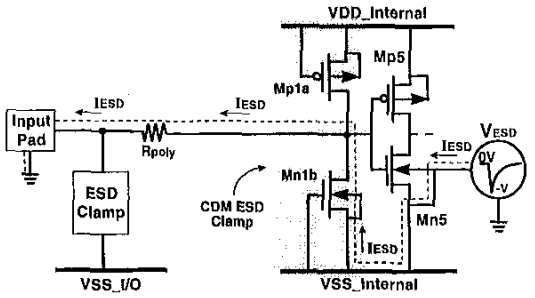


Fig.12 ESD protection design for the input pin to clamp the CDM ESD stress across the gate oxide of the input stage.

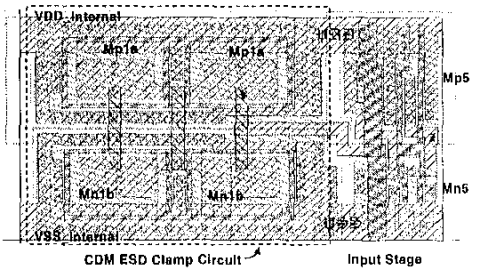
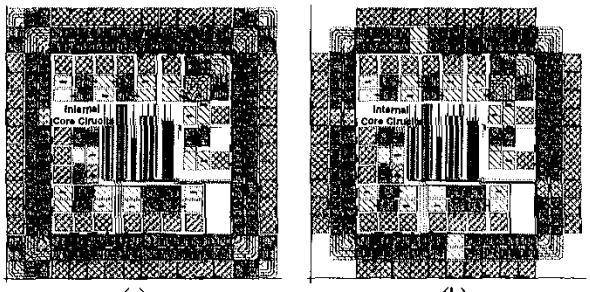


Fig.13 The layout example of the input stage with the CDM ESD clamp devices (Mn1b and Mp1a).

VI. TESTCHIPS FOR ESD VERIFICATION

To verify the ESD performance of the I/O cells in this 0.35-μm ASIC library, four 40-pin testchips had been designed and fabricated with/without VDD-to-VSS ESD clamp circuits or ESD-implant/PRO layers on a same wafer in a 0.35-μm silicide CMOS process. The whole-chip layouts of the testchips with and without the VDD-to-VSS ESD clamp circuits are shown in Fig.14(a) and 14(b), respectively. The experimental combination to form the four testchips is listen in Table II to practically verify the effectiveness of the whole-chip ESD protection design. All of the four testchips include the internal core circuits inside the chips, which are surrounded by the I/O cells with bond pads at the four sides of the chips. The internal core circuits include a 16-bit counter and four different ring oscillators. Such four test-chips are assembled in the DIP 40-pin packages and tested by the *ZapMaster* ESD tester to find their ESD levels.



(a) (b)

Fig.14 The whole-chip layout of the 40-pin testchips including the internal core circuits for ESD verification, in (a) with VDD-to-VSS ESD clamp circuit, in (b) without VDD-to-VSS ESD clamp circuit.

TABLE II
The different combinations with design or process in the four testchips.

Testchip	VDD-to-VSS ESD Clamp (Design)	ESD / RPO Layers (Process)
T1	Yes	Yes
T2	No	Yes
T3	Yes	No
T4	No	No

VII. Experimental Results

The four testchips are tested by the HBM, MM, and CDM ESD stresses. At each ESD test condition, three samples are used to verify the ESD robustness of the testchips. After the ESD zapping (three zaps at every ESD voltage level), both of the leakage current at each I/O pin and the function of internal core circuits are checked to judge the ESD levels of the testchips. The output frequencies of the ring oscillators in the testchips are also monitored to judge whether the ESD damage is located in the internal core circuits.

From the experimental results, the testchip T1 with both the design of VDD-to-VSS ESD clamp circuits and the process modification of ESD/RPO layers can sustain the HBM (MM) ESD level greater than 6kV (1kV). The testchip T2, only using the process modification of ESD/RPO layers but without the VDD-to-VSS ESD clamp circuits, can not sustain the HBM (MM) ESD stress of 3kV (300V). These test results have clearly verified that the whole-chip ESD protection design (shown in Fig.7) with the VDD-to-VSS ESD clamp circuits can significantly improve the ESD level of the IC's.

The CDM ESD protection design on the input pin (shown in Fig.12) is also verified by the socket-mode CDM ESD stress. Two input pins are especially placed in the testchips. One is designed as that shown in Fig.12 with the CDM ESD clamp circuit around the input stage that is connected to the input pin. The other input pin is placed in the testchip and connected to an input stage in the internal core circuits but without the CDM ESD clamp circuit around the input stage. The input stage with the CDM ESD clamp circuit can pass the CDM ESD stress of greater than 2kV, but that without the CDM ESD clamp circuit can not sustain the CDM ESD stress of 1kV. This verifies the effectiveness of the CDM ESD protection design in the CCL's 0.35-μm ASIC library.

VIII. Conclusion

ESD protection design and verification method to verify the ESD robustness of I/O cells in a CMOS cell library have been demonstrated in this paper. By the detailed investigation on the testchips where the internal circuits and I/O cells are designed and placed as those in the real IC products, the ESD performance of a 0.35-μm CMOS ASIC library has been practically verified. The ESD level of the I/O cells can be significantly improved by the additional VDD-to-VSS ESD clamp circuits. Therefore, the device dimensions and layout area in each I/O cell can be reasonably reduced for application in the high-pin-count IC's.

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