ESD Protection Design on Analog Pin with Very Low Input Capacitance for RF or Current-Mode Applications

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Abstract --- An ESD design is proposed to solve the ESD protection challenge to the analog pins for high-frequency or current-mode applications. By including an efficient power-rails clamp circuit into the analog I/O pin, the device dimension (W/L) of ESD clamp devices in the analog ESD protection circuit can be reduced to only 50/0.5 (μm/μm) in a 0.35-μm silicided CMOS process, but it can sustain the HBM (MM) ESD level of up to 6kV (400V). With such smaller device dimensions, the input capacitance of this analog ESD protection circuit can be significantly reduced to only ~1.0 pF (including the bond pad capacitance) for high-frequency applications.

I. INTRODUCTION

Due to the low breakdown voltage of the gate oxide in deep-submicron CMOS technologies, the efficient input electrostatic discharge (ESD) protection circuit should be designed and placed on every input pad to clamp the overstress voltage across the gate oxide of the first input circuit. A conventional ESD protection design with the two-stage structure for digital input pin is shown in Fig.1, where a gate-grounded short-channel NMOS is used as the secondary protection device to clamp the overstress voltage across the gate oxide of the input circuit. To provide a high ESD level, a robust device (such as SCR [1], field-oxide device, or long-channel NMOS) is used in the primary protection stage to bypass ESD current on the input pad. Between the primary stage and the secondary stage of the input ESD protection circuit, a resistor is added to limit the ESD current flowing through the short-channel NMOS in the secondary stage. The resistance value of this resistor is dependent on the turn-on voltage of the ESD clamp device in the primary stage and the It2 (secondary breakdown current) of the short-channel NMOS in the secondary stage. The resistance was designed large enough (in the order of kΩ [1]), so the primary ESD clamp device can be triggered on to bypass ESD current before the gate-grounded NMOS (ggNMOS) in the secondary stage was damaged by the overstress ESD current. Such two-stage ESD protection design can provide high ESD level for the digital input pins. But the large series resistance and the large junction capacitance in the ESD clamp devices cause a long *RC* timing delay to the input signals, it is not suitable for analog pins, especially for the high-frequency or current-mode applications.

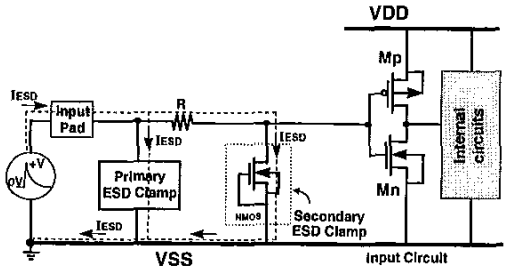

Fig.1 A schematic diagram of the conventional two-stage ESD protection circuit for digital input pin in CMOS IC's.

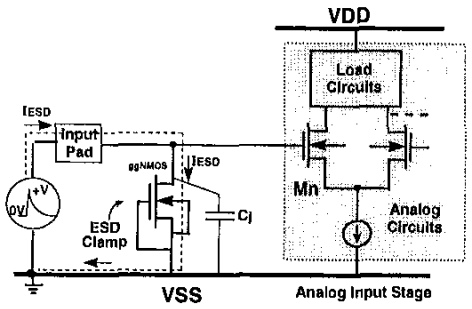

Fig.2 A schematic diagram of the single-stage ESD protection circuit for analog input pin in CMOS IC's.

For current-mode input signal or high-frequency applications, the series resistance between the input pad and input circuits is forbidden. Therefore, the two-stage ESD protection design in Fig.1 is no longer suitable for analog input pins. To protect the analog input pin, the typical ESD protection circuit with a single-stage ESD protection design is shown in Fig.2, where a ggNMOS is used as the ESD clamp device. Due to the lack of a series resistance to limit ESD current toward the ggNMOS, as well as the ESD robustness of the NMOS device is seriously degraded by the advanced deep-submicron CMOS technologies [2]-[3], such a ggNMOS is often designed with a larger device dimension and a wider drain-contact-to-poly-gate spacing to sustain an acceptable ESD level [3]-[4]. The additional silicide-blocked mask had been included into the deep-submicron CMOS process to increase ESD robustness of the ESD clamp device. The schematic cross-sectional view of a ggNMOS with the silicide-blocked drain region is illustrated in Fig.3. But the

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ggNMOS with a larger device dimension and a wider drain spacing contributes a larger parasitic drain capacitance to the input pad. Such a parasitic junction capacitance is nonlinear and dependent on the input voltage level. This nonlinear input capacitance can cause serious distortion on the analog circuit performance or resolution, such as the harmonic distortion [5]. Thus, it has become an emergent challenge to design an effective ESD protection circuit for high-performance analog input and output pins.

In this paper, a novel ESD protection design with the advantages of small input capacitance, no series resistance, and high ESD level, has been practically implemented in a 0.35-μm CMOS technology to protect the analog pins for high-frequency and high-performance applications.

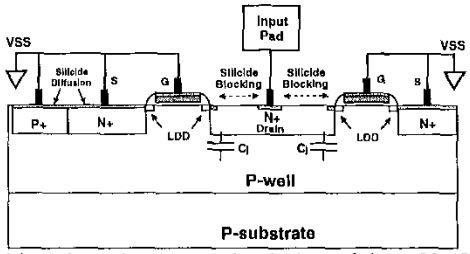


Fig.3 The schematic cross-sectional view of the ggNMOS with the silicide-blocked drain region.

II. ESD Test on Analog Input/Output Pins

To investigate the ESD robustness of input / output pins in IC's, the pin combinations during the ESD stress had been specified in the standard [6]. For an input pin, there are four basic ESD-stress modes, as shown in Fig.4, where the ESD voltage is applied to an input pin with the VDD or VSS pins relatively grounded. Except for such ESD-testing pin combinations, an additional pin-to-pin ESD stress had been also specified in the standard [6] for the analog circuits with operational amplifiers or differential input stages to verify the ESD level of the analog input pins. The analog pin-to-pin ESD stress for the differential input pins of an operational amplifier is illustrated in Fig.5, where the positive or negative ESD voltage is applied to the inverting input pin with the corresponding non-inverting input pin relatively grounded. During such an analog pin-to-pin ESD stress, all the other pins including both the VDD and VSS pins are floating.

The ESD current during such an analog pin-to-pin ESD stress is illustrated in Fig.6 with the differential input stage of an operational amplifier. Because of the lack of series resistor between the analog input pad and the input circuits, the overstress ESD current easily reaches to the input gate oxide of the differential input stage with a common-source circuit structure. If the VSSA power connection between the inverting input and non-inverting input has a longer metal line in the IC layout, the gate oxides of the differential input stage are easily ruptured by the ESD voltage to cause a discharging current path as the dashed line shown in Fig.6. The ESD clamp device (such as the large-dimension ggNMOS in Fig.2) between the inverting input pad and the VSSA power line can not provide effective ESD protection against this additional analog pin-to-pin ESD stress. Therefore, some advanced designs should be included into the analog ESD protection circuit to overcome this analog pin-to-pin ESD-stress issue.

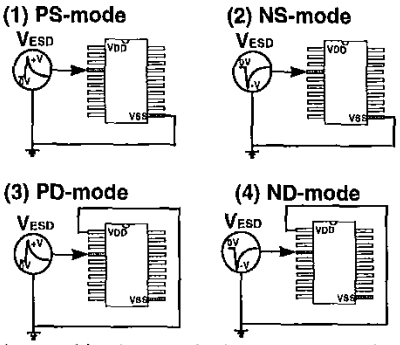


Fig.4 Testing combinations on the input or output pin of an IC in the Human-Body-Model (HBM) ESD stress.

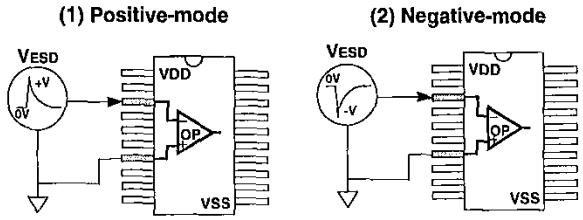


Fig.5 The pin combination of the additional analog pin-to-pin ESD stress to verify the ESD level of analog circuits with the operational amplifier or differential input stage.

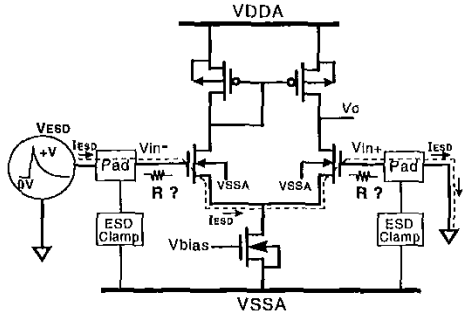


Fig.6 The ESD current path during the analog pin-to-pin ESD stress.

III. ESD Protection Design for Analog Pins

A. Circuit Configuration and Operation

The proposed ESD protection circuit for analog pins is shown in Fig. 7, whereas its practical layout in a 0.35-μm

silicided CMOS cell library is drawn in Fig.8. In order to reduce the input capacitance of the analog pin, the Mn1 and Mp1 are both designed with a much smaller device dimension of only 50/0.5 (μm/μm) in Fig.7. The HBM ESD level of a stand-alone NMOS with a device dimension of 50/0.5 (μm/μm) is less than 500V in the 0.35-μm silicided CMOS process, while the NMOS is tested in the PS-mode ESD stress. But, such a small NMOS can sustain an HBM ESD level of 8000V in the same 0.35-μm silicided CMOS process, while the NMOS is tested in the NS-mode ESD stress. In the PS-mode (NS-mode) ESD stress, the NMOS is operated in its drain-breakdown condition (drain diode forward-bias condition) to bypass ESD current. Therefore, the NMOS has quite different ESD levels between the PS-mode and NS-mode ESD stresses. Similarly, a stand-alone PMOS with a small device dimension also has a high ESD level in the PD-mode ESD stress but a much low ESD level in the ND-mode ESD stress.

To avoid the small Mn1 and Mp1 into the drain-breakdown condition in the PS-mode and ND-mode ESD stresses to cause a much low ESD level, an efficient ESD clamp circuit between the power rails is co-constructed into the analog ESD protection circuit to increase the overall ESD level. In Fig.7, the *RC*-based ESD detection circuit [7] is used to trigger on the Mn3 device, when the input pad is tested in the PS-mode or ND-mode ESD stresses. The ESD current paths in this analog ESD protection circuit are illustrated by the dashed lines in Fig.9(a) and 9(b), respectively, when the input pin is tested in the PS-mode and ND-mode ESD stresses. Because the Mn1 in the PS-mode (Mp1 in the ND-mode) ESD stress is not operated in the drain-breakdown condition, the ESD current is bypassed through the forward-biased drain diode Dp1 in Mp1 (Dn1 in Mn1) and the turned-on Mn3 between the VDD/VSS power rails. The Mn3 is especially designed with a larger device dimension (1800/0.5 in Fig.8) to sustain a high ESD level. Although the large-dimension Mn3 has a large junction capacitance, this capacitance does not contribute to the input pad. Therefore, the analog pin can sustain much higher ESD levels in the four-mode ESD stresses but only with a much smaller input capacitance.

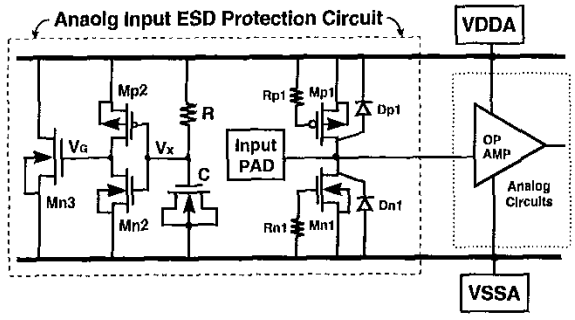


Fig.7 The proposed ESD protection circuit for analog input pins.

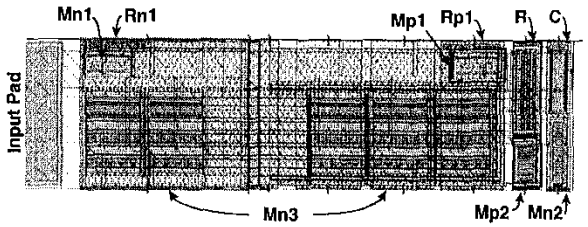


Fig.8 Layout example of the proposed ESD protection circuit for analog input pins in a 0.35-μm silicided CMOS process.

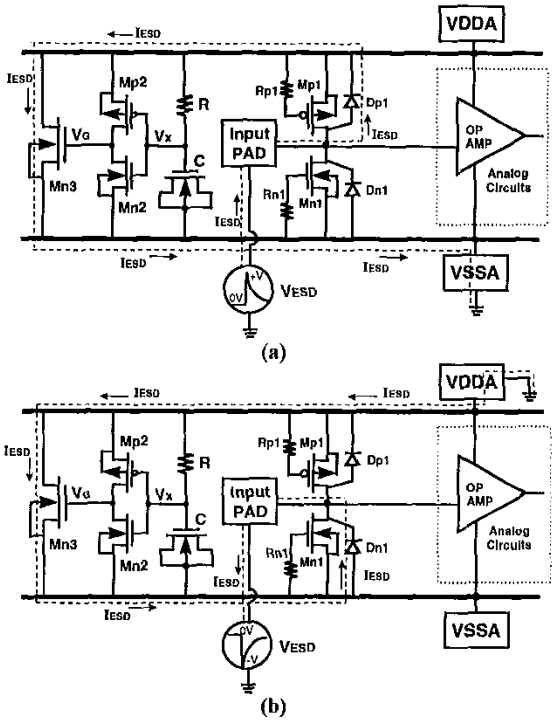


Fig.9 The ESD current path in the proposed analog ESD protection circuit when the input pin is tested in (a) the PS-mode, (b) the ND-mode, ESD stress.

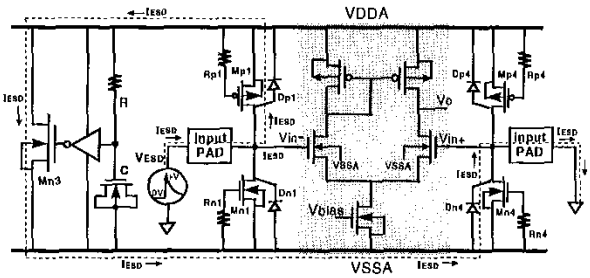


Fig.10 The ESD current path in the proposed analog ESD protection circuit when the input pins are tested in analog pin-to-pin ESD stress.

When the input pins are tested in the analog pin-to-pin ESD stress (Fig.6), the ESD current path along this proposed

analog ESD protection circuit is illustrated in Fig.10. By using this design, the gate oxide of analog differential input stage can be fully protected without adding any series resistance between the input pad and the analog input stage.

B. Input Capacitance

The input capacitance of this proposed analog ESD protection circuit can be calculated as :

$$Cin = Cpad + Cjp + Cjn, \quad (1)$$

where the Cpad is the parasitic capacitance of the bond pad. The Cjp (Cjn) is the drain junction capacitance and the drain-to-gate overlapped capacitance in the Mp1 (Mn1). The drain junction capacitance of NMOS or PMOS is bias-dependent [5]. The input capacitance of the previous protection design with a single NMOS in Fig.2 extensively varies when the input signal has different voltage levels. But, the input capacitance of the proposed analog ESD protection circuit (Fig.7) with complementary PMOS and NMOS structure can be kept almost constant even if the input signal has a voltage swing from 0V to VDD (3V). The total input junction capacitance of the analog ESD protection circuit with different device dimensions are accurately calculated in the frequency domain by using the pin-capacitance-measurement simulation [8] in the *Star-Hspice* CAD tool.

The calculated results are shown in Fig.11, where the channel widths of Mn1 and Mp1 vary from 50μm to 400μm with a fixed channel length of 0.5μm under different voltage levels on the input pad. The drain-contact-to-poly-gate spacing in both Mn1 and Mp1 is drawn as 3.4μm, whereas the source side spacing is drawn as 1.55μm. With both device dimensions of 50/0.5 in Mn1 and Mp1, the input junction capacitance is only varying from 0.37pF to 0.4pF when the input voltage swing is from 0V to 3V.

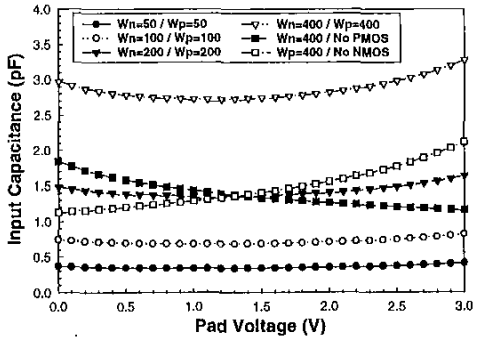


Fig.11 The input junction capacitance of the analog ESD protection circuit with different device dimensions in Mn1 and Mp1 during different input voltage levels on the input pad.

TABLE I

	Pin Combination in ESD Test				
	PS-mode	NS-mode	PD-mode	ND-mode	Pin-to-Pin
HBM (V)	6000	- 6000	7000	- 7000	6000
MM (V)	400	- 400	400	- 400	400

The layout size of the metal bond pad for wire bonding in the 0.35-μm CMOS process is specified as 96×96μm^2, which contributes a parasitic Cpad of 0.67pF. So, the total Cin of this analog ESD protection circuit including the bond pad is only about 1.04~1.07 pF, even if the input signal has different voltage levels. With such a small and almost constant input capacitance, this proposed analog ESD protection circuit is more suitable for high-precision and high-frequency applications in both analog input and output pins.

IV. Experimental Results

This design has been practically fabricated in a 0.35-μm silicide CMOS process with an operational amplifier as its input circuit. Both the inverting and non-inverting input pins are protected by the proposed analog ESD protection circuit. The silicide-blocked mask is also used on the device Mn1, Mp1, and Mn3 to improve their ESD robustness.

A. ESD Test Results

The HBM (human-body model) and MM (machine model) ESD testing results are summarized in Table I, which includes the analog pin-to-pin ESD stress. As shown in Table I, the proposed analog ESD protection circuit can successfully provide analog input pins with an HBM ESD level of above 6000V in each ESD-stress condition but only has a much smaller input capacitance. After the HBM 6500-V pin-to-pin ESD stress, the damage location is founded on the Mn3 device. This verifies the protection effectiveness of the proposed analog ESD protection circuit, especially in the analog pin-to-pin ESD stress.

The conventional ESD protection design in Fig.2 with an ggNMOS of 480/0.5 (μm/μm) for analog input pin is also fabricated in the same testchip as a reference. The HBM PS-mode ESD level of the design in Fig.2 is about 3kV, but its analog pin-to-pin HBM ESD level is below 500V. The pin-to-pin ESD damage location is founded on the poly gate of the input stage in the operational amplifier circuit. So, the conventional ESD protection design can not protect the thinner gate oxide of the differential input stage during the pin-to-pin ESD stress.

B. Turn-on Verification

To verify the turn-on efficiency of the proposed analog ESD protection circuit during the pin-to-pin ESD stress, a square-type voltage pulse generated from a pulse generator is applied to the inverting pin of an operational amplifier, whereas the non-inverting pin of the operational amplifier is relatively grounded and both the VDDA and VSSA pins are floating. The experimental setup to verify the turn-on efficiency in the positive and negative pin-to-pin ESD-stress conditions are shown in Fig.12(a) and 12(b), respectively.

The measured voltage waveforms in the positive pin-to-pin ESD-stress condition are shown in Fig.13(a) and 13(b).

The voltage waveform in Fig.13(a) is the original voltage pulse generated from the *hp* 8118A pulse generator with a pulse height of 8V and a pulse width of 200ns. While this voltage pulse is applied to the analog pin as shown in Fig.12(a), it is clamped by the proposed analog ESD protection circuit and the degraded voltage waveform is shown in Fig.13(b). The voltage waveforms in the negative pin-to-pin ESD-stress condition are also measured and shown in Fig. 14(a) and 14(b). From Fig.13(b) and Fig.14(b), the voltage pulses are actually clamped by the proposed analog ESD protection circuit during the pin-to-pin ESD-stress conditions. This has practically verified the turn-on effectiveness of the proposed analog ESD protection circuit.

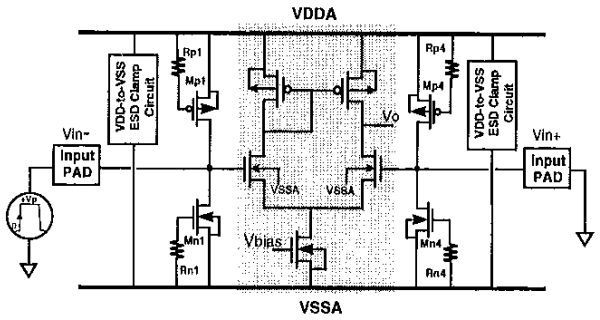
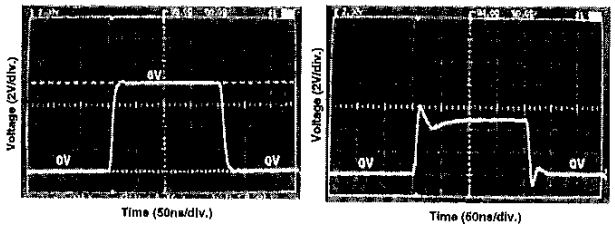


Fig.12 The experimental setup to verify the turn-on efficiency of the proposed ESD protection circuit for analog input pins during (a) the positive, and (b) the negative, pin-to-pin ESD-stress conditions.

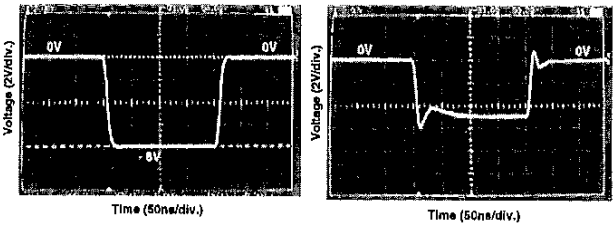
V. CONCLUSION

An analog ESD protection circuit with a very low and nearly-constant input capacitance, high ESD level, but no series resistance, has been successfully designed and verified in a 0.35-μm silicided CMOS process. This design can be applied to protect both the analog input and output pins for current-mode, RF, or high-resolution applications. This design has been practically applied in some IC products, such as the cable modem IC, data communication IC, video graphic IC, network IC, chip set IC, DVD IC, and so on, which had been manufactured by tsmc in the 0.35-μm or 0.25-μm CMOS processes.



(a) (b)

Fig.13 (a) The measured voltage waveform of the original 8-V voltage pulse generated from a pulse generator, (b) the degraded voltage waveform when the 8-V voltage pulse is applied to the inverting analog input pin in the pin-to-pin stress condition as shown in Fig.12(a).



(a) (b)

Fig.14 (a) The measured voltage waveform of the original negative (-8V) voltage pulse generated from a pulse generator, (b) the degraded voltage waveform when the voltage pulse is applied to the inverting analog input pin in the pin-to-pin stress condition as shown in Fig.12(b).

ACKNOWLEDGEMENT

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