Hardware / Firmware Co-Design in an 8-Bits Microcontroller to Solve the System-Level ESD Issue on Keyboard

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Abstract -- A hardware / firmware co-design solution in an 8-bits microcontroller has been proposed to practically fix the system-level ESD (electrostatic discharge) issue on the keyboard products. By including the especial ESD sensors and an additional ESD flag into the chip, the fast electrical transient due to the system-level ESD zapping on the keyboard can be detected. The firmware stored in the ROM of the 8-bits microcontroller is designed to automatically check the ESD flag to monitor the abnormal conditions in system operations. If the keyboard is upset or locked up by a system-level ESD transient, the microcontroller can be quickly recovered to a known and stable state. The 8-bits microcontroller with such a hardware / firmware co-design solution has been fabricated in a 0.45-μm CMOS process. The system-level ESD susceptibility of the keyboard with this 8-bits microcontroller has been improved from the original 2kV (4kV) to become greater than 8kV (15kV) in the contact-discharge (air-discharge) ESD zapping.

1. Introduction

An 8-bits microcontroller, compatible to the *Intel* 8051 [1], has been used as the main microcontroller in the keyboard products for general personal computer (PC) applications. Such a keyboard microcontroller IC has to face the component-level [2]-[5] and system-level [6]-[10] ESD issues.

In the component phase, the mircocontroller IC without any power supply bias is sensitive to ESD stress. Therefore, the on-chip ESD protection circuits must be designed and placed around the pads of IC's to clamp ESD voltages without causing permanent damage in the IC's. The typical component-level ESD specifications for commercial IC products are 2-kV in the human-body-model (HBM) [3], 200-V in the machine-model (MM) [4], and 1-kV in the charged-device-model (CDM) [5] ESD tests. The design of on-chip ESD protection circuits in a microcontroller IC to sustain the HBM (CDM) ESD stresses of greater than 5kV (1.5kV) is described in Section 2.

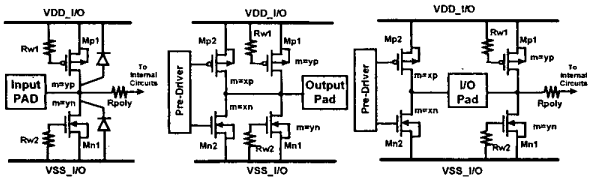
Besides the component-level ESD issue, the keyboard including the 8-bits microcontroller has to be tested in the system-level ESD events to verify the system-level EMC (electromagnetic compatibility) susceptibility [6]-[10]. In the test standard of IEC 801-2 [10], two test methods have been specified to discharge the ESD energy, which are called as the air-discharge method and the contact-discharge method. The keyboard in PC applications is required to sustain both the 4-kV contact-discharge ESD zap and the 8-kV air-discharge ESD zap without any keyboard upset or operating errors. Even if the 8-bits microcontroller can sustain a component-level HBM ESD stress of greater than 5kV, the upset and operating errors in the keyboard still happened in the system-level ESD zapping with only a 2-kV ESD voltage in the contact-discharge testing method.

In this paper, a hardware / firmware co-design solution in an 8-bits microcontroller is proposed to fix the system-level ESD issue on the keyboard products without adding extra discrete components to absorb or bypass the electrical transient on the system boards.

2. Component-Level ESD Protection

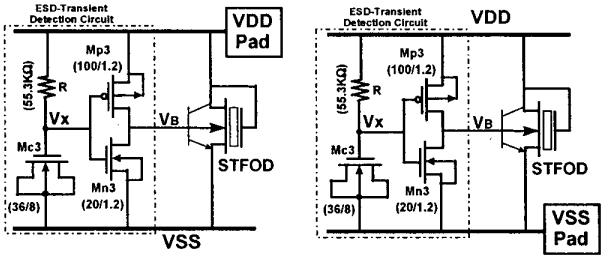
To avoid the microcontroller IC damaged by ESD energy in the component phase, the on-chip ESD protection circuits are included into the chip of the

microcontroller IC. To protect this 8-bits microcontroller with a shrunk die size fabricated in a 0.45-μm CMOS technology, the whole-chip ESD protection design [11]-[12] with multiple area-efficient VDD-to-VSS ESD clamp circuits [13]-[14] is used to protect this microcontroller IC.



(a) (b) (c)

Fig.1 The schematic circuit diagrams of the (a) input, (b) output, and (c) bi-directional I/O cells in the 8-bits microcontroller.



(a) (b)

Fig.2 The schematic circuit diagrams of (a) VDD cell, and (b) VSS cell, with area-efficient VDD-to-VSS ESD clamp circuits.

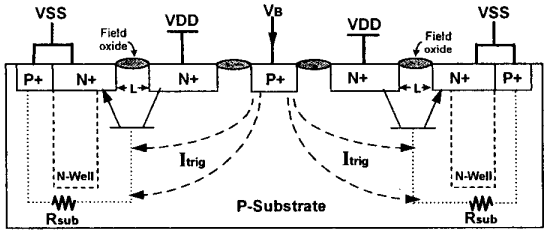
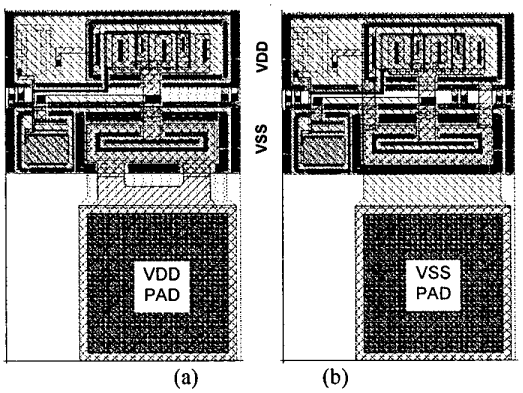


Fig.3 The device structure of the substrate-triggering field-oxide device (STFOD) realized in a p-substrate CMOS process [13]-[14].



(a) (b)

Fig.4 Layout examples of (a) VDD, and (b) VSS, cells in the 8-bits microcontroller with area-efficient VDD-to-VSS ESD clamp circuits.

The input, output, and bi-directional I/O cells in the 8-bits microcontroller are drawn in Fig.1. In the input cell, a poly resistor (Rpoly) of ~200Ω is connected between the pad and the internal circuits to avoid direct overstress on the gate oxide of internal circuits. To improve ESD robustness of the I/O cells and to achieve whole-chip ESD protection, VDD-to-VSS ESD clamp circuits must be added in the chip [12]. Therefore, an area-efficient VDD-to-VSS ESD clamp circuit [13]-[14] is added into every power pad of this 8-bits microcontroller. The VDD and VSS cells with area-efficient VDD-to-VSS ESD clamp circuits are shown in Fig.2, where a *RC*-based ESD-detection circuit is used to turn on a substrate-triggered field-oxide device (STFOD). The device structure of the STFOD in a p-substrate CMOS process is drawn in Fig.3. The layouts of VDD and VSS power cells in the 8-bits microcontroller are shown in Fig.4. By using such a whole-chip ESD protection design, this 8-bits microcontroller fabricated in a 0.45-μm CMOS process can sustain a component-level HBM ESD robustness of greater than 5kV.

Due to the thinner gate-oxide thickness in deep-submicron CMOS processes, the input stages of CMOS IC's are more sensitive to CDM ESD damages [5], [15]-[16]. The schematic diagram to show negative CDM electrostatic charges stored in a p-substrate CMOS IC and discharged through an input pin is illustrated in Fig.5, where the CDM ESD current discharging path is indicated by a dashed line. When the input pin of a charged IC touches ground, the electrostatic charges in the charged IC are conducted from the IC body to the external ground and therefore generate the discharging current.

The input ESD protection circuit located around the input pad can effectively clamp HBM ESD voltage across the gate oxide of internal input stages, but such an input ESD protection circuit can not protect the gate oxide of input stages in CDM ESD events, even if there is a series resistance connected between the input pad and the internal input stages [16]. To protect such a CDM ESD stress across the gate oxide of input stage, the additional ESD clamp devices are added into the internal input stage, as shown in Fig.6. The additional Mn1b and Mp1a devices are used to locally clamp ESD voltage across the gate oxide of the input stage. The VSS (VDD) power line connected to Mn1b (Mp1a) must be the same VSS (VDD) power line that is connected to Mn5 (Mp5) of the internal input stage. The Mn1b and Mp1a are drawn as close as possible to the gate oxide of Mn5 and Mp5 in cell layout of the internal input

stage. The typical cell layout of such an input stage with CDM ESD protection is shown in Fig.7, where the drains of Mn1b and Mp1a have a suitable layout spacing from the drain contact to their poly gates to avoid damage in HBM ESD stresses.

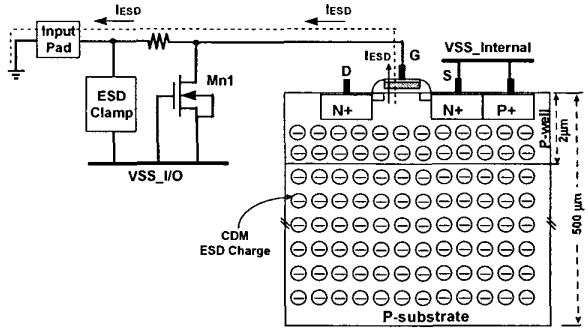


Fig.5 Schematic diagram to show the negative CDM ESD charges stored in a CMOS IC with a p-type substrate.

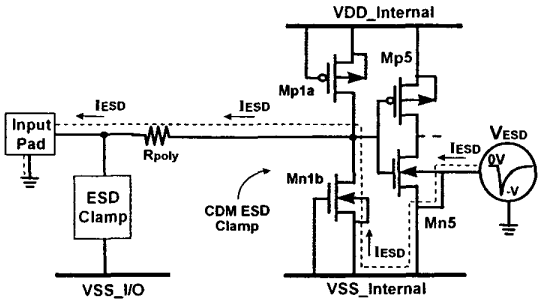


Fig.6 ESD protection design for the input pin to clamp CDM ESD stress across the gate oxide of input stage.

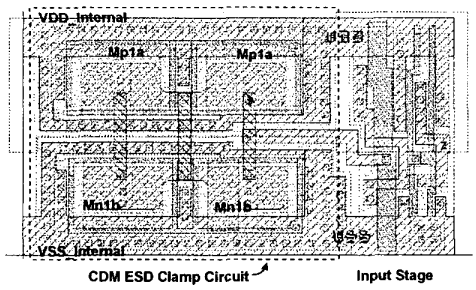


Fig.7 The layout example of an input stage with CDM ESD clamp devices (Mn1b and Mp1a).

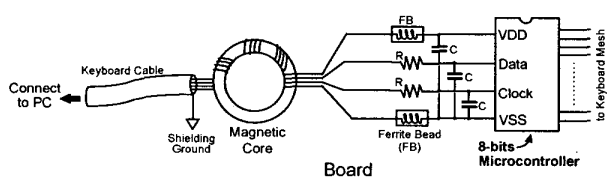


Fig.8 The traditional solution to overcome the system-level ESD issue in the keyboard by adding extra discrete components to absorb or bypass the electrical transient.

By using such a CDM protection design, the 8-bits microcontroller can sustain the CDM ESD stress greater than 1.5kV in the socketed CDM tester.

3. Electrical Transient During System-Level ESD Test

With a high component-level ESD robustness (HBM>5kV, CDM>1.5kV), the 8-bits microcontroller was not yet returned by the field customers in keyboard assembly due to ESD damage. Even if the 8-bits microcontroller can sustain the component-level HBM (CDM) ESD stress of greater than 5kV (1.5kV), the upset or operating errors in keyboard have been found in the system-level ESD stress with a only 2-kV ESD voltage in the contact-discharge testing method [10].

To meet this system-level ESD specification, some discrete components (such as the magnetic core, ferrite beads, and *RC* low-pass circuits) are added into the keyboard circuit board to absorb or bypass the electrical transient due to system-level ESD test, which are shown in Fig.8. Because the microcontroller fabricated in the scaled-down CMOS process with a much smaller die size is more sensitive to electrical transient, more or larger magnetic cores and ferrite beads are used on the keyboard circuit board to restrain the electrical transient generating from the system-level ESD test. But, such additional discrete components substantially increase the total cost of a keyboard. Therefore, a microcontroller with robust system-level ESD susceptibility, but without adding expensive additional discrete components on the circuit board, is strongly requested by the keyboard manufactories.

To investigate the electrical transient on the microcontroller during the system-level ESD test on the keyboard, the voltage waveforms on both the VDD and VSS pins of the microcontroller IC in keyboard are simultaneously monitored by an *HP* oscilloscope with a sampling rate of 2Gs/s. The ESD simulator used to generate the system-level ESD pulse in this experimental setup is the *MiniZap* ESD gun produced by the *Keytek Instrument Corp.*. To test the system-level ESD susceptibility of keyboard, the keyboard is connected to an *IBM* PC to verify whether the keyboard has any operating error or upset. Two test points have to be hit by the ESD gun to investigate the EMC/ESD susceptibility of a keyboard in the PC system [10]. One is the table with a metal plane where the keyboard and PC is on, as shown in

Fig.9. The other point is the backside of the PC case, as shown in Fig.10, where the keyboard cable is connected to.

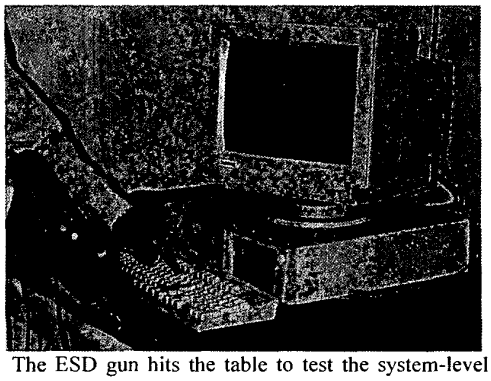


Fig.9 The ESD gun hits the table to test the system-level ESD susceptibility of a keyboard in the PC system.

Fig.10 The ESD gun hits the backside of the PC case to test the system-level ESD susceptibility of a keyboard in the PC system.

The measured voltage transition on the VDD and VSS pins of the microcontroller in keyboard is shown in Figs. 11 ~ 14. In Fig.11 (Fig.12), it shows the measured VDD and VSS voltage waveforms, when the ESD gun with an ESD voltage of positive 1000V (negative 3000V) hits the table by the contact-discharge test method. In Fig.13 (Fig.14), it shows the measured VDD and VSS voltage waveforms, when the ESD gun with an ESD voltage of positive 500V (negative 2000V) hits the backside of the PC case by the contact-discharge test method.

The corresponding VDD-to-VSS voltage waveforms during such system-level ESD tests are shown in Figs.15 ~ 18. In Fig.15 (Fig.16), it shows the voltage difference between the VDD and VSS power pins of the microcontroller in the keyboard, when the ESD gun with an ESD voltage of positive or negative 1000V (3000V) hits the table. In Fig.17 (Fig.18), it shows the voltage difference between the VDD and VSS power pins of the microcontroller in the keyboard, when the ESD gun with an ESD voltage of positive or negative 500V (2000V) hits the backside of the PC case. The dependence of the maximum positive and negative voltage peaks in the corresponding VDD-to-VSS voltage waveforms on the ESD zap voltage during the system-level ESD zapping on the table or the backside of a PC case by the contact-discharge test method is shown in Fig.19(a) and 19(b). The larger ESD zap voltage leads to a higher voltage peak on the VDD-to-VSS voltage waveforms.

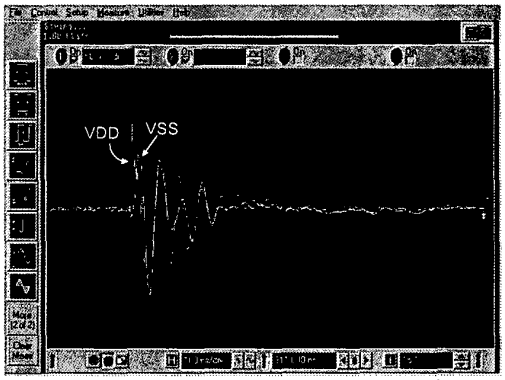


Fig.11 The measured VDD and VSS voltage waveforms on the microcontroller in a keyboard when the ESD gun with a positive 1000-V ESD voltage hits the table.

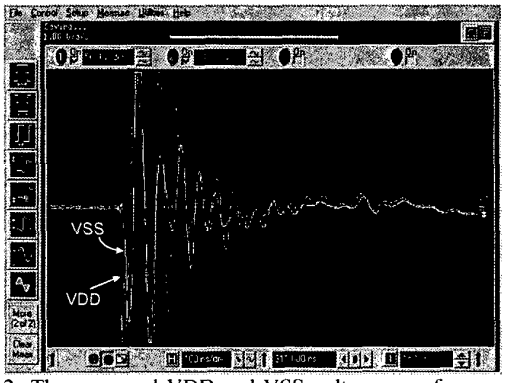


Fig.12 The measured VDD and VSS voltage waveforms on the microcontroller in a keyboard when the ESD gun with a negative 3000-V ESD voltage hits the table.

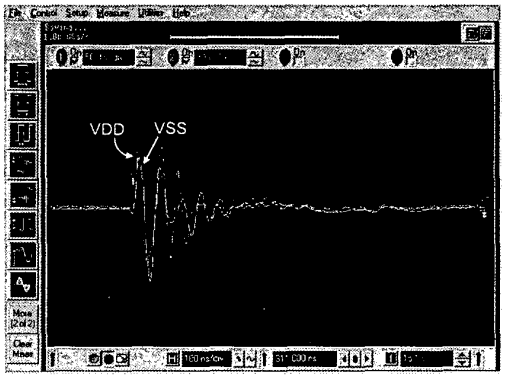


Fig.13 The measured VDD and VSS voltage waveforms on the microcontroller in a keyboard when the ESD gun with a positive 500-V ESD voltage hits the backside of the PC case.

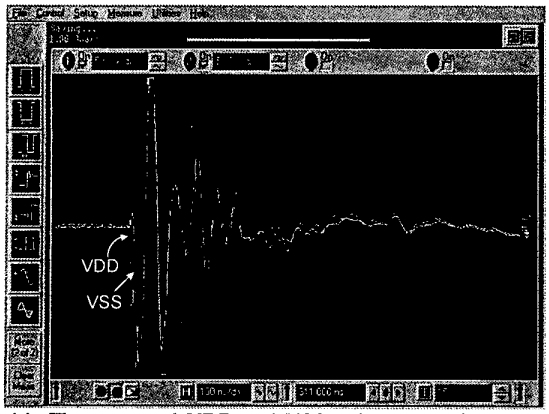
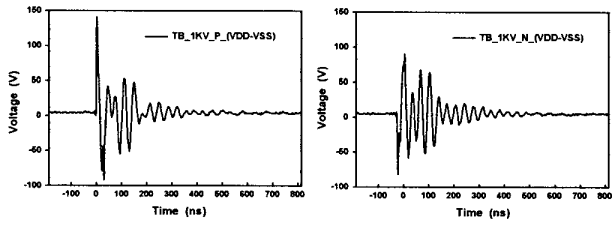
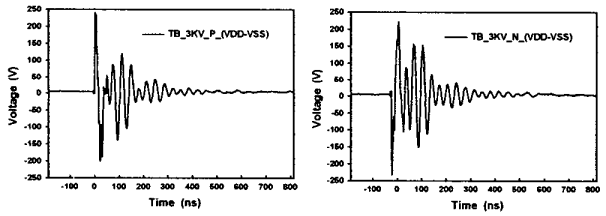


Fig.14 The measured VDD and VSS voltage waveforms on the microcontroller in a keyboard when the ESD gun with a negative 2000-V ESD voltage hits the backside of the PC case.



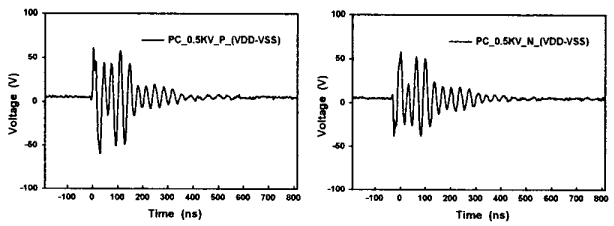
(a) (b)

Fig.15 The corresponding VDD-to-VSS voltage waveforms on the microcontroller in the keyboard during the system-level ESD test, when the ESD gun with a (a) 1000V, and (b) -1000V, ESD voltage hits the table.



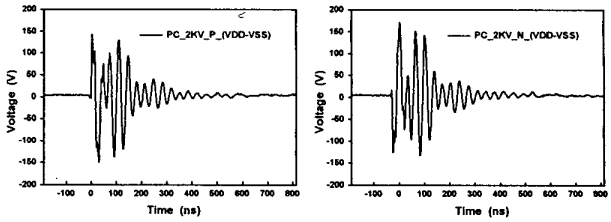
(a) (b)

Fig.16 The corresponding VDD-to-VSS voltage waveforms on the microcontroller in the keyboard during the system-level ESD test, when the ESD gun with a (a) 3000V, and (b) -3000V, ESD voltage hits the table.



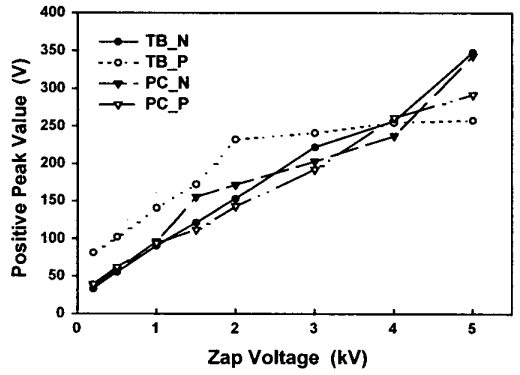
(a) (b)

Fig.17 The corresponding VDD-to-VSS voltage waveforms on the microcontroller in the keyboard during the system-level ESD test, when the ESD gun with a (a) 500V, and (b) -500V, ESD voltage hits the backside of the PC case.

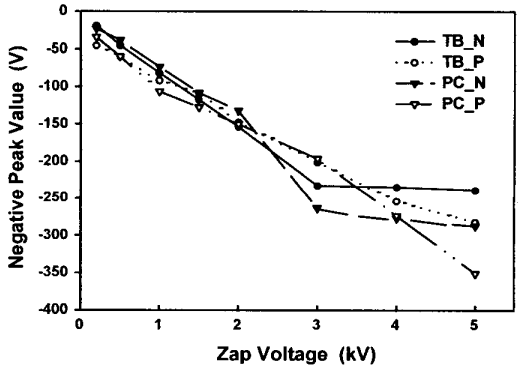


(a) (b)

Fig.18 The corresponding VDD-to-VSS voltage waveforms on the microcontroller in the keyboard during the system-level ESD test, when the ESD gun with a (a) 2000V, and (b) -2000V, ESD voltage hits the backside of the PC case.



(a)



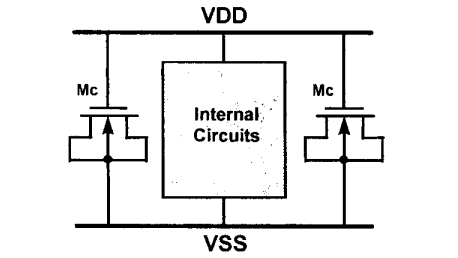
(b)

Fig.19 The dependence of (a) the positive, and (b) the negative, largest voltage peak in the VDD-to-VSS voltage waveforms on the ESD zap voltage during the system-level ESD tests by the contact-discharge method.

When such a high-voltage-level fast transient occurs on the VDD and VSS power pins, the logic states stored in the counters, registers, memory, or flip flops in the microcontroller are totally destroyed by the fast system-level electrical transient. Therefore, the program instructions in keyboard may lock-up in an infinite loop from which it can not escape, even if the watchdog timer has been included in the chip. This causes the keyboard to be upset or frozen after the system-level ESD zapping. Such a frozen keyboard can be recovered if the hardware reset is

manually restarted again. But such a manual restart is not acceptable for the keyboard products certified by the CE mark.

To bypass such a fast electrical transient, the on-chip decoupling capacitor realized by an NMOS device was added between the VDD and VSS power lines of the 8-bits mircocontroller [17]. The circuit and layout of this decoupling NMOS capacitor are shown in Fig.20(a) and 20(b). Four decoupling NMOS capacitors are placed at the four corners of the chip layout of the 8-bits mircocontroller IC, where each decoupling NMOS capacitor has a device dimension (W/L) of 2100μm/8μm. However, this 8-bits mircocontroller with on-chip decoupling capacitors in the keyboard is still upset by the system-level ESD zapping with a contact-discharge ESD voltage of 2 ~ 3 kV. Therefore, the discrete components shown in Fig.8 and more complex redesign on the board layout have to be added into the keyboard circuit board to absorb or bypass the electrical transient. If the keyboard is required to sustain a much higher system-level ESD zapping, more expensive discrete components must be used but the keyboard may still upset in some ESD testing conditions.



(a)

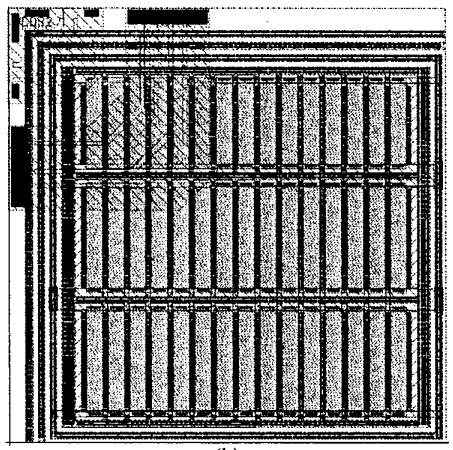

(b)

Fig.20 (a) The on-chip decoupling NMOS capacitor. (b) Layout of the decoupling NMOS for placing at the corners of the chip layout of the 8-bits microcontroller IC.

4. Hardware Design with On-Chip ESD Sensors

To avoid the keyboard upset or frozen by the system-level ESD zapping, the microcontroller should have an auto-detection function to detect such a system-level electrical transient. If the fast system-level electrical transient is detected in the IC, the microcontroller can automatically reset itself and restore gracefully to a known and stable state. To do this, the firmware must be regularly checking for abnormal conditions. The most effective method to help firmware check is to use an external hardware timer, such as the retriggerable monostable multivibrator [6]. But, it significantly increases the total cost of the keyboard products. Therefore, an effective on-chip ESD sensor is proposed in this work to detect the system-level electrical transient.

The circuit diagram of the on-chip ESD sensor is shown in Fig.21, where two latch logic gates are used as the ESD sensors to detect the system-level electrical transient. The NMOS in the inverters of the sensor_1 in Fig.21 is designed with a larger W/L ratio than that of the PMOS to make the latch easily locking at logic 0. On the contrary, the PMOS in the inverters of the sensor_2 in Fig.21 is designed with a larger W/L ratio than that of the NMOS to make the latch easily locking at logic 1. To enhance the sensitivity of the on-chip ESD sensor to electrical transient, some coupling capacitors can be added between the latch nodes and the VDD or VSS power lines. By using such a simple design, the on-chip sensor can really detect the system-level electrical transient in the microcontroller.

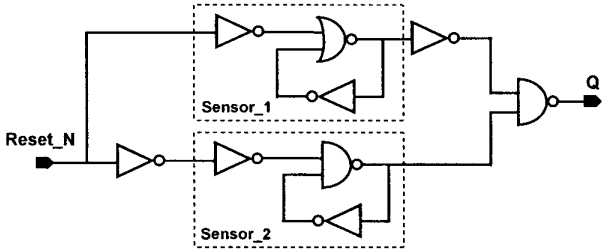


Fig.21 The sensor circuit used to detect the electrical transient on the VDD and VSS power lines in the microcontroller during the system-level ESD tests. Multiple sensors are randomly placed into the chip layout of the microcontroller IC.

The HSPICE simulated results are shown in Figs. 22 and 23. In Fig.22, the VDD voltage is originally kept at 5V with a relatively stable VSS of 0V, but some undershooting glitches from the system-level

electrical transient are coupled to the VDD. The first (second) glitch on the VDD voltage waveform in Fig.22 has a rise time/fall time of 1ns (10ns) and an undershooting voltage level of 0V, whereas the sensor output Q still maintains at logic 0. The third (fourth) glitch on the VDD voltage waveform in Fig.22 has a rise time/fall time of 1ns (10ns) and an undershooting voltage level of -1.2V, whereas the sensor output Q changes its state from the logic 0 to logic 1.

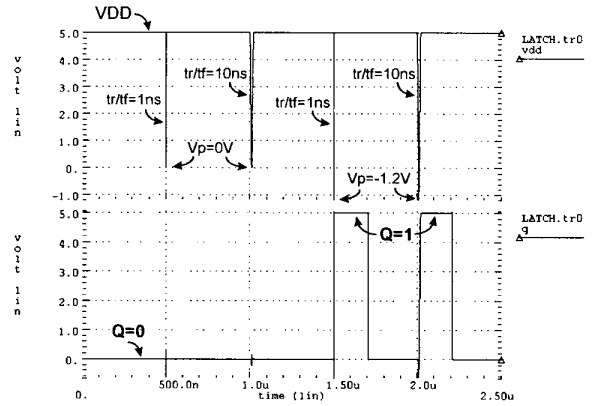


Fig.22 HSPICE simulated results on the output Q of the sensor circuit to be changed state to logic 1 when undershooting voltage glitches on VDD drop to -1.2V, whereas the VSS is biased at 0V.

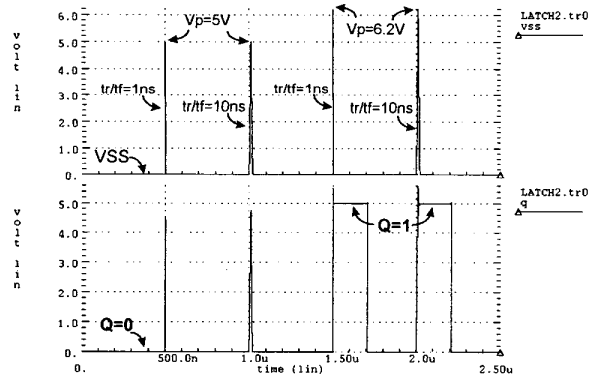


Fig.23 HSPICE simulated results to show the output Q of the sensor circuit to be changed state to logic 1 when the overshooting voltage glitches on the VSS rise up to 6.2V, whereas the VDD is biased at 5V.

In Fig.23, the VSS voltage is originally kept at 0V with a relatively stable VDD of 5V, but some overshooting glitches from the system-level electrical transient are coupled to the VSS. The first (second) glitch on the VSS voltage waveform in Fig.23 has a rise time/fall time of 1ns (10ns) and an overshooting voltage level of 5V, whereas the sensor output Q still maintains at logic 0 after the VSS overshooting transition. The third (fourth) glitch on the VSS voltage waveform in Fig.23 has a rise time/fall time of 1ns (10ns) and an overshooting voltage level of is 6.2V, whereas the sensor output Q changes its state from the logic 0 to logic 1. The voltage detection level of the ESD sensor on the undershooting or overshooting transient peaks can be adjusted by changing the device W/L ratios in the latch logic gates or the coupling capacitors between the latch nodes and the VDD / VSS power lines. The HSPICE simulation can be used to fine tune the device sizes in the sensors to detect different overshooting or undershooting voltage levels in the microcontroller coupled from the system-level electrical transient.

5. Firmware Design with the ESD Flag

With multiple on-chip ESD sensors included into the microcontroller at different layout locations, the outputs from the multiple ESD sensors are collected together by an OR gate and then stored in an ESD flag which is formed by a typical D-type flip flop. With the additional ESD flag, the detection results from the on-chip ESD sensors can be temporarily stored for firmware check. When the state of Q=1 happens in one of the ESD sensors, it will simultaneously re-start the hardware reset and recover procedures in the microcontroller to avoid the keyboard upset or operating errors.

The firmware design with the additional ESD flag is illustrated in Fig.24. As shown in the flowchart, the microcontroller is first started by the hardware reset through the power-on reset circuit when the keyboard in the PC system is powered on. The states in the ESD sensors and the ESD flag are initially cleared to logic 0 by the power-on reset. The reset procedure is executed through the normal firmware reset procedure when the ESD flag has a state of logic 0. Then, the keyboard enters the normal operating condition to work with the PC system.

But, when a system-level ESD event occurs to the keyboard, the multiple ESD sensors in the microcontroller IC in the keyboard can detect the fast electrical transient to change the output states to Q=1. When the state of Q=1 occurs, the ESD flag is re-stored at logic 1, as well as the hardware reset procedure is re-started again. The reset procedure is executed again with the firmware to check the logic state in the ESD flag. At this time, the state stored in the ESD flag is logic 1, therefore the firmware

executes the recover procedure to recover all the keyboard functions to a known and stable state as soon as possible. The keyboard can be recovered within only few milli-second to get a nearly real-time response for a person to key-in data into the PC. After the reset and recover procedures, the states in the ESD sensors and the ESD flag are re-set to logic 0 again for detecting the next ESD events. The firmware stored in the ROM of the 8-bits microcontroller must be modified with this additional function to implement such reset and recover procedures.

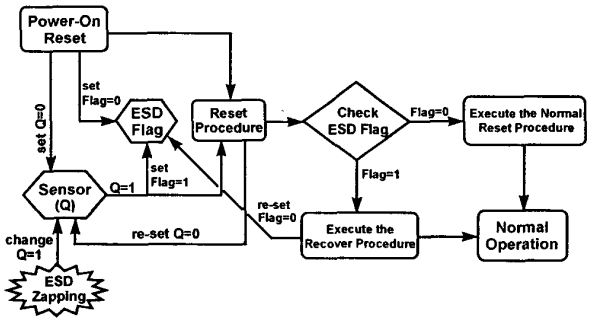


Fig.24 The firmware flowchart to reset or recover the microcontroller if the ESD sensor detects the electrical transient in the keyboard during the system-level ESD stress.

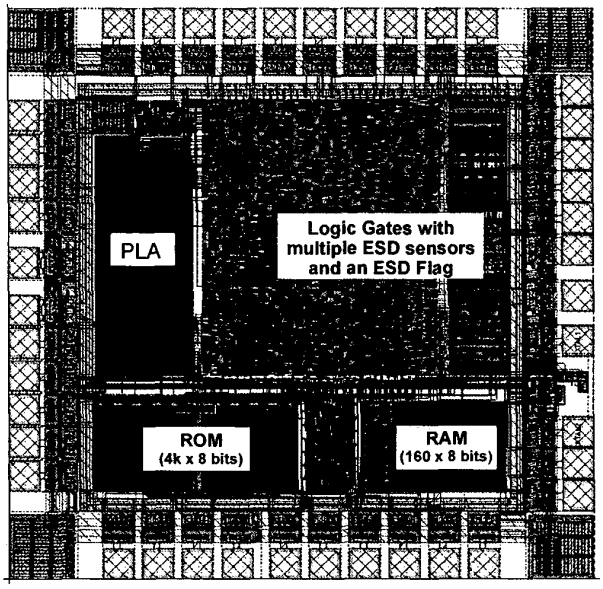


Fig.25 The layout of the 8-bits microcontroller. The multiple ESD sensors to detect the system-level electrical transient are randomly placed in the chip with the logic blocks synthesized by the standard cells.

6. Experimental Results

The whole-chip layout of the 8-bits microcontroller IC with multiple ESD sensors and an ESD flag is shown in Fig.25. The die size of this microcontroller is only about 1800×1800 μm^2, which is fabricated in a 0.45-μm CMOS process with three metal layers. The picture of the keyboard circuit board included this 8-bits microcontroller is shown in Fig.26, where no extra discrete components such as the magnetic core, ferrite bead, or low-pass *RC* filter are added on the circuit board. On the circuit board shown in Fig.26, there are three capacitors and one resistor. The resistor is used to adjust the on-chip oscillator frequency for different keyboard applications. One capacitor is used with the on-chip power-on reset circuit to initiate the power-on reset function in the microcontroller. The other two capacitors of 10μF and 0.01μF are generally placed across VDD and VSS of a circuit board to provide a stable power supply for the microcontroller in normal system operations.

By only using the proposed hardware and firmware co-design solution in the microcontroller IC, the system-level ESD susceptibility of the keyboard products with this 8-bits microcontroller has been improved from the original 2kV (4kV) to become greater than 8kV (15kV) in the contact-discharge (air-discharge) ESD test method, in spite of the ESD zapping location being on the table or at the PC case.

Moreover, this design has been also applied to overcome the upset issue in keyboards due to the electrical fast transient (EFT) test [18]. The keyboard with this 8-bits microcontroller can pass the EFT test with a voltage peak of 2 kV and a repetition rate of 5 kHz on the AC power supply port.

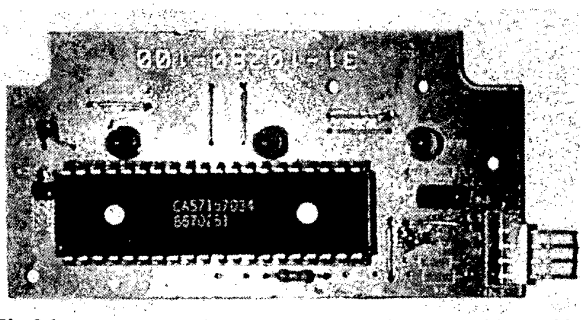


Fig.26 The picture of the keyboard circuit board with a 8-bits microcontroller, where only three capacitors and one resistor are included on the board. Without adding any magnetic core, ferrite bead, or low-pass circuit, this keyboard can sustain the system-level ESD stresses with a zapping voltage of greater than 8kV (15kV) in the contact-discharge (air-discharge) testing method.

7. Conclusion

A hardware and firmware co-design on an 8-bits microcontroller has been demonstrated in this paper to solve the system-level ESD issue in the keyboard products. The fast transient voltage waveforms on the VDD and VSS pins of the microcontroller in the keyboard have been practically measured during the ESD zapping. The on-chip ESD sensors are therefore designed to detect the electrical transient from the system-level ESD zapping, and the additional ESD flag is included into the microcontroller for firmware check to recover the keyboard after the ESD zapping. Without adding any additional discrete component on the keyboard circuit board, the system-level ESD susceptibility of the keyboard has been successfully improved from the original 2kV (4kV) to become greater than 8kV (15kV) in the contact-discharge (air-discharge) ESD zapping. This microcontroller is now in the mass-production phase and widely used by the keyboard manufactories.

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