

Layout Design on Bond Pads to Improve the Firmness of Bond Wire in Packaged IC Products

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Abstract

During the manufacture of IC products, the break of bond wires or the peeling of bond pads occurs frequently and thus results in the open circuit phenomenon in the IC's. There are several methods proposed to overcome this problem, but additional special process flows are desired for all of these previous methods. This paper presents a layout design method to improve the bond wire reliability in a standard CMOS process. By changing the layout patterns on the bond pads, the firmness of bond wires on the bond pads can be improved. One set of layout patterns on the bond pads has been designed and fabricated in a $0.6\mu\text{m}$ 1P3M CMOS process for the ball shear test and the wire pull test. By implementing the effective layout designs in IC products, the bond wire reliability can be obviously improved in a standard CMOS process.

Introduction

The bond pad peeling and the heel break of bond wires have been recognized as the two main issues of low bonding reliability. There are two general methods to qualify the bond pad reliability [1]. One is the wire pull test via a hook pulling the bond wire, as shown in Fig. 1(a). The other is the ball shear test with a horizontal force in parallel with the silicon die, as shown in Fig. 1(b). To increase the bonding reliability, one method is to use specific materials for replacement of the original one in the process before bonding. The possible replaced materials are oxide [2], metal [2], inter-layer material [3], dielectric layer [4]-[5], and also the top surface material on the bond pads [6]. Different device structures had been also used to improve the bond wire firmness. The structural reinforcement of inter-metal dielectrics was developed by Texas Instruments to eliminate the bond pad damage [7]. A multi-metal layer notched surface, as shown in Fig. 2, was presented by Micron Technology to increase the adhesion of the bond pad [8]. It presents a pad structure with multi-metal layers on the dielectric layer in order to form a paling surface for improving the firmness of bond wires. Although it does improve the bond wire reliability, it needs to modify the process flow to implement the multi-metal layers.

Moreover, the paling dielectric layer used directly to reduce the stress of pad bonding is also reported by Motorola, TSMC (Taiwan Semiconductor Manufacturing Company) and UMC (United Microelectronics Corporation) [9]-[11] to rise up the bonding yield. Also, the control of bonding stress is effective for the reliability issue of bond pads [12]-[13]. To get a better bonding reliability, using a wider bond pitch is another way [14], but this often increases the chip sizes of IC products.

This paper presents a layout design method on bond pad to improve the bonding reliability without extra process

or material modifications. By changing the layout patterns of the metal layer beneath the bond pad, the bonding reliability of IC products can be improved in a standard CMOS process. The performances of different layout patterns have been fabricated and analyzed statistically through the measurement results.

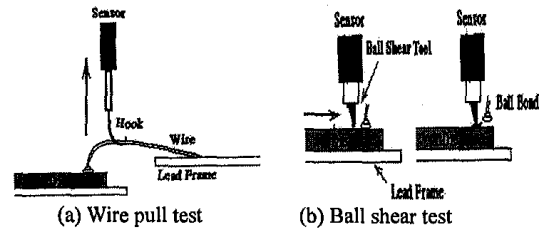


Fig.1 Two general test methods on bond wires for qualifying the reliability of bond wires [1].

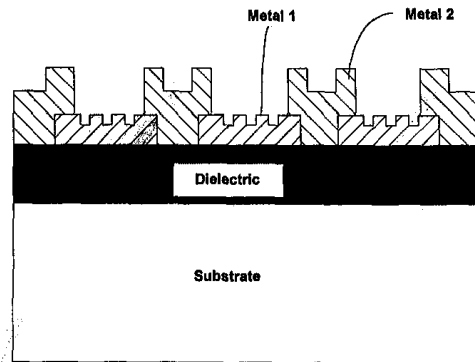


Fig.2 An example of multi-metal layer structure on the bond pad [8].

Layout Design for Increasing Bond Wire Reliability

Fig. 3 shows the cross-sectional view of the proposed layout design method by using a single-poly triple-metal CMOS process. In the conventional pad structure of this process, the layout pattern of each metal layer is one flat plate and the electrical connection between two metal layers is performed by a plurality of via plugs. In order to increase the adhesion of the bond ball on the bond pad, the surface of the top metal denoted by Metal-3 in Fig. 3 should be designed to be rough. To make the surface of the top metal rough, the metal layer denoted by Metal-2 in Fig. 3 beneath the top metal is designed with regular or irregular layout patterns except a flat plate, and the connection between Metal-3 and Metal-2 is performed by small size of via-plugs. This arrangement will cause the dielectric deposited on the Metal-2 to have an undulating surface. Thus the top metal deposited on the undulating dielectric can have a rough surface to improve the firmness of bond wires.

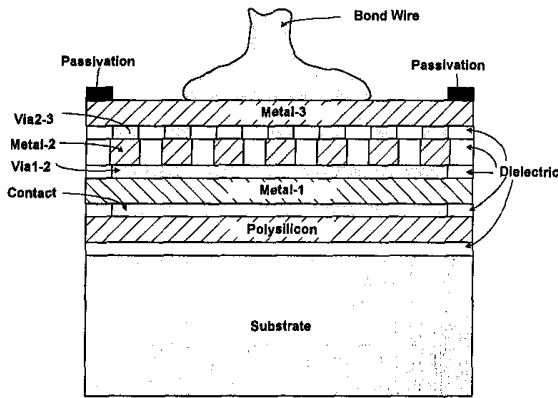


Fig.3 The cross-sectional view of the proposed layout design method by using a single-poly triple-metal CMOS process.

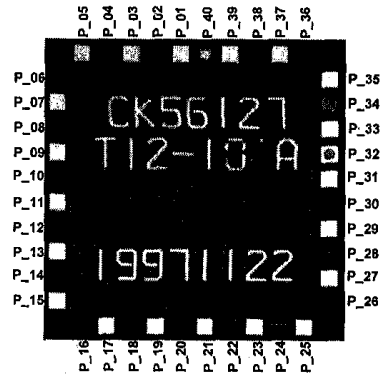


Fig.5 The photograph of the test chip. The denoted odd-number pads are with the conventional layout pattern, and the even-number pads are with the experimental layout patterns.

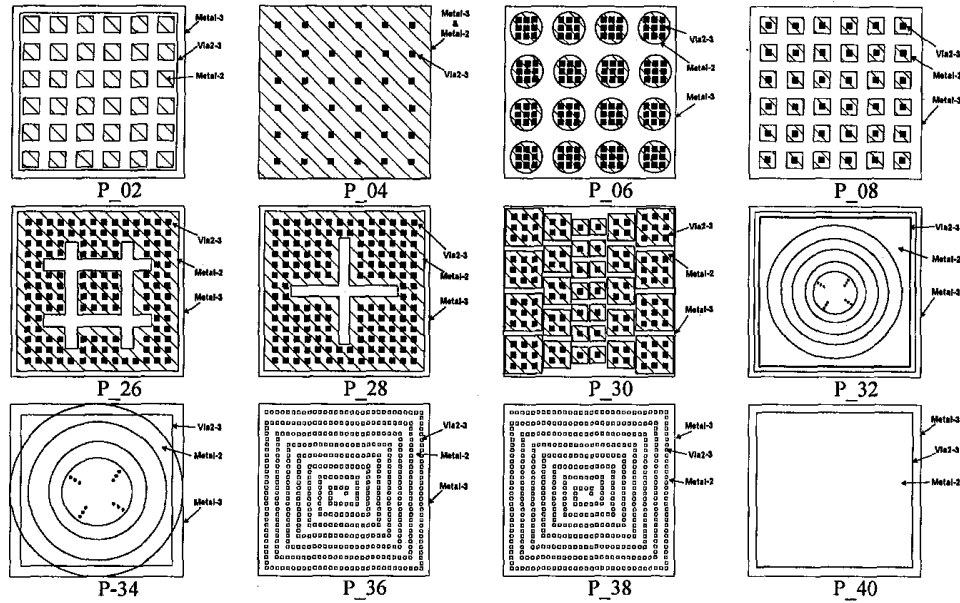


Fig.4 The designed experimental layout patterns in the test chip.

Several experimental layout patterns of the Metal-2 and Via2-3 denoted in Fig. 3 have been designed to investigate their performances. Fig. 4 shows the designed experimental layout patterns.

Experimental Results

To verify the effect of the proposed layout design method, a test chip has been fabricated by using a 0.6 μm single-poly triple-metal CMOS process. Fig. 5 shows the photograph of the fabricated test chip. The pads denoted by odd-number are with the conventional layout pattern as reference, and the pads denoted by even-number are with the experimental layout patterns shown in Fig. 5. The experimental layout patterns of P_10 to P_24 are similar to

that of P_08 except for the size of Metal-2 polygons and the number of Via2-3.

In the industrial standards, the bond wires on the pads have to stand at least 5mg of pull force and 30mg of shear force treated on them. Fig. 6 shows the measurement results of the wire pull test on the pads with the conventional layout pattern in three dies. The horizontal axis shown in Fig. 6 is the pad number denoted in Fig. 4. As shown in Fig. 6, the measured pull-off forces on the pads, which have the same conventional layout pattern but locate at different places, have a wide-range variation. Moreover, the minimum value in Fig. 6 is 5.3mg, which is only a little greater than the industrial standard of 5mg. The measurement results of the wire pull test on the pads with different experimental layout patterns are shown in Fig. 7.

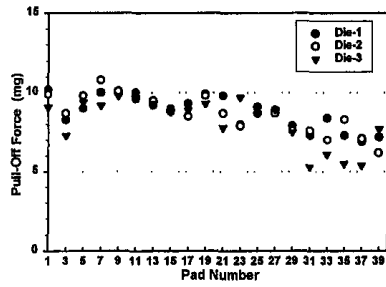


Fig.6 The experimental results of wire pull test on the pads with conventional layout pattern. In the industrial standard of this test, bond wires have to stand at least 5 mg pull-off force treated on them.

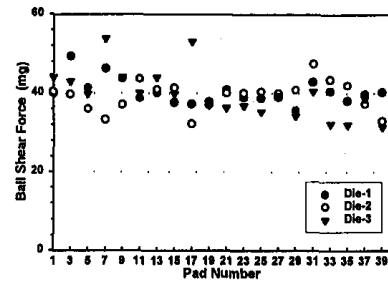


Fig.9 The experimental results of ball shear test on the pads with conventional layout pattern. In the industrial standard, the bond wires have to stand at least 30 mg pull-off force treated on them.

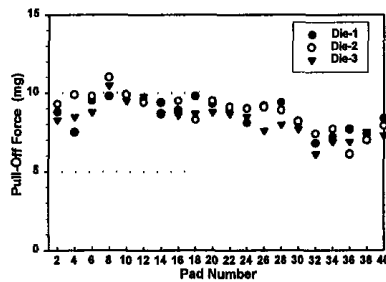


Fig.7 The experimental results of wire pull test on the pads with experimental layout patterns.

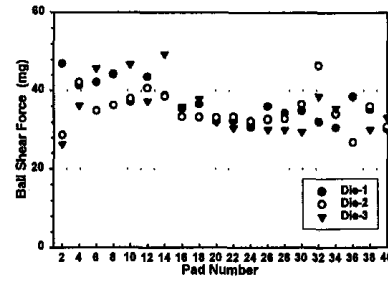


Fig.10 The experimental results of ball shear test on the pads with experimental layout patterns.

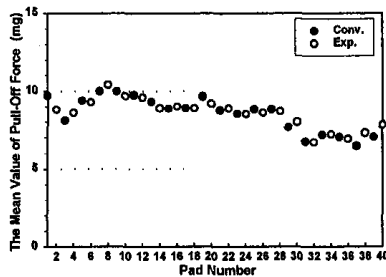


Fig.8 The comparison of the mean values of the pull-off force between the conventional and experimental layout patterns.

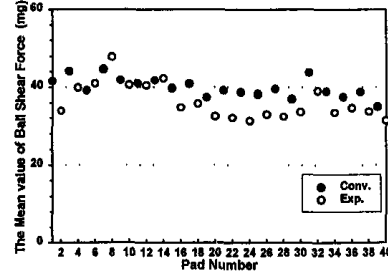


Fig.11 The comparison of the mean values of the ball shear force of the conventional and experimental layout patterns.

The minimum value in Fig. 7 is 6.1mg, which is obviously greater than that of conventional layout pattern. Fig. 8 shows the mean values of the pull-off forces measured from the three dies at each pad location. The minimum mean value of 6.7mg, in the experimental layout patterns is occurred on the pad located at P_32 denoted in Fig. 4, which is still greater than that of 6.47mg in the conventional layout pattern.

Fig. 9 shows the measurement results of the ball shear test on the pads with the conventional layout pattern. The measured minimum value of the ball shear force is 31.5mg, which is greater than the industrial standard of 30mg. The measurement results of the ball shear test on the pads with

different experimental layout patterns are shown in Fig. 10. The minimum value is 26.3mg, which is unfortunately smaller than the industrial standard. Fig. 11 shows the mean values of the ball shear forces measured from the three dies. The minimum mean value of 31.2mg in the experimental layout patterns is occurred on the pad located at P_24 denoted in Fig. 4, which is greater than the industrial standard and still smaller than that of 34.97mg in the conventional layout pattern.

From Figs. 6 to 11, it can be found that most of the experimental layout patterns have better bond wire reliability than the conventional layout pattern under the wire pull test. However, under the ball shear test, the

conventional layout pattern has better bond wire reliability than most of the experimental layout patterns. Although not every designed experimental layout pattern has better bond wire reliability than the conventional layout pattern under both of the wire pull and ball shear tests. It can be found that the experimental layout pattern of P_08 in Fig. 5 is the most effective design in this chip for both of the wire pull and ball shear tests. Fig. 12(a) shows the photograph of the pattern of P-08, which Metal-2 is shaped into pieces of small foursquare rectangular and each piece is connected to Metal-3 through one via plug. Fig. 12(b) shows the dimensions of this layout pattern.

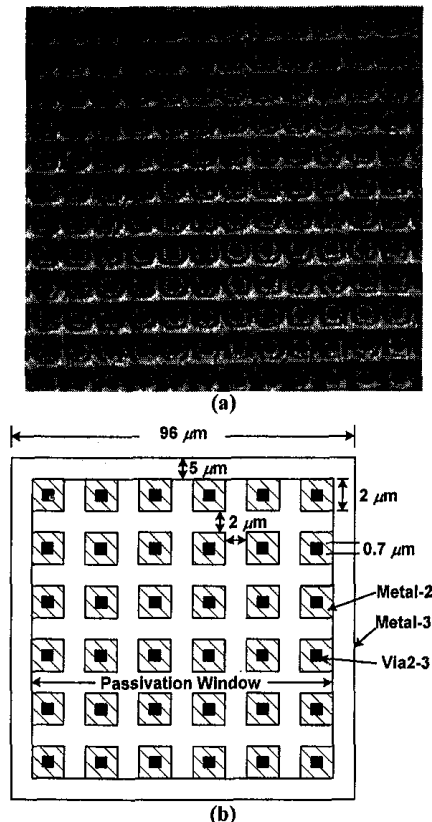


Fig.12 The (a) photograph and (b) dimensions of the pattern of P-08 shown in Fig.4.

Intuitively, the better bond-wire reliability for both of the wire pull and ball shear tests can be obtained if the layout pattern of the metal layer beneath the top bonding metal layer was designed in small pieces of polygons instead of conventional flat plate. But, the aforementioned statistical measurement results indicate that it is not valid for all designed experimental layout patterns except for the layout pattern of P_08 in Fig. 5. This indicates that the proposed layout design method is still able to increase the bond wire reliability while the layout pattern is chosen correctly.

Conclusion

In this paper, a layout design method has been proposed to increase the bond wire reliability for IC products. The metal layer beneath the top bonding metal layer is designed with regular or irregular layout patterns to make the surface of the top metal rough to increase the adhesion of the bond ball on the bond pad. Several experimental layout patterns have been designed and fabricated in a standard CMOS process. The statistical measurement results show that the proposed method can increase the bond wire reliability if the layout pattern is chosen correctly.

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