New Experimental Methodology to Extract Compact Layout Rules for Latchup Prevention in Bulk CMOS IC's

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Abstract

A new experimental methodology to find the compact layout rules on guard rings is proposed to increase latchup immunity of bulk CMOS IC's. The layout rules are extracted from the experimental testchips with the latchup sensors and different drawing spacings. A new latchup prevention design with additional internal guard rings between the I/O cells and the internal circuits is first investigated in the fabricated experimental testchips. Through detailed experimental verification including temperature effect, one set of compact layout rules has been established to save the chip size of the pad-limited CMOS IC's but still with enough latchup immunity in a 0.5-μm bulk CMOS technology.

Introduction

As more complex functions and circuits integrated into a single chip, the pin count of a CMOS USLI is often greater than 200. Especially, in the communication IC's or chip set IC's, more I/O pins are designed to provide the system applications with the desired functions. In such high-pin-count IC's, the whole chip size is decided by the pad-limited effect but no longer the core-limited effect. Therefore, the pad pitch is seriously limited to reduce the total chip size on the silicon wafer. To further reduce the pad pitch for high-pin-count CMOS IC's, the staggered (interdigitated) bond pad has been widely used in CMOS IC's to reduce the whole chip size. With the staggered bond pad design, the layout pitch for a corresponding I/O cell has been scaled down to only ~50μm. With such a narrow layout spacing, the cell height of an I/O cell including the output buffer circuit or ESD protection circuit with latchup guard rings becomes much longer. The much longer cell height of I/O cells also causes a larger whole chip size. Therefore, the compact layout rules for I/O cells to prevent latchup are highly demanded in the high-pin-count CMOS IC's.

In this paper, a new latchup prevention design with more compact layout rules to reduce the whole chip size is proposed with experimental verification in the testchips and practical IC products in a 0.5-μm CMOS technology. The new latchup test structures to define the compact layout rules are designed with the consideration on real circuit-operating cases in CMOS IC's. By using this new design methodology, CMOS IC's still have a high latchup immunity.

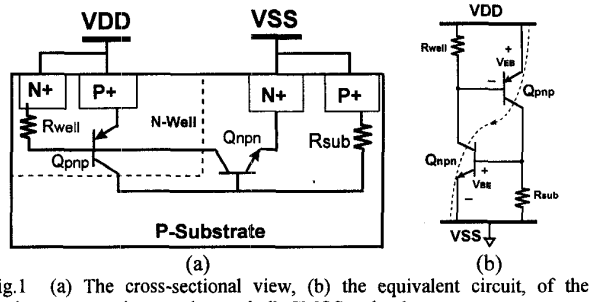


Fig.1 (a) The cross-sectional view, (b) the equivalent circuit, of the latchup structure in a p-substrate bulk CMOS technology.

Latchup in CMOS IC's

Latchup in CMOS IC's is formed by the parasitic p-n-p-n structure between the VDD and VSS [1]. The device cross-sectional view of latchup path in a p-substrate bulk CMOS technology is shown in Fig.1(a), whereas the 1st-order equivalent circuit of the latchup path is illustrated in Fig.1(b). If the latchup is fired in CMOS IC's, it causes a low-impedance path with a high current loss from VDD to VSS to burn out the chip. To prevent the occurrence of latchup in CMOS IC's, some advanced process techniques (such as the epitaxial substrate, retrograde well, trench isolation, or SOI) had been used to increase the holding voltage of the parasitic p-n-p-n structure in CMOS IC's [2]. Although such advanced techniques can effectively solve the latchup issue in CMOS IC's, the production cost of CMOS IC's with such advanced techniques is more expensive. Thus, the most consumer IC products are still manufactured in the bulk CMOS process.

In the bulk CMOS process, the guard rings in the I/O cells and the p-substrate/n-well pickups in the internal circuits are generally used to prevent latchup occurrence in CMOS IC's. Therefore, some layout rules are specified in the design rules of CMOS technologies to prevent the occurrence of latchup. To define the latchup layout rules in CMOS process, some test structures with different layout spacings had been used to investigate the latchup immunity [3]-[7]. The typical latchup test structure is shown in Fig.2, where the trigger nodes are drawn in the p-substrate or the n-well of the test structure. By applying different trigger current or voltage into the trigger nodes in the test structure, the threshold trigger current to initiate latchup occurrence in the test structure can be measured. A trigger current of only several mA can trigger on the latchup path in the test

0-7803-5443-5/99/$10.00©1999 IEEE

structure in a bulk CMOS process. Although the critical value of the trigger current to cause latchup in the test structures can be founded, but the critical trigger current has no relation to the real substrate or well current when the CMOS IC's are in normal circuit operation. Therefore, some empirical layout rules are specified from experience to prevent latchup in CMOS IC's. For example, in a 0.5-μm bulk CMOS process, the maximum distance between every two pickups in p-substrate or n-well is specified as 40μm.

The I/O cells, which are connected to the bond pads in CMOS IC's, are often triggered by the external overshooting or undershooting voltage/current signals. Therefore, the double guard rings are especially specified in the design rules to prevent latchup in the I/O cells. The test structure shown in Fig.3 is often used to investigate the layout rules of double guard rings for I/O cells [4].

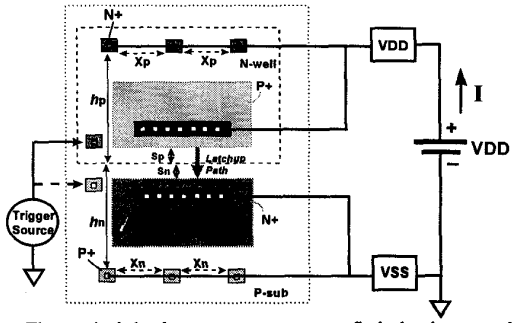


Fig.2 The typical latchup test structure to find the layout rules for substrate and well pickups in internal circuits in the bulk CMOS process.

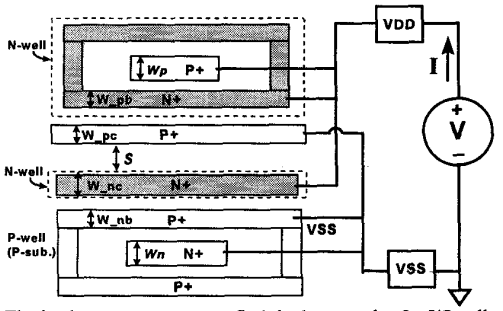


Fig.3 The latchup test structure to find the layout rules for I/O cells in the bulk CMOS process.

To verify the latchup immunity of CMOS IC's, a overshooting (positive) current or undershooting (negative) current are applied to the I/O pins of CMOS IC's to investigate whether the latchup is fired, or not [8]. The schematic diagram to show such latchup testing is illustrated in Fig.4(a). The latchup in CMOS IC's is also sensitive to VDD power transition [9]-[10]. To verify the latchup immunity of CMOS IC's due to such power-transient trigger, the test configuration is illustrated in Fig.4(b). For general CMOS IC's, they should not be triggered into latchup by a trigger current of ±100mA on the I/O pins or a trigger voltage of 1.5×VDD on the VDD pin [8].

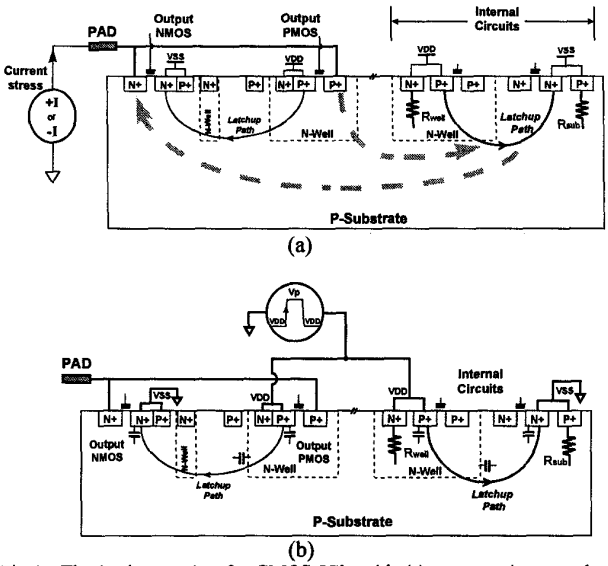


Fig.4 The latchup testing for CMOS IC's with (a) current trigger at the I/O pins, and (b) power-transient trigger at the VDD pin.

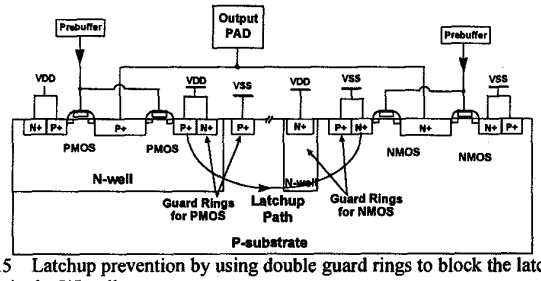


Fig.5 Latchup prevention by using double guard rings to block the latchup path in the I/O cell.

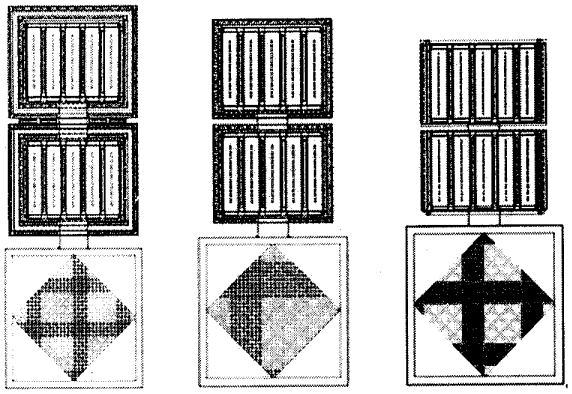
In Fig.4(a), the overshooting/undershooting trigger current on the I/O pin is conducted into the drain regions of the output devices. When the overshooting (undershooting) current is applied to the I/O pin, the P+ drain / n-well (N+ drain / p-substrate) junction in the output PMOS (NMOS) is forward biased to generate the trigger current into the substrate. This substrate current can fire the latchup paths in the I/O cell or the internal circuits. To avoid the latchup paths in CMOS IC's fired by the overshooting or undershooting current on the I/O pins, the double guard rings are often used to block the latchup path between the output PMOS and NMOS in the I/O cells, as shown in Fig.5.

Methodology to Extract Compact Layout Rules

To further reduce layout area of the I/O cell for high-pin-count applications, one set of I/O cells with double guard rings, single guard rings, or no guard ring, are drawn with different anode-to-cathode distances between the output PMOS and NMOS to investigate the latchup immunity in a 0.5-μm bulk CMOS process. The I/O cells with double guard rings, single guard rings, or no guard ring, are shown

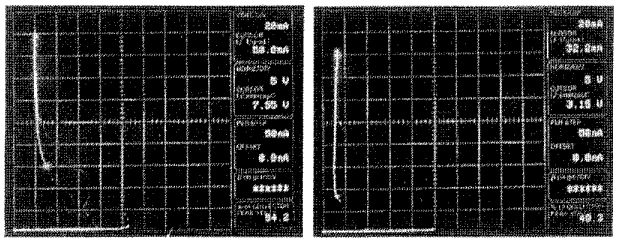
in Fig.6(a) -6(c). Such I/O cells had been fabricated in a 0.5-μm bulk CMOS process and the holding voltage of the latchup path in those I/O cells is measured. The measured latchup I-V characteristics of the I/O cell with single guard ring and a anode-to-cathode spacing of 15μm under temperature of 100°C is shown in Fig.7(a) with a holding voltage of 7.55V, whereas the I-V characteristics of the I/O cell with no guard ring and a anode-to-cathode spacing of 20μm under temperature of 30°C is shown in Fig.7(b) with a holding voltage of 3.15V. The P+ (N+) diffusion width of the single guard ring for output NMOS (PMOS) is drawn as 3μm (3μm).

The dependence of the holding voltage on the layout spacing and temperature effect is shown in Fig.8. By only using a single guard ring to surround each PMOS and NMOS in the I/O cell and with a anode-to-cathode spacing of only 12μm, the holding voltage of the latchup path in the I/O cell can be kept greater than VDD (5V) even if the temperature is as high as 125°C. With only single guard ring in the I/O cell and a narrower anode-to-cathode spacing, the total layout area of the I/O cell can be significantly reduced.



(a) (b) (c)

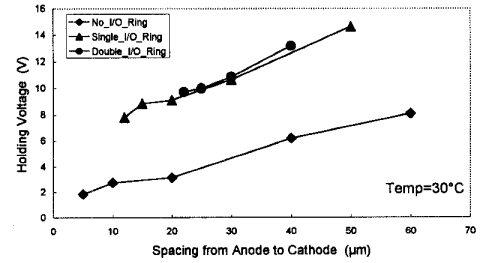
Fig.6 The I/O cell layout with (a) double guard rings, (b) single guard ring, and (c) no guard ring, to investigate the layout rules for I/O cells to prevent latchup.



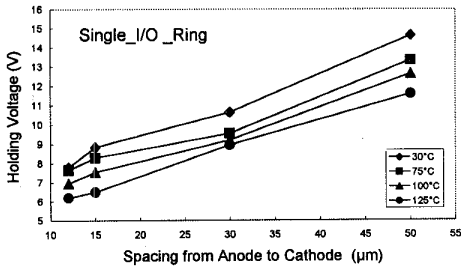
(a) (b)

Fig.7 The measured latchup I-V characteristics of the I/O cell with (a) single guard ring under temperature of 100°C, (b) no guard ring under temperature of 30°C.

With a holding voltage greater than VDD, the I/O cell can be free to latchup issue. But the internal circuits in the bulk CMOS IC's is still sensitive to latchup. As shown in Fig.4(a), the overshooting or undershooting trigger current applied to the I/O pins will generate substrate current to cause latchup occurrence in the internal circuits. To avoid the substrate current generated from the I/O cells to cause latchup in the internal circuits, the internal circuits should keep an enough distance away from the I/O cells. To investigate the suitable distance to avoid latchup occurrence in the internal circuits, a test method is proposed in Fig.9, where a latchup sensor cell is especially drawn and placed in parallel to the I/O cells. The latchup sensor cell is drawn with a specified distance (S_1a, S_1b, S_2a, and S_2b) between the p-substrate / n-well pickups.



(a)



(b)

Fig.8 The relations between the holding voltage and the anode-to-cathode spacing for the I/O cells, (a) at the temperature of 30°C with different guard rings design, (b) with only single guard ring but with different temperatures from 30 to 125 °C.

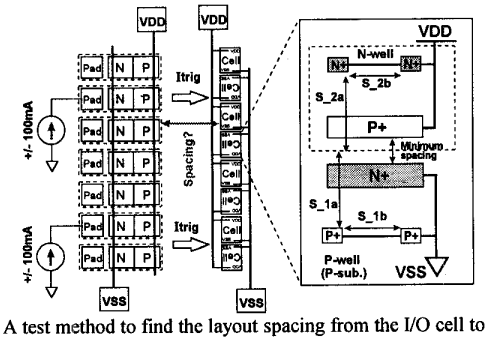


Fig.9 A test method to find the layout spacing from the I/O cell to internal circuits.

To further reduce the distance between the I/O cells and internal circuits to save chip size, the additional guard rings should be placed between the I/O cells and the internal circuits, as shown in Fig.10. To define the important layout

rules on the additional internal guard rings between the I/O cells and internal circuits, several testchips with different layout spacing from the I/O cells to internal latchup sensor cells are drawn and fabricated. One of the experimental testchips to define the layout rules for the internal guard rings is shown in Fig.11. Those testchips had been fabricated in a 0.5-μm bulk CMOS process and used to find the relations between the layout spacing and the trigger current (on the I/O pins) to cause latchup in the internal circuits. The measured results are shown in Fig.12(a) and 12(b). When the additional internal double guard rings are biased, the trigger current on the I/O pins to cause latchup occurrence in the internal latchup sensors is increased while the spacing from the I/O cells to the latchup sensors is increased. According to the EIA/JEDEC standard of ± 100mA current trigger at the I/O pins, a distance of 30μm from the I/O cells to the latchup sensors is enough to prevent latchup occurrence in the internal circuits with the help of additional internal double guard rings. The diffusion widths of the additional internal double guard rings are drawn as 3μm in the experimental testchips. By using the proposed latchup prevention design, a compact layout rules can be obtained with a shorter distance between the I/O cells and internal circuits to reduce the whole chip size of the high-pin-count IC's in bulk CMOS process.

Conclusion

An experimental methodology has been demonstrated to find the compact layout rules for latchup prevention in the bulk CMOS IC's. By applying such compact latchup layout rules in the high-pin-count CMOS ULSI to save whole chip size, the I/O cells with a single guard ring and a shorter distance to the internal circuits still have an enough latchup immunity for safe applications. The extracted compact latchup layout rules in the 0.5-μm bulk CMOS process have been practically applied in some consumer IC products to save the chip size but still to maintain a high latchup immunity.

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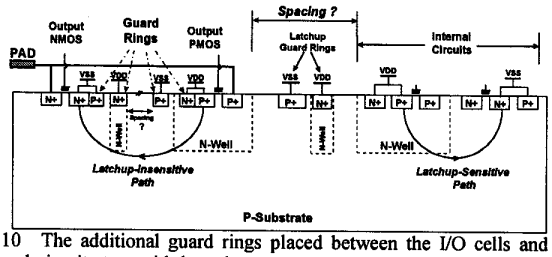


Fig.10 The additional guard rings placed between the I/O cells and the internal circuits to avoid the substrate current generated form I/O cells but to cause latchup in the internal circuits.

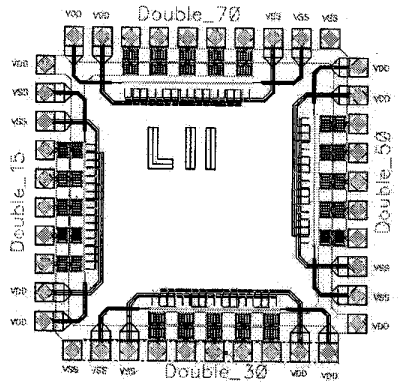
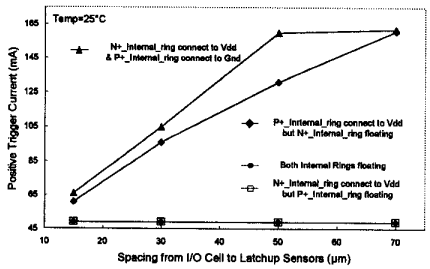
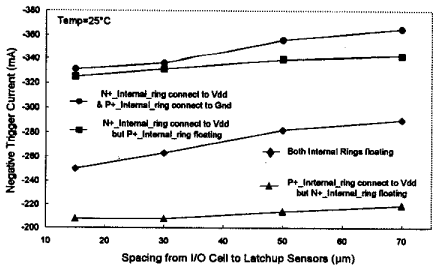


Fig.11 One of the experimental testchips fabricated in a 0.5-μm bulk CMOS process used to investigate the layout rules for the additional internal guard rings.



(a)



(b)

Fig.12 The relations between the (a) positive, (b) negative, trigger current on the I/O pins and the layout spacing from I/O cells to latchup sensors under different guard rings biases.