

Whole-Chip ESD Protection Strategy for CMOS IC's with Multiple Mixed-Voltage Power Pins

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Abstract

A novel whole-chip ESD (electrostatic discharge) protection design with multiple ESD buses has been proposed to solve the ESD protection issue in the CMOS IC which has multiple mixed-voltage power pins. The ESD current in the CMOS IC is diverted into the ESD buses, therefore the ESD current is conducted by the ESD buses away from the internal circuits and quickly discharged through the desired ESD protection devices. By using the ESD buses, the CMOS IC with separated power pins can be safely protected against the ESD damages which is often located in the internal circuits.

Introduction

To improve ESD robustness of CMOS IC products, some additional process modifications (such as the ESD-implantation or the silicide-blocking processes) and circuit design techniques (such as the LVTSCR device [1], the gate-coupled design [2], or the substrate-triggered design [3]) had been used in the input/output ESD protection circuits of CMOS IC's. But, even with the effective ESD protection circuits on the input and output pins, some unexpected ESD damages still happen on the internal circuits of CMOS IC's [4]-[6]. Besides, the power pins for different circuitry in an ULSI are often separated to overcome the noise-coupling and ground-bouncing issues for high-performance circuit operation. For an IC with multiple supply voltage levels, the power pins in the chip have to be separated. But, the IC with separated power pins are more sensitive to internal ESD damage [7]. The pin-to-pin ESD stress to cause the ESD damage on the internal circuits is illustrated in Fig.1. So, the main challenging to ESD protection in the CMOS IC's with multiple or mixed-voltage power pins is how to design the effective whole-chip ESD protection to avoid the ESD damages located on the internal circuits or the interface circuits.

In this paper, a general whole-chip ESD protection strategy with multiple ESD buses is proposed to overcome the internal ESD damages in the CMOS IC with multiple mixed-voltage power pins.

Previous Design

To overcome the unexpected ESD damage located at the internal circuits or interface circuits, some pervious designs had been reported by adding the series diode string between the separated power lines of the CMOS IC [8]-[10]. The typical previous design is shown in Fig.2, where the bi-directional diode strings are connected between the VDD1 and

VDD2, or between the VSS1 and VSS2, power lines of the CMOS IC. The number of diodes in the diode string between the separated power lines is dependent on the voltage level or the noise level between the separated power lines. The additional diode strings between the separated power lines are designed to conduct the ESD current between the separated power lines to avoid the ESD damage located at the internal circuits, when the IC is under the ESD-stress condition. But, when the IC is in the normal operating condition with normal power supplies, the diode string is designed to block the voltage or noise between the separated power lines.

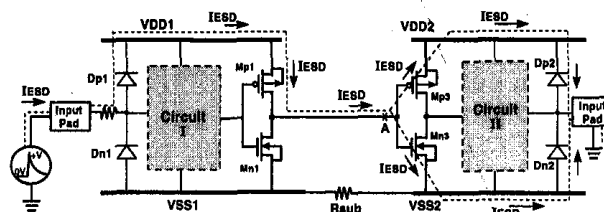


Fig.1 A schematic diagram to show the pin-to-pin ESD damage located at the interface circuits between the separated power lines of the CMOS IC with separated power pins.

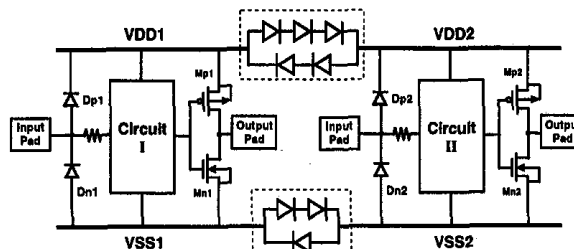


Fig.2 The prior art by using the bi-directional diodes to overcome the ESD damage at the interface circuits of the CMOS IC with separated power pins.

If the IC has much more separated power pins, the bi-directional diode strings have to be added between every two adjacent separated power lines. A typical example by using the bi-directional diode strings to connect the separated power lines of a CMOS IC with four separated circuitry is shown in Fig.3. In Fig.3, there are four circuitry with four separated power pairs. The circuit I is supplied by the VDD1 and VSS1. The circuit II is supplied by the VDD2 and VSS2. The circuit III is supplied by the VDD3 and VSS3. The circuit IV is supplied by the VDD4 and VSS4. The bi-directional diode strings are therefore added between the VDD1 and VDD2, between the VDD2 and VDD3, and between the VDD3 and

VDD4. The bi-directional diode strings are also added between the VSS1 and VSS2, between the VSS2 and VSS3, and between the VSS3 and VSS4. Such bi-directional diode strings provide the ESD-current conducting path between the separated power lines when the IC is under the ESD-stress conditions.

For an example in the pin-to-pin ESD-stress condition, as shown in Fig.3, a positive ESD voltage is attached to some input pad of the circuit I, but some input pad of the circuit IV is relatively grounded. During this pin-to-pin ESD stress, the positive ESD voltage/current is first conducted into the VDD1 (or VSS1) through the diode Dp1 (Dn1) in the input ESD protection circuit on the input pad. Such ESD voltage/current on the VDD1 (VSS1) is conducted into the VDD2 (VSS2) through the diode string between the VDD1 and VDD2 (VSS1 and VSS2).

As the dashed lines illustrated in Fig.3, the ESD voltage/current is finally conducted into the VDD4 (or VSS4) through the diode strings between the separated power lines of the IC. Finally, the ESD voltage/current is discharged from the grounded input pad of circuit IV to the ground through the diodes Dp4 or Dn4 in the input ESD protection circuit on the input pad. In Fig.3, the ESD current has to be discharged through at least 3 diode-strings, before the ESD current goes out from the grounded input pad of the circuit IV. If the CMOS IC has much more separated power pins to supply much more different circuitry, the ESD current will be discharged through much more diode strings connected between the separated power lines. The more diode-strings in the ESD-current discharging paths lead to a longer delay to bypass the ESD current away from the internal circuits of the CMOS IC with separated power pins. Therefore, the ESD damages may still happen to the internal circuits of the CMOS IC with more separated power pins. So, the ESD protection design of Fig.2 is no longer suitable for the CMOS IC which has much more separated power pins.

Whole-Chip ESD Protection Strategy

A. ESD Protection with multiple ESD Buses :

The proposed whole-chip ESD protection strategy with multiple ESD buses to overcome the ESD failure on the internal circuits or interface circuits of a CMOS IC with multiple mixed-voltage power pins is illustrated in Fig.4, where the CMOS IC has three VDD power supplies (2.5V, 3V, and 5V). In such a CMOS IC with complex power supplies, four ESD buses are used to configure the whole-chip ESD protection scheme. The ESD-Bus-1 (ESD-Bus-4) is used to connect the VDD_2.5V (VDD_3V) power lines of the circuit I and circuit II (circuit III and circuit IV) through the bi-directional ESD-connection cells. The ESD-Bus-3 is used to connect the VDD_5V power lines of the circuit V to circuit K through the bi-directional ESD-connection cells. Because the voltage levels of the VSS power lines between the circuitry are all ground, the ESD-Bus-2 is used to connect all the VSS_0V power lines of the circuit I to the circuit K through the bi-directional ESD-connection cells. Between the ESD buses, five ESD clamp cells are used to connect the ESD-Bus-1, ESD-Bus-2, ESD-Bus-3, and ESD-Bus-4. A CMOS IC even

with more complex mixed-voltage power supplies can be still well protected by this proposed whole-chip ESD protection scheme with multiple ESD buses.

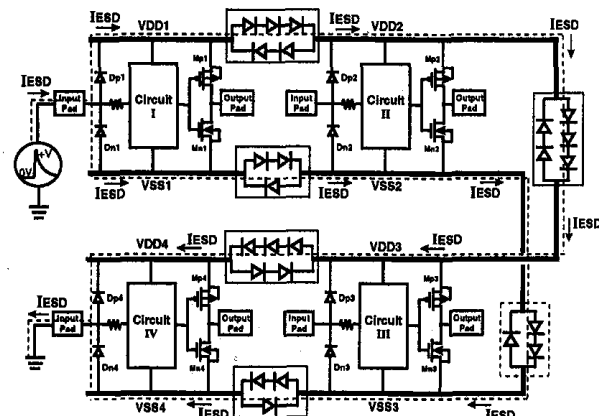


Fig.3 The pin-to-pin ESD current discharging paths in the CMOS IC with more separated power pins.

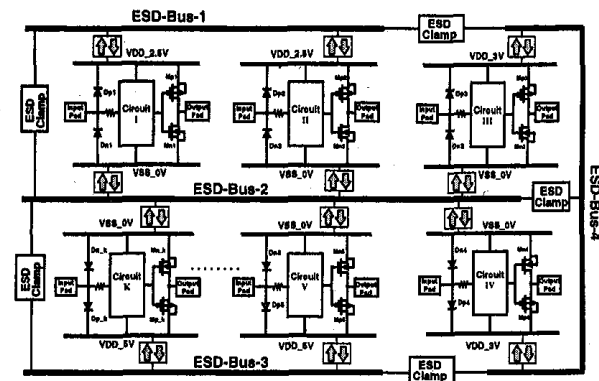


Fig.4 The schematic circuit diagram to show the proposed whole-chip ESD protection scheme with the multiple ESD buses to overcome the ESD failure on the internal circuits of a CMOS IC with multiple mixed-voltage power pins.

B. The Bi-directional ESD-Connection Cells :

The circuit diagram and device structure of the bi-directional ESD-connection cells connected between the VDD/VSS power lines and the ESD buses are shown Fig.5. In Fig.5, the bi-directional ESD-connection cell is formed by two NMOS-triggered SCR devices (NSCR1 and NSCR2), which can provide bi-directional current paths between the ESD-Bus-# and the VDD_# (or VSS_#) power lines. In Fig.5, if the voltage difference from the ESD-Bus-# to the VDD_# (or VSS_#) power line is greater than the threshold voltage of the NMOS, the NSCR2 will be triggered on to provide a low-impedance path between the ESD-Bus-# and the VDD_# (or VSS_#) power line. On the other hand, if the voltage difference from the VDD_# (or VSS_#) power line to the ESD-Bus-# is greater than the threshold voltage of the NMOS, the NSCR1 will be triggered on to provide a low-impedance path between the ESD-Bus-# and the VDD_# (or VSS_#) power line. This provides the bi-directional current paths between the ESD-Bus-# and the VDD_# (or VSS_#) power

lines to achieve the whole-chip ESD protection scheme with the multiple ESD buses.

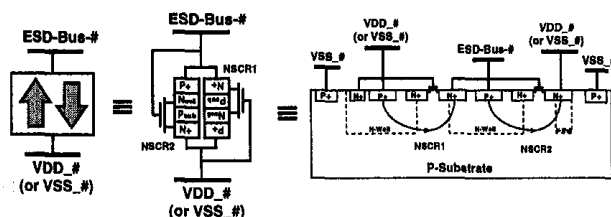


Fig. 5 The schematic diagram and cross-sectional view of the bi-directional ESD-connection cell realized by the NMOS-triggered lateral SCR devices.

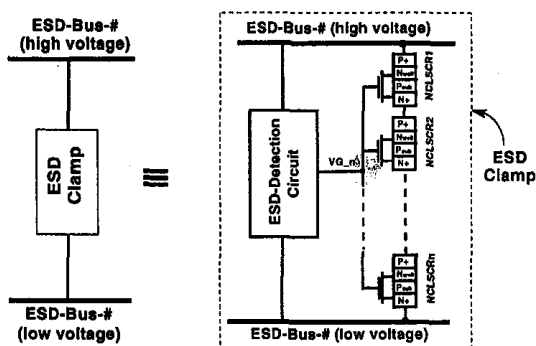


Fig. 6 The schematic diagram of the ESD clamp cell realized by the cascoded NCLSCR devices between the high-voltage and low-voltage ESD buses.

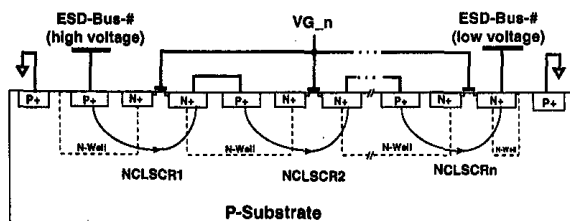


Fig. 7 The schematic cross-sectional view of the cascoded NCLSCR's.

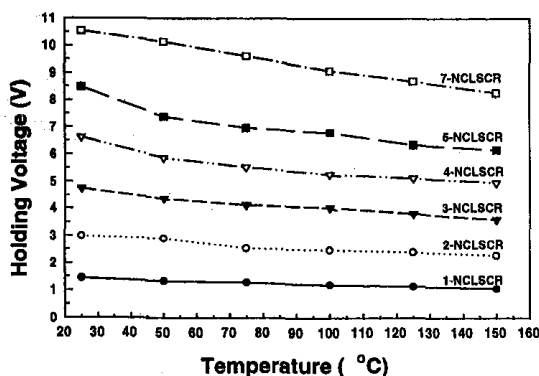


Fig. 8 The temperature dependence of the total holding voltage in the cascoded NCLSCR's with different number of NCLSCR devices.

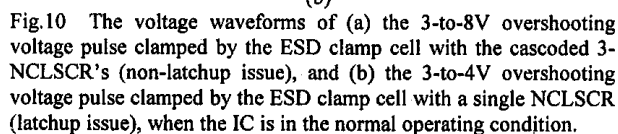
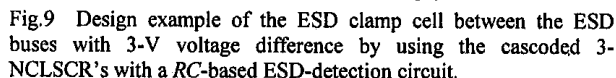
C. The Efficient ESD Clamp Cells :

The ESD clamp cell between the ESD buses with different voltage levels is shown in Fig. 6. In Fig. 6, a plurality of NMOS-controlled lateral SCR's (NCLSCR's) are formed in cascode configuration from the ESD-Bus-# of high voltage to the ESD-Bus-# of low voltage. The device structures of the cascoded NCLSCR's are drawn in Fig. 7. The gates of the NMOS's in the cascoded NCLSCR's are controlled by an ESD-detection circuit. When the ESD voltage/current occurs across the ESD clamp cell, the ESD-detection circuit will quickly generate a voltage level greater than the NMOS turn-on voltage to turn on the cascoded NCLSCR's. But, when the IC is in the normal operating condition, the voltage level on the node VG_n in Fig. 6 is kept at the voltage level of the ESD-Bus-# of low voltage. Thus, the NMOS's in the NCLSCR's are kept off, and then the cascoded NCLSCR's are guaranteed to be off to block the current path between the ESD-Bus-# of high voltage and the ESD-Bus-# of low voltage. The number (n) of the NCLSCR devices in the cascoded NCLSCR's between the ESD-Bus-# of high voltage and the ESD-Bus-# of low voltage can be calculated as $n \geq (V_{diff} / V_{hold})$. The V_{diff} is the voltage difference from the ESD-Bus-# of high voltage to the ESD-Bus-# of low voltage, when the IC is in the normal operating condition. The V_{hold} is the holding voltage of a single NCLSCR device, which is typically about $\sim 1V$ in the general bulk CMOS technology. With suitable number of the cascoded NCLSCR devices in the ESD clamp cells, the latchup issue to cause power loss through the ESD clamp cells does not happen between the ESD-Bus-# of high voltage and the ESD-Bus-# of low voltage.

Realization in a 0.35- μm CMOS Technology

The total voltage drop across the cascoded NCLSCR's is the sum of the voltage drop across every NCLSCR device. Therefore, the total holding voltage of the cascoded NCLSCR's becomes tunable by changing the number of the NCLSCR's in the cascode configuration. The cascoded NCLSCR's with different number of NCLSCR devices have been investigated in a 0.35- μm bulk CMOS process with both silicided diffusion and LDD structure. The device characteristics, especially including the temperature effect, has been measured and investigated in Fig. 8 [11]. To avoid the latchup issue between the ESD buses when the IC is in the normal operating condition, the total holding voltage of the cascoded NCLSCR's has to be greater than the voltage difference between the ESD buses.

In Fig. 8, the holding voltage of the 3-NCLSCR's is 3.82V at temperature of 125°C, whereas the holding voltage of the 5-NCLSCR's is 6.36V. For example, to safely apply the cascoded NCLSCR's for ESD protection in 3-V CMOS IC's without causing latchup danger, three cascoded NCLSCR's have to be used. This provides a practical and useful solution to safely apply the NCLSCR for effective ESD protection, especially in the bulk CMOS process. The ESD clamp cell by using the cascoded 3-NCLSCR's with the RC-based ESD-detection circuit [12] is shown in Fig. 9.



The turn-on verifications on the ESD clamp cells with three NCLSCR's or a single NCLSCR between the ESD buses has been practically investigated to verify the latchup issue in the normal operating condition, as shown in Fig.10. With three NCLSCR's, the ESD clamp cell can provide effective ESD protection but without causing latchup danger between the ESD buses with 3-V voltage difference.

In the 0.35- μm bulk CMOS process, the cascoded 3-NCLSCR's with a layout area of $60 \times 60 \mu\text{m}^2$ can sustain a 3-kV HBM ESD stress. Whereas, a gate-grounded NMOS (ggNMOS) with a device dimension of $W/L=480/0.5$ occupies a layout area of $80 \times 76 \mu\text{m}^2$ can sustain an HBM ESD level of only 1.5kV. So, the ESD robustness per layout area of the

cascoed 3-NCLSCR's (ggNMOS) is $0.83 \text{ V}/\mu\text{m}^2$ ($0.25 \text{ V}/\mu\text{m}^2$) in the $0.35\text{-}\mu\text{m}$ bulk CMOS process without using the extra silicide-blocking and ESD-implantation process steps. This shows the good area efficiency for using the NCLSCR's to realize the ESD clamp cells and the bi-directional ESD-connection cells for whole-chip ESD protection design with multiple ESD buses.

A novel ESD protection strategy of using multiple ESD buses to perform the whole-chip ESD protection for the CMOS IC with multiple mixed-voltage power pins has been demonstrated in this paper. The ESD damages located on the internal circuits or interface circuits beyond the input/output ESD protection circuits can be overcome by this ESD protection strategy. Such a protection strategy with ESD buses has been practically applied in the design rules of TSMC 0.35- μm and 0.25- μm CMOS technologies to help the IC designers to achieve a successful whole-chip ESD protection.

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