Experimental Investigation on the HBM ESD Characteristics of CMOS Devices in a 0.35-μm Silicided Process

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Abstract

In this paper, the layout dependence on ESD robustness of NMOS and PMOS devices in a 0.35-μm silicided CMOS process has been experimentally investigated in details. Six 40-pins testchips including 78 different devices with different device dimensions, layout spacings, and clearances have been drawn and fabricated in a 0.35-μm silicided CMOS process to find the optimal layout rules for the ESD protection devices. The gate-driven effect and substrate-triggered effect on the ESD performance of CMOS devices are also measured and compared. The experimental results show that the substrate-triggered effect is much better than the gate-driven effect to improve ESD robustness of the CMOS devices.

Introduction

To design area-efficient ESD protection circuits, the robustness of protection devices is considered as strong as possible in per unit layout area. To optimize the layout area, the layout spacings are the major considerations for designing strong ESD robustness devices [1]-[3]. The main layout factors to affect the ESD level of ESD-protection devices are the channel width (W), channel length (L), the clearance from contact to poly-gate edge at drain and source regions (Dcg & Scg), the spacing from the drain diffusion to the guardring diffusion (Sba), and the finger width (Wf) of each finger, which are indicated in the 2-D device structure of an NMOS as shown in Fig.1. Generally, the ESD current flow in an NMOS device has two discharging paths. One is the channel current of the MOSFET, and the other is the lateral-BJT current flowing through the bulk of the MOSFET device. These two kinds of ESD currents are also shown in Fig.1.

In this work, the dependence of these five layout factors on the ESD level of the NMOS and PMOS devices are practically investigated through the six 40-pins fabricated testchips. Besides, the gate-driven effect [4] and the substrate-triggered effect [5] used to improve the ESD robustness of the ESD protection circuits are also investigated in more details.

Layout Dependence

ESD robustness of CMOS devices in the output buffers or input ESD protection circuits is strongly dependent on the layout style and layout spacings. The layout factors to affect the ESD robustness of CMOS devices are practically investigated on the fabricated testchips in a 0.35-μm silicide CMOS process. The *ZapMaster* ESD tester, produced by *Keytek Instrument Corp.*, is used to measure the human-body-model (HBM) ESD level of the fabricated testchips.

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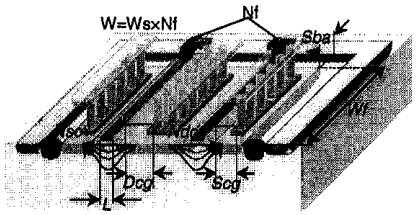


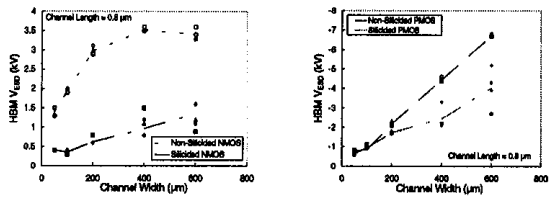
Fig.1 The device structure of an NMOS.

A. Channel Width Dependence

The relations between the device channel width (W) and the HBM ESD level of NMOS and PMOS devices are shown in Fig.2(a) and 2(b), respectively. The finger width (Wf) of the NMOS and PMOS devices in the finger-type layout is kept as 50 μm. For both NMOS and PMOS devices, the channel length (L), the clearance from drain contact to poly-gate edge (Dcg), the clearance from source contact to poly-gate edge (Scg), and the spacing from the drain diffusion to the guardring diffusion (Sba) are drawn as 0.8μm, 3μm, 1μm, and 4μm, respectively. The NMOS and PMOS devices with and without the RPO layer [6] to block the silicided diffusion on the drain region are also drawn in the testchips to investigate their ESD level.

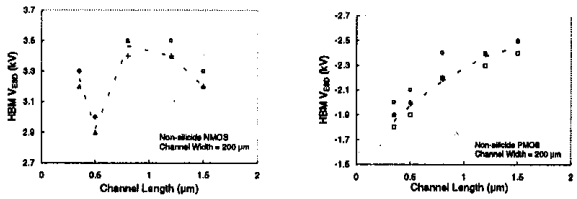
In Fig.2(a), the HBM ESD level of the NMOS device is roughly increased while the device channel width is increased. The NMOS device with silicide-blocking process can sustain much higher ESD level than that with the sicilided diffusion. For example, the ESD level of the silicided NMOS with a channel width of 400μm is only 0.97kV, but that of the non-silicided NMOS with the same device dimension and layout style is 3.5kV. If the device channel width is increased, more of fingers are drawn and connected in parallel to form the large-dimension NMOS device. The ESD level of such large-dimension devices may decrease while the device channel width is increased. In Fig.2(a), the ESD level (3.4kV) of the non-silicided NMOS with a channel width of 600μm is less than that (3.5kV) of the non-silicided NMOS with a channel width of 400μm. This is due to the non-uniform turn-on issue among the multiple fingers of a large-dimension device.

In Fig.2(b), the ESD levels of the PMOS with or without silicided diffusion are both increased as the device channel width is increased. But, the ESD level of the silicided PMOS with a channel width of 400μm is only -2.45kV, but that of the non-silicided PMOS with the same device dimension and layout style is -4.45kV. This verifies the effectiveness of the silicide-blocking process used to improve ESD level in deep-submicron CMOS technologies.



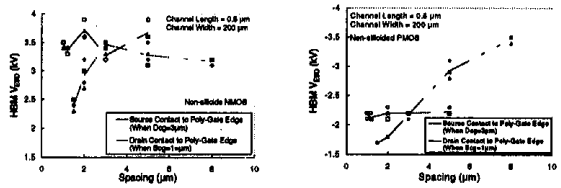
(a) (b)

Fig.2 The dependence of ESD level on the channel width of (a) NMOS, and (b) PMOS, with or without silicided diffusion.



(a) (b)

Fig.3 The dependence of ESD level on the channel length of (a) NMOS, and (b) PMOS, with a fixed channel width of 200μm.



(a) (b)

Fig.4 The dependence of the clearance from the drain/source contact to the poly-gate edge on the HBM ESD level of non-silicided (a) NMOS, and (b) PMOS.

B. Channel Length Dependence

The relations between the device channel length (L) and the HBM ESD level of NMOS and PMOS devices are shown in Fig.3(a) and 3(b), respectively. The layout style and spacings are all kept the same (W=200μm, Ws=50μm, Dcg=3μm, Scg=1μm, and Sba=4μm), but only the channel length is different under this investigation. Both the NMOS and POMS are fabricated with the RPO layer to block the silicided diffusion on the drain region.

From the experimental results shown in Fig.3(a), the HBM ESD level of the NMOS with a minimum channel length of 0.35μm is 3.25kV, whereas that of the NMOS with a channel length of 0.5 (0.8) μm is 2.9 (3.4) kV. In Fig.3(a). the NMOS with a channel length of 0.5 μm has the lowest ESD level in this experimental investigation. When an NMOS has a shorter enough channel length, the efficiency and performance of the parasitic lateral BJT in the NMOS device is significantly improved. Therefore, it can sustain much higher ESD level than the NMOS with a medium channel length about 0.5~0.8 μm. On the contrary, the PMOS with a shorter channel length has a lower ESD level, as shown in Fig.3(b). Even if the PMOS with a minimum channel length of 0.35 μm, its HBM ESD level is only -1.85kV because the lateral p-n-p BJT in the PMOS device is not efficient.

From this experimental investigation, the selection on the channel length of NMOS and PMOS for ESD protection is quite different in the 0.35-μm silicided CMOS process.

C. Drain/Source Contact to Poly-Gate Edge

The dependence of the clearances from the drain/ source contact to the poly-gate edge (Dcg and Scg) on the HBM ESD level of NMOS and PMOS devices is shown in Fig.4(a) and 4(b), respectively. In this investigation, all the layout style and other spacings are kept the same (W=200μm, Ws=50μm, L=0.8μm, and Sba=4μm), but only the Dcg and Scg are varied from 1 to 8 μm in the testchips. Both the NMOS and POMS are fabricated with the RPO layer to block the silicided diffusion on the drain and source regions.

From the experimental results, the clearance variation on the Scg from 1 to 5 μm at the source region (with a fixed Dcg of 3μm at the drain region) only leads to a slight variation on the ESD level from 3.3kV to 3.6kV (-2.1kV to -2.2kV) in the non-silicided NMOS (PMOS) device. But, the clearance variation on the Dcg from 1.5 to 8 μm at the drain region (with a fixed Scg of 1μm at the source region) can cause significantly improvement on the ESD level from 2.4kV to 3.4kV (-1.7kV to -3.4kV) in the non-silicided NMOS (PMOS) device. Therefore, the clearance of Dcg in both PMOS and NMOS devices for ESD protection is suggested greater than 3 μm to achieve better ESD robustness in the 0.35-μm silicided CMOS process.

D. Spacing from Drain Diffusion to Guardring Diffusion

The spacing from the drain diffusion to the first guardring diffusion in the finger-type layout also has an obvious impact on the ESD robustness of the NMOS and PMOS devices. This spacing is illustrated in Fig.5 and marked as "Sba". The wider spacing Sba contributes a larger base resistance (R_B) to the parasitic lateral n-p-n (p-n-p) BJT in the NMOS (PMOS) device. The parasitic lateral BJT with a larger R_B makes itself to be triggered on more quickly and uniformly to bypass ESD current. The ESD robustness of the NMOS and PMOS devices with different Sba spacings but the fixed other layout spacings (W=200μm, L=0.8μm, Dcg=3μm, Scg=1μm, and Wf=50μm) is investigated in Fig.6(a) and 6(b), respectively. When this Sba spacing is increased from 3μm to 5μm, the HBM ESD level of the NMOS (PMOS) is improved from 2.8kV to 3.6kV (from -1.7kV to -2.2kV). This investigation confirms the important effect from the layout spacing Sba on the ESD level of the ESD protection devices.

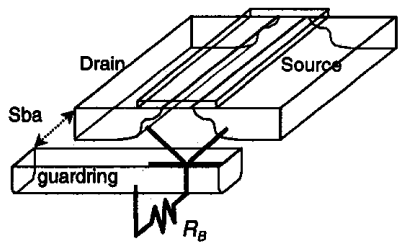
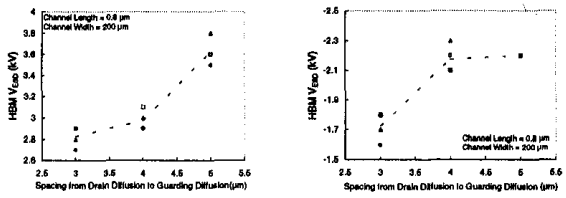
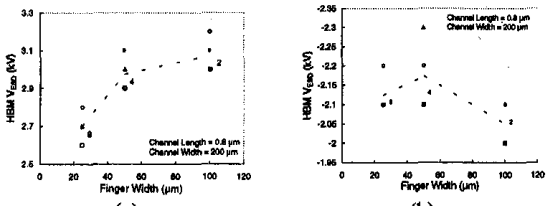


Fig.5 The device structure to show the Sba spacing in the finger-type layout.



(a) (b)

Fig.6 The dependence of ESD robustness of (a) NMOS, and (b) PMOS, on the Sba spacings.



(a) (b)

Fig.7 The dependence of ESD robustness of (a) NMOS, and (b) PMOS, on the finger width and finger number in the finger-type layout.

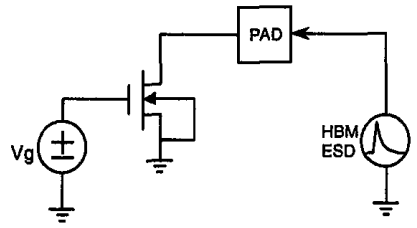


Fig.8 The experimental setup to measure the HBM ESD robustness of NMOS device under the gate-driven effect.

E. Finger Width Dependence

In the finger-type layout, a large-dimension device is traditionally drawn with multiple fingers in a parallel connection. If the finger width (Wf) of every finger is shorter, more fingers are used to construct the large-dimension device. The large-dimension devices with different number of finger and finger width can cause different ESD performance, even if the devices have the same W and L dimensions. The more multiple fingers of a large-dimension device are hard to be uniformly triggered on during the ESD stress, therefore it may cause a different ESD level. To verify this issue, both the NMOS and PMOS devices with the fixed channel width / length of 200μm / 0.8μm but different finger widths are fabricated in the 0.35-μm silicided CMOS process and investigated by the ESD tester. The tested results are shown in Fig.7(a) and 7(b).

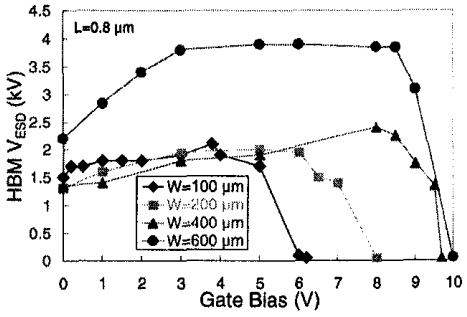
From the experimental results, the ESD level of the NMOS of W=200μm is deceased from 3kV to 2.7kV, while the NMOS is drawn with the finger number from 2 to 8. On the contrary, the more finger number in the PMOS layout leads to a slight lower ESD level.

Gate-Driven Effect

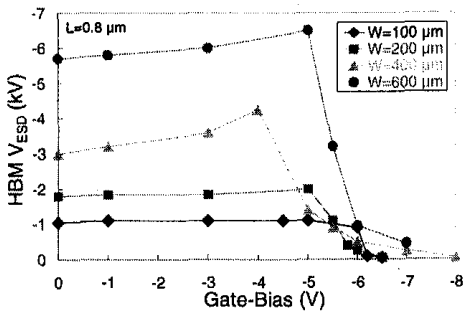
To improve ESD robustness of the ESD-protection NMOS devices, the gate-coupled design had been reported to more uniformly trigger on the multiple fingers of the large-dimension ESD-protection NMOS [4], [7]. But, the coupled voltage on the gate of NMOS can turn on the channel of the NMOS, therefore the ESD current is discharging through the shallow channel region of the ESD-protection NMOS. Due to the shallower junction depths and the LDD structure at the drain/source regions, the turned-on NMOS is weak to sustain ESD stress [8].

To investigate this gate-driven effect, an experimental setup shown in Fig.8 is used to measure the ESD level of the NMOS with different gate biases. The measured results on both the NMOS and PMOS devices with different channel width (W) are shown in Fig.9(a) and 9(b), respectively. The ESD level of the NMOS with W=600μm is initially increased while the gate bias increases from 0V to 4V. But, the ESD level is suddenly decreased while the gate bias is greater than 8.5V, as that shown in Fig.9(a). There is a similar gate-driven effect on the PMOS device. In Fig.9(b), the ESD level (in absolute value) of the PMOS with W=600μm is initially increased while the gate bias changes from 0V to -5V. But, the ESD level is suddenly decreased while the gate bias is lower than -5V.

From the measured results in Fig.9(a) and 9(b), the gate-coupled circuit design used to improve ESD level of the ESD-protection devices has to be correctly optimized to avoid the sudden degradation on the ESD level of the gate-driven ESD-protection devices.



(a)



(b)

Fig.9 The effect of the gate biases on the ESD robustness of (a) NMOS, and (b) PMOS.

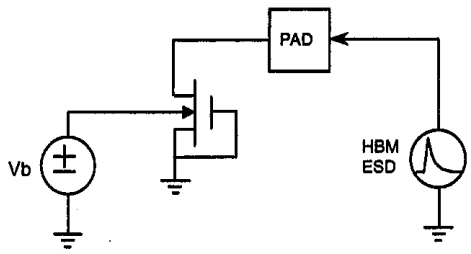
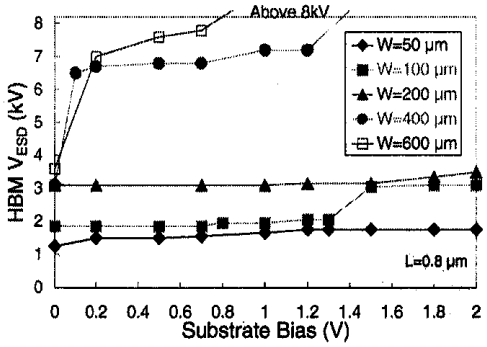
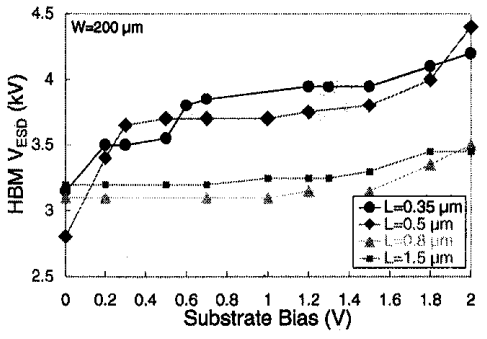


Fig.10 The experimental setup to measure the HBM ESD robustness of NMOS device under the substrate-triggered effect.



(a)



(b)

Fig.11 The effect of the substrate biases on ESD robustness of NMOS devices with (a) different channel width, and (b) different channel length.

Substrate-Triggered Effect

To avoid the degradation on the ESD level of the gate-driven devices, the substrate-triggered design had been reported to improve ESD level of the ESD-protection devices [5], [9]. To investigate the substrate-triggered effect on ESD robustness of the ESD-protection NMOS, an experimental setup is shown in Fig.10, which is used to measure the ESD level of the devices under different substrate biases. The measured results are shown in Fig.11(a) and 11(b) for the NMOS devices with different channel width and length.

In Fig.11(a), the ESD level of the NMOS with a device dimension of W=600μm and L=0.8μm can be significantly increased greater than 8kV while the substrate bias increases from 0V to only 0.8V. In Fig.11(b), the NMOS device (W=200μm) with a shorter channel length and higher substrate bias can sustain a much higher ESD level. The ESD level of the NMOS with a channel length of 0.5μm under 0-V gate and substrate biases is only 2.8kV, but the ESD level is increased up to 4.4kV while the NMOS has a substrate bias of 2V. As shown in Fig.11, the ESD level is not suddenly degraded while the substrate bias increases up to 2V. The substrate-triggered design can effectively improve ESD robustness of the ESD-protection devices without the sudden ESD-level degradation issue in the gate-driven design. Therefore, this substrate-triggered design is more suitable to improve ESD robustness of the ESD-protection devices and circuits in the deep-submicron CMOS technologies.

Conclusion

The dependence of layout spacings on the ESD level of CMOS devices in a 0.35-μm silicided CMOS process has been experimentally investigated in more details. The device with shorter channel length, wider channel width, larger clearance from drain contact to the poly-gate edge, and wider spacing from the drain diffusion to the guardring diffusion generally lead to a higher ESD robustness. Moreover, from the measured results, the gate-driven effect has been confirmed to cause a sudden degradation on the ESD level of ESD-protection devices. But, the substrate-triggered effect can continually increase the ESD level of ESD-protection devices. Some suitable circuit designs have been applied to improve ESD robustness of the ESD-protection devices by the substrate-triggered technique.

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