ESD Protection Design for Mixed-Voltage I/O Buffer by Using Stacked-NMOS Triggered SCR Device

Ming-Dou Ker (1), Chien-Hui Chuang (1), and Hsin-Chin Jiang (2)

(1) Integrated Circuits & Systems Laboratory, Institute of Electronics, National Chiao-Tung University, 1001 Ta-Hsueh Road, Hsinchu, Taiwan. Fax: (886)-3-5715412, e-mail: *mdker@ieee.org*

(2) Analog IP Technology Section, SoC Technology Center, Industrial Technology Research Institute, Hsinchu, Taiwan. e-mail: *hcj@itri.org.tw*

Abstract -- A new ESD protection circuit, by using the stacked-NMOS triggered silicon controlled rectifier (SNTSCR) as the ESD clamp device, is designed to protect the mixed-voltage I/O buffers of CMOS IC's. Without using the thick gate oxide, the experimental results in a 0.35-μm CMOS process have proven that the human-body-model ESD level of the mixed-voltage I/O buffer can be successfully increased from the original ~2kV to become >8kV by using this new proposed ESD protection circuit.

I. Introduction

To improve circuit operating speed and performance, the device dimensions of MOSFET had been shrunk in advanced integrated circuits. In order to follow constant-field scaling requirement and to reduce power consumption, the power supply voltages in CMOS ICs have been also scaled downwards. So, most computer architectures require the interfacing of semiconductor chips or sub-systems with different internal power supply voltages. With the mix of power supply voltages, chip-to-chip interface I/O circuits must be designed to avoid electrical overstress across the gate oxide [1], to avoid hot-carrier degradation [2] on the output devices, and to prevent undesirable leakage current paths between the chips [3]-[4]. For example, 5-V interfacing is generally required for ICs realized in CMOS processes with a normal internal power supply voltage of 2.5V or 3.3V.

To solve the gate-oxide reliability issue without using the additional thick gate-oxide process (or called as dual gate oxide in some CMOS processes [5]-[6]), the stacked-MOS configuration had been widely used in the mixed-voltage I/O buffers [7]-[12], or even used in the power-rail ESD clamp circuits [13]. The typical 3V/5V-tolerant mixed-voltage I/O circuit is shown in Fig. 1 [8]. The pull-up PMOS, connected from the I/O pad to VDD power line, has the self-biased circuits for tracking its gate and n-well voltages, when the 5V input signals enter the I/O pad. ESD stresses on an I/O pad have four zapping modes: positive-to-VSS, negative-to-VSS, positive-to-VDD, and negative-to-VDD ESD-stress conditions. But, the mixed-voltage I/O circuit often has the lowest ESD level (often < 2kV in HBM ESD test) under the positive-to-VSS ESD-stress condition. Therefore, ESD protection design on the mixed-voltage I/O circuits is mainly focused to improve the ESD level under the positive-to-VSS ESD-stress condition.

Due to the limitation of placing a diode from the pad to VDD in the mixed-voltage I/O circuits, the positive-to-VSS ESD voltage zapping on the I/O pad cannot be diverted from the pad to VDD power line, and cannot be discharged through the additional power-rail (VDD-to-VSS) ESD clamp circuit. Such positive-to-VSS ESD current on the I/O pad is totally discharged through the stacked-NMOS in the snapback breakdown condition. Besides, the NMOS in stacked configuration has a higher trigger voltage (Vt1), a higher snapback holding voltage (Vsb), and a lower secondary breakdown current (It2), as compared to the single NMOS [14]. Therefore, such mixed-voltage I/O circuits with stacked NMOS often have much lower ESD level, as compared to the I/O circuits with a single NMOS [14]-[15].

* *This work was partially supported by the National Science Council, Taiwan; and partially supported by Industrial Technology Research Institute, Taiwan.*

To increase ESD level of such mixed-voltage I/O circuits, some designs with extra multiple diodes in stacked configuration had been added from the I/O pad to VDD power line [3]-[4]. However, while the mixed-voltage I/O circuits operating in a high-temperature environment with a high-voltage input, the forward-biased leakage current from the pad to VDD through the stacked diodes must be reduced by additional circuit designs [16]-[19].

To sustain a high ESD level within a much smaller silicon area, the low-voltage-triggering SCR (LVTSCR) device [20]-[22] had been reported as one of the most effective ESD clamp devices in CMOS ICs. But, such an LVTSCR device can't be directly applied to protect the mixed-voltage I/O buffers due to the gate-oxide reliability issue on the short-channel NMOS, which is inserted in the LVTSCR device structure without using the thick gate oxide.

In this paper, a new ESD protection circuit is proposed to significantly improve ESD level of the mixed-voltage I/O buffers by using the stacked-NMOS triggered SCR device. The new proposed ESD protection circuit, which combines the stacked-NMOS structure with the gate-coupling circuit technique into the SCR device, is fully process-compatible to general mixed-voltage I/O circuits without causing the gate-oxide reliability problem. The human-body-model (HBM) ESD level of the mixed-voltage I/O buffers has been successfully increased from the original ~2kV to become >8kV in a 0.35-μm CMOS process, without using the thick gate oxide.

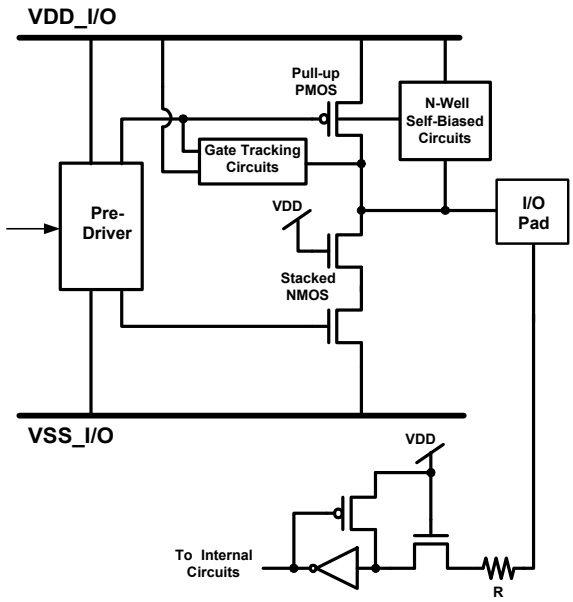


Fig. 1 The typical circuit diagram for the mixed-voltage I/O buffer with the stacked-NMOS and the floating-well PMOS.

II. Stacked-NMOS Triggered Silicon Controlled Rectifier (SNTSCR) Device

A. Device Structure

The cross-sectional view and the corresponding layout pattern of the proposed stacked-NMOS triggered silicon controlled rectifier (SNTSCR) device are shown in Figs. 2(a) and 2(b), respectively. This SNTSCR device structure can be realized in general CMOS processes. The SNTSCR device is disposed on a bond pad to protect the mixed-voltage I/O circuits from ESD damage. The corresponding equivalent circuit of this SNTSCR device is shown in Fig. 3.

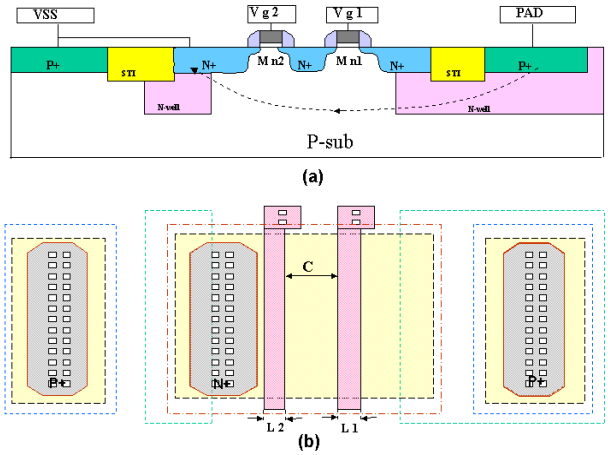


Fig. 2 (a) The cross-sectional view, and (b) the corresponding layout pattern, of the proposed SNTSCR device in a p-substrate CMOS process.

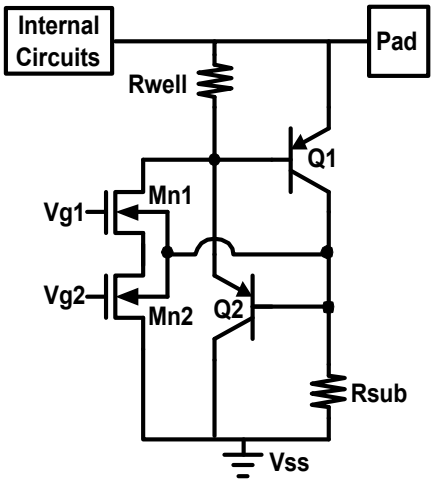


Fig. 3 The equivalent circuit of the proposed SNTSCR device in a p-substrate CMOS process.

In the SNTSCR device, two NMOS transistors (Mn1 and Mn2) are stacked in cascoded configuration, where the drain of Mn1 is across the junction between an N-well region and p-substrate.

The p+ diffusion, N-well, p-substrate, and n+ diffusion to form a lateral SCR between the I/O pad and VSS is indicated by the dashed line in Fig. 2(a). The purpose of Mn1 and Mn2 connected in stacked configuration is to sustain the high voltage level of input signals without causing gate oxide reliability issue in the SNTSCR device under normal circuit operation. If only single NMOS is inserted in the lateral SCR device, such as the traditional LVTSCR [20], the voltage across gate oxide will be greater than VDD when a high-voltage signal enters into the I/O pad. This causes the gate oxide reliability issue on the traditional LVTSCR for long-time operation in such mixed-voltage I/O circuits. During ESD-stress condition, Mn1 and Mn2 are both turned on by suitable gate-biased design to trigger the lateral SCR on for discharging ESD current.

B. Characteristics of the SNTSCR Device

To investigate the characteristics of the proposed SNTSCR device, three layout parameters (C, L1, and L2 shown in Fig. 2) of the layout pattern are adjusted. C is the poly-to-poly spacing across the center floating n+ diffusion. L1 and L2 are the channel lengths of the Mn1 and Mn2, respectively. Such SNTSCR devices with different layout parameters but with a fixed channel width of 60μm have been fabricated in a 0.35-μm CMOS process.

The measured I-V characteristics of the SNTSCR device with C=0.5μm and L1=L2=0.35μm under different gate biases of Vg1 and Vg2 are shown in Fig. 4. The trigger voltage (Vt) of the SNTSCR device decreases from 10V to 6V, when the gate bias increases from Vg1= Vg2=0V to Vg1=Vg2=0.5V. As Vg1=Vg2 > 0.6V, both the Mn1 and Mn2 are turned on to trigger SNTSCR on, therefore the Vt decreases to around 1~2 V. With suitable gate biases on Mn1 and Mn2, the trigger voltage of SNTSCR device can be reduced lower than the snapback voltage of the stacked-NMOS (about ~10V) in the mixed-voltage I/O buffer. Therefore, the new proposed ESD protection circuit with the SNTSCR device can effectively protect the mixed-voltage I/O buffers.

The impacts of layout parameters on Vt of the SNTSCR device are measured and summarized in Fig. 5 and Fig. 6 under the variation of different gate biases (Vg1=Vg2). In Fig. 5, the L1 and L2 are fixed at 0.35μm, but the spacing C is changed. The shorter spacing C causes a lower trigger voltage on SNTSCR device. In Fig. 6, the spacing C is fixed at 0.5μm, but the L1 and L2 are changed. The shorter L1 and L2 channel lengths cause a lower trigger voltage on SNTSCR device. The trigger voltage of the SNTSCR increases when the layout parameters (C, L1, and L2) are increased. But, when the gate biased is increased up to > 0.6V, the trigger voltage can be lowered significantly. After the turn-on of SNTSCR device, its holding voltage is around ~1V, which is not obviously changed by the different layout parameters on C, L1, and L2.

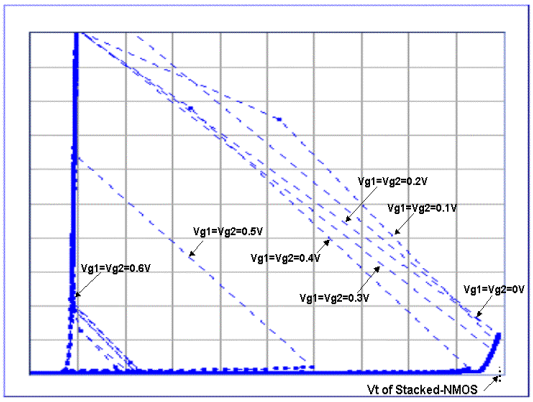


Fig. 4 The measured I-V curves of the fabricated SNTSCR devices with C=0.5μm and L1=L2=0.35μm under different gate biases (X-axis: 1V/div; Y-axis: 1mA/div).

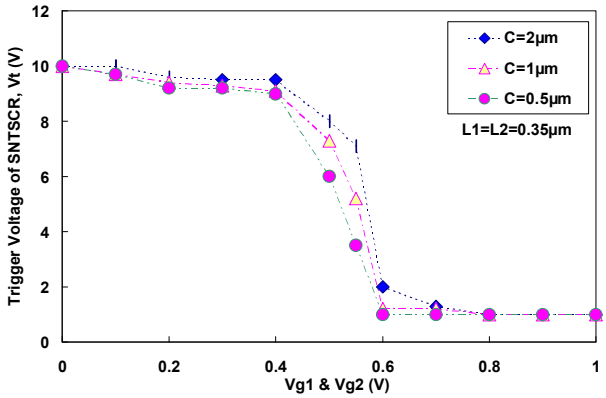


Fig. 5 Dependence of the trigger voltage on the gate bias voltage of the SNTSCR devices with different layout spacing C (where L1=L2 is fixed at 0.35μm).

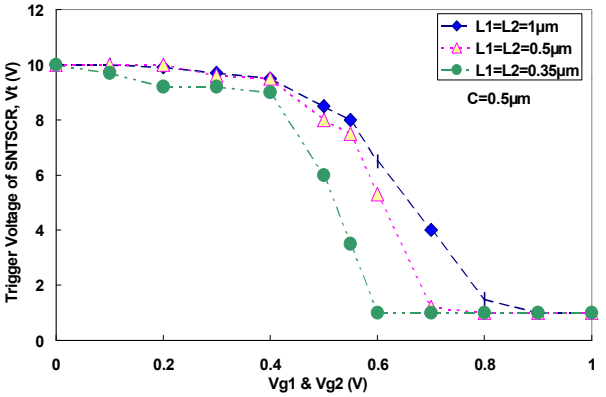


Fig. 6 Dependence of the trigger voltage on the gate bias voltage of the SNTSCR devices with different layout parameters of L1 and L2 (where C is fixed at 0.5μm).

The other impacts of layout parameters and gate biases on the ESD level of the SNTSCR device are measured and summarized in Fig. 7 and Fig. 8. The failure criterion is defined at the leakage current greater than 1 μA under the voltage bias of 5V. The HBM ESD robustness of the SNTSCR device is slightly degraded when the layout parameters C, L1, and L2 are increased. With shorter layout parameters (C, L1, and L2), the SNTSCR device has a shorter anode-to-cathode spacing, which implies a smaller turn-on resistance. Therefore, the SNTSCR device drawn with shorter layout parameters (C, L1, and L2) has a higher ESD level. The gate biases on Vg1 and Vg2 do not obviously improve ESD level of the SNTSCR device as those shown in Fig. 7 and Fig. 8, but it can trigger on the SNTSCR earlier to discharge the ESD current. Thus, the SNTSCR device with suitable gate-biased design can effectively protect the mixed-voltage I/O circuits of CMOS ICs.

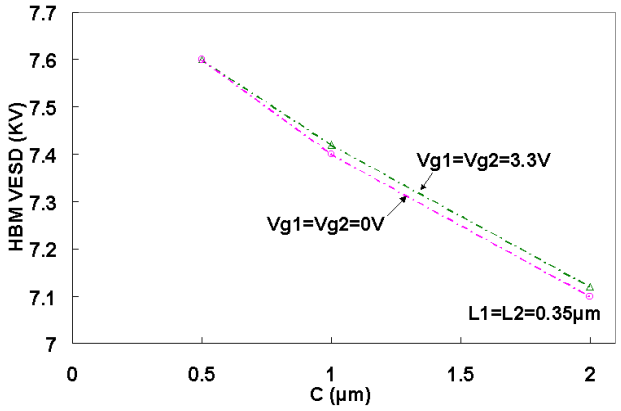


Fig. 7 Dependence of the HBM ESD level on the layout parameter C of the SNTSCR devices under different gate biases (Vg1=Vg2). Failure criterion : $I_{leakage}$ > 1μA @ Vbias = 5V.

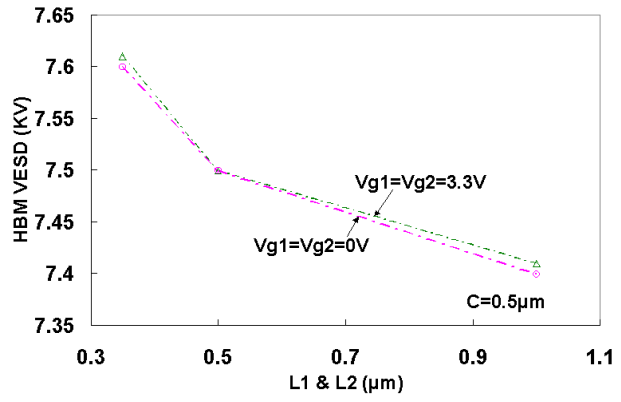


Fig. 8 Dependence of the HBM ESD level on the layout parameters L1 and L2 of the SNTSCR devices under different gate biases (Vg1=Vg2). Failure criterion : $I_{leakage}$ > 1μA @ Vbias = 5V.

III. On-Chip ESD Protection Design with the SNTSCR Device

Based on above experimental investigation on the SNTSCR device, the proposed ESD protection circuit with SNTSCR for protecting the mixed-voltage I/O circuits is shown in Fig. 9. An ESD detection circuit is designed to provide suitable gate biases to trigger on the SNTSCR device during the ESD-stress condition. On the contrary, this ESD detection circuit should keep the SNTSCR off, when the IC is under normal circuit operations. The ESD detection circuit, designed by using the gate-coupling technique with consideration on gate-oxide reliability issue, is shown in Fig. 10.

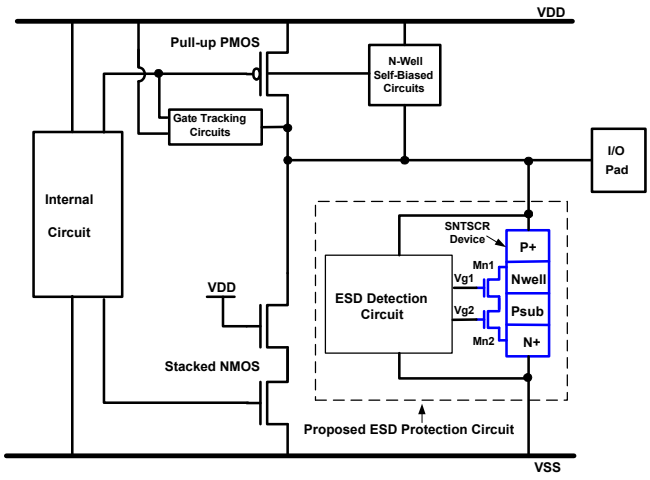


Fig. 9 The proposed ESD protection circuit with the SNTSCR device to protect the mixed-voltage I/O buffer.

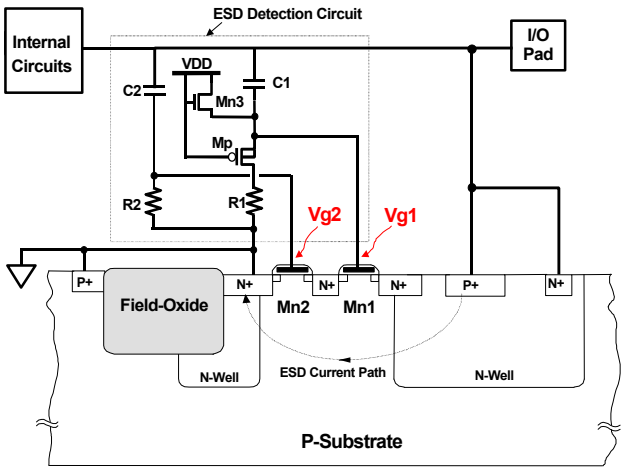


Fig. 10 The ESD detection circuit realized by the gate-coupling technique to trigger on the SNTSCR device.

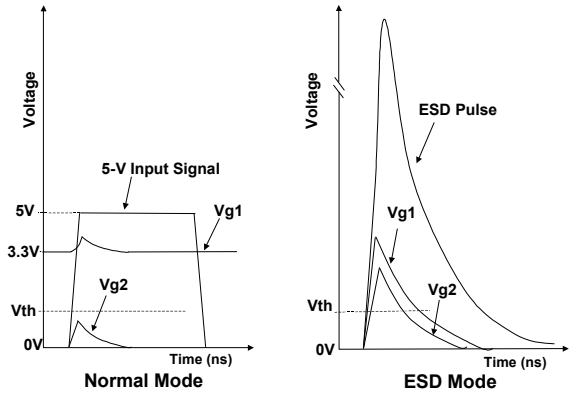


Fig. 11 The gate voltages on Vg1 and Vg2 of the SNTSCR device during normal circuit operating condition or ESD-stress condition in a 3V/5V-tolerant mixed-voltage I/O circuit.

A. Operating Principles

Fig. 11 shows the desired voltage waveforms of the gate biases (Vg1 & Vg2) provided by ESD detection circuit in the normal circuit operating condition and the ESD-stress condition in the 3V/5V-tolerant mixed-voltage I/O circuit.

In normal circuit operating condition, the SNTSCR is kept off, so that it does not interfere with the voltage levels of signals on the I/O pad. At such a normal state, the Mn3 in Fig. 10 acts as a resistor to bias the gate voltage of Mn1 at VDD. But, the gate of Mn2 is grounded through the resistor R2. When the I/O pad is applied with a high input voltage (5V), the center n+ region between Mn1 and Mn2 transistors has a voltage level about VDD-Vthn (Vthn is the threshold voltage of NMOS). So, all the devices in the ESD protection circuit can meet the limited electrical-field constraint of gate-oxide reliability during normal circuit operation condition. When the voltage of I/O pad transfers from 0V to 5V, the coupled gate voltage of Mn2 through the capacitor C2 is designed to be below the threshold voltage of NMOS. The coupled voltage through the capacitor C1 could also increase the gate voltage of Mn1, when the voltage on I/O pad transfers from 0V to 5V. The PMOS (Mp) in Fig. 10 is therefore designed to clamp the excessive voltage once the voltage of Mn1's gate increases to VDD+Vthp (Vthp is the magnitude of the threshold voltage of Mp). The corresponding voltage waveforms on Vg1 and Vg2 are illustrated in Fig. 11, when the voltage on I/O pad transfers from 0V to 5V. By suitable design on the ESD detection circuit, the SNTSCR can be kept off under normal circuit operating condition. Moreover, the PMOS (Mp) can further clamp the gate voltage of Mn1 to ensure gate oxide reliability on Mn1, even if the I/O pad has a high input voltage level.

During the positive-to-VSS ESD-stress condition, a positive high ESD voltage is applied to the I/O pad with VSS grounded but VDD floating. In this ESD-stress condition, the gate of Mp is grounded since the initial voltage level on the floating VDD power line is ground. So, the Mp is turned on, but the Mn3 is off. The capacitors, C1 and C2, are designed to couple ESD transient voltage from the I/O pad to the gates of Mn1 and Mn2, respectively. The coupled voltage should be designed higher than the threshold voltage to turn on Mn1 and Mn2 for triggering the SNTSCR device on, before the devices in the mixed-voltage I/O circuit is damaged by ESD energy. When the SNTSCR is triggered on, the ESD current is mainly discharged from the I/O pad to VSS through this SNTSCR device. The characteristics of lower trigger voltage and low holding voltage of the gate-coupling SNTSCR device can safely protect the thin gate oxide in the mixed-voltage I/O circuits, and sustain a high ESD level within a smaller silicon area.

B. Design of the ESD Detection Circuit

The purpose of the ESD detection circuit is to provide the suitable gate biases for the SNTSCR device under the normal circuit operating and ESD-stress conditions. To obtain the suitable gate biases, it is important to determine the values of the coupling capacitors (C1 and C2) and the sustaining resistors (R1 and R2). Based on above operational principles, the suitable values of C1, C2, R1, and R2 to meet the desired circuit operation in different CMOS processes can be adjusted and finely tuned by using *HSPICE* simulation.

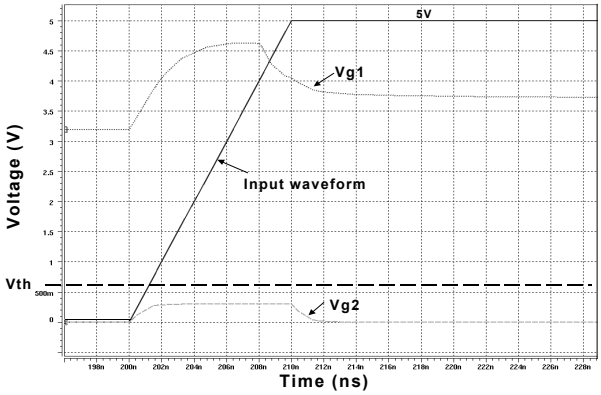
The dependence between the coupling capacitance and the sustaining resistance can be investigated by *HSPICE* simulation with different turn-on time period on Mn1 and Mn2. A 0-to-5V input waveform with a rise time of 10ns is used to simulate a 5-V input signal applied to the I/O pad, when the mixed-voltage I/O circuit is under normal circuit operating condition with VDD bias of 3.3V. The *HSPICE*-simulated voltage waveforms on Vg1 and Vg2 are shown in Fig. 12(a), when the C1=C2 is chosen at 20 fF and the R1=R2 is chosen at 130 kohm. The coupled voltage on Vg2 in Fig. 12(a) is smaller than Vthn (~0.6V), therefore the SNTSCR is not triggered on. The coupled voltage on Vg1 is further limited to ~3.8V after the rising transition of the input 5-V signal, which is clamped by the PMOS Mp in Fig. 10.

The SNTSCR device should be triggered on by the ESD detection circuit under ESD-stress condition, before the devices in the mixed-voltage I/O circuit are broken down by the overstress ESD voltage. A 0-

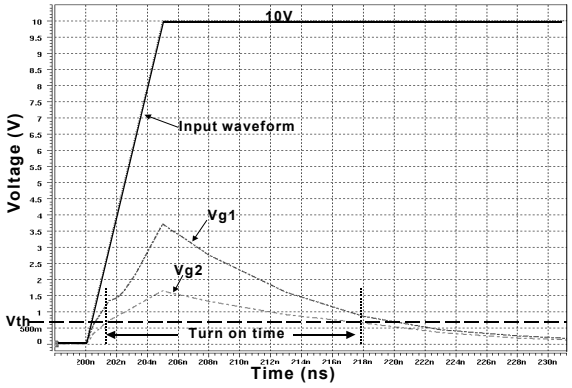
to-10V ramp voltage waveform with a rise time of 5ns is therefore used to simulate the rising transition of ESD voltage, before the mixed-voltage I/O circuit is broken down by ESD voltage. Under positive-to-VSS ESD-stress condition, VDD is floating with an initial voltage level of 0V. The *HSPICE*-simulated voltage waveforms on Vg1 and Vg2 under such an ESD-stress condition are shown in Fig. 12(b), when the C1=C2 (R1=R2) is still kept at 20 fF (130 kohm). The coupled voltage on Vg1 and Vg2 in Fig. 12(b) are both greater than Vthn (~0.6V). From the measured results shown in Fig. 4 ~ Fig. 6, the SNTSCR is turned on when the Vg1 and Vg2 are greater than 0.6V. Therefore, the SNTSCR can be triggered on to discharge ESD current before the mixed-voltage I/O circuit is broken down by ESD voltage.

To further investigate the dependence between the coupling capacitors (C1, C2) and sustaining resistors (R1, R2) to trigger on the SNTSCR device under ESD-stress condition, a turn-on time is further defined in Fig. 12(b) as the time period when the coupled voltages on Vg1 and Vg2 are both greater than the NMOS threshold voltage (Vthn) under such a 0-to-10V rising transition. In Fig. 12(b), the turn-on time is found as 20ns. This turn-on time can be further adjusted by changing the coupling capacitors and sustaining resistors in the ESD detection circuit. The values of the coupling capacitors (C1, C2) and sustaining resistors (R1, R2) are changed and simulated by *HSPICE* to choose the suitable R and C values for different required turn-on times.

Fig. 13 depicts the simulated results on the relation between coupling capacitance (C1=C2) and sustaining resistance (R1=R2) under two different turn-on times (10ns and 20ns). The turn-on time can be kept the same by using different values of the coupling capacitance and sustaining resistance. This leads to a more feasible design to realize the ESD detection circuit in different CMOS processes. To obtain a longer turn-on time, the R1 (R2) and C1 (C2) have to be designed with larger values. But, with too larger R1 (R2) and C1 (C2), the SNTSCR could be also trigged on by the normal 0-to-5V input signals under the normal circuit operating condition. Therefore, there is a design boundary to choose suitable R1 (R2) and C1 (C2) to meet the desired operating principles as those described in the Section III-A. Such a design boundary on the coupling capacitance and sustaining resistance can be found by *HSPICE* simulation, which is shown by the dashed line in Fig. 13. The over design region in Fig. 13 means that the coupling capacitance is over designed in the ESD detection circuit, which will cause the unexpected turn-on of SNTSCR under the normal 5-V input operation. So, the coupling capacitance and sustaining resistance located in the over design region is not suitable for practical applications. From Fig. 13 with the design boundary, the coupling capacitance and sustaining resistance in ESD detection circuit can be correctly chosen to meet the desired operating principles for a given CMOS process.



(a)



(b)

Fig. 12 The HSPICE-simulated results under (a) the normal circuit operating condition with a 5-V input signal, and (b) the ESD-stress condition with a 10-V rising voltage, on the I/O pad.

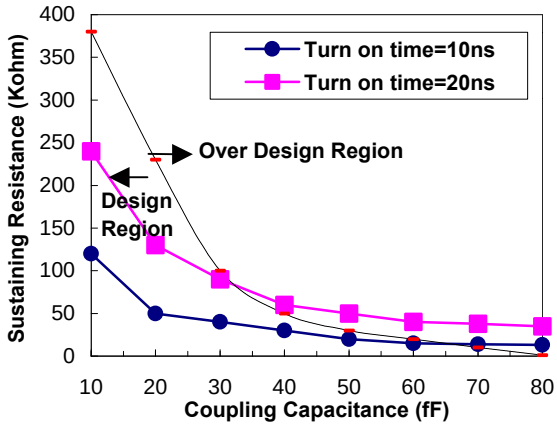


Fig. 13 HSPICE-simulated results on the relation between the coupling capacitance (C1=C2) and the sustaining resistance (R1=R2) under different turn-on times.

C. Improved Design Region for R and C

As shown in Fig. 13, the design region for choosing the suitable sustaining resistance and coupling capacitance to meet the desired operating principles of the ESD detection circuit only has a small design window. When realized in a practical CMOS IC, such a design window will become smaller due to the influence of process variation on the sustaining resistance and coupling capacitance.

To further improve the design region for easily choosing the suitable sustaining resistance and coupling capacitance, a modified design on the ESD detection circuit with an additional NMOS (Mn4) is shown in Fig. 14. The Mn4 is added across the sustaining resistor R2, which is located between the gate of Mn2 and VSS. The gate of Mn4 is connected to VDD. Under the normal circuit operating condition, Mn4 is always turned on to discharge the coupling voltage Vg2 below the threshold voltage (Vthn), and to keep the Mn2 always off. Therefore, the SNTSCR can be guaranteed off under the normal circuit operating condition.

Under the ESD-stress condition, Mn4 is off since the initial voltage level on the floating VDD power line is ground. The voltage (Vg2) coupled to the gate of Mn2 is determined by the sustaining resistance (R2) and the coupling capacitance (C2). Therefore, the suitable design region for the sustaining resistance and coupling capacitance of this modified ESD detection circuit can be obviously improved. The sustaining resistance and coupling capacitance of this modified ESD detection circuit to have the desired turn-on times of 10 or 20ns are simulated and shown in Fig. 15, where all the region is suitable for choosing the sustaining resistance and coupling capacitance.

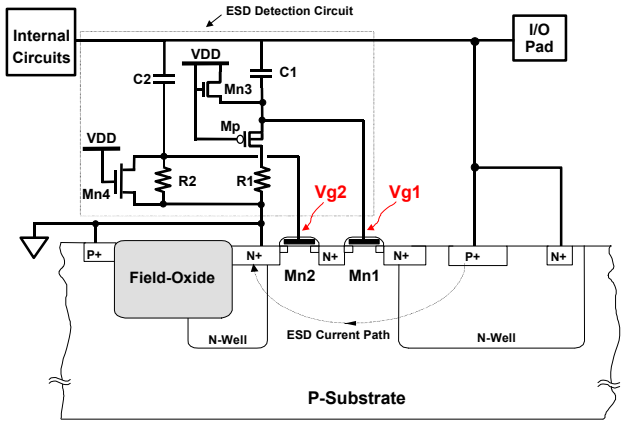


Fig. 14 The modified design on the ESD detection circuit with the SNTSCR device to have a larger design region on the sustaining resistance and coupling capacitance for protecting the mixed-voltage I/O buffer.

With a device dimension (W/L) of only 10μm/0.35μm for Mn4, the Vg1 and Vg2 voltage waveforms in this modified circuit, under normal circuit operating condition with a 5-V input signal applied to the I/O pad, is simulated and shown in Fig. 16, where the input signal has a rise time of only 1ns. As seen in Fig. 16, even if the rise time of the 5-V input signal is as short as 1ns, the coupled Vg2 voltage waveform during the input transition can be kept always smaller than its Vth. Therefore, the SNTSCR can be guaranteed off under the normal circuit operating condition by this modified circuit design. By only adding Mn4 into the ESD detection circuit, it becomes very easy to determine the suitable values for the coupling capacitance (C1 and C2) and the sustaining resistance (R1 and R2).

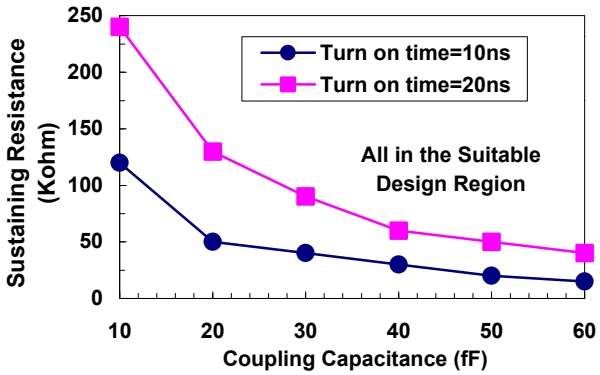


Fig. 15 HSPICE-simulated results on the relation between the coupling capacitance (C1=C2) and the sustaining resistance (R1=R2) under different turn-on times of the modified ESD detection circuit in Fig. 14 to have a wide design region.

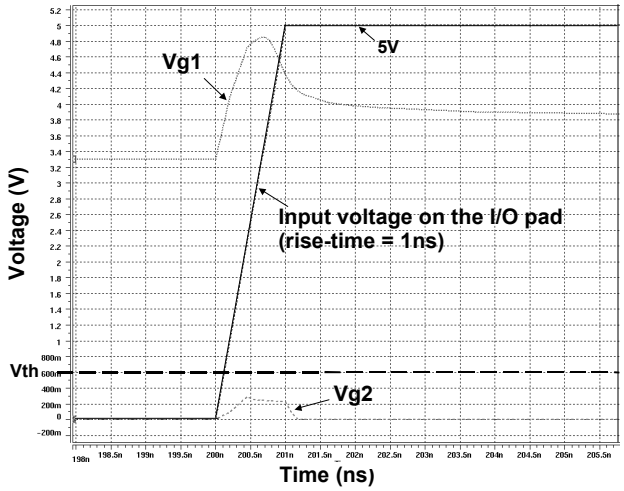


Fig. 16 The HSPICE-simulated voltage waveforms on Vg1 and Vg2 in the modified circuit of Fig. 14, under normal operating condition with a 5-V input signal of 1-ns rise time on the I/O pad.

D. Modified Design to Improve Noise Margin of SNTSCR

When the mixed-voltage I/O buffer is under normal circuit operating condition with a high voltage input signal, the overshooting noise pulse generated from the external circuits or interfaces could be coupled into the I/O pad to accidentally trigger on the SNTSCR in the ESD protection circuit [23]-[26]. To further improve noise margin of the SNTSCR device in the ESD protection circuit without being accidentally triggered on during the normal circuit operating condition, a further modified design is shown in Fig. 17. The ESD detection circuit is connected from the self-biased N-well of the pull-up PMOS, where the parasitic drain-to-bulk diode Dp between the I/O pad and the N-well essentially exists in the PMOS device structure.

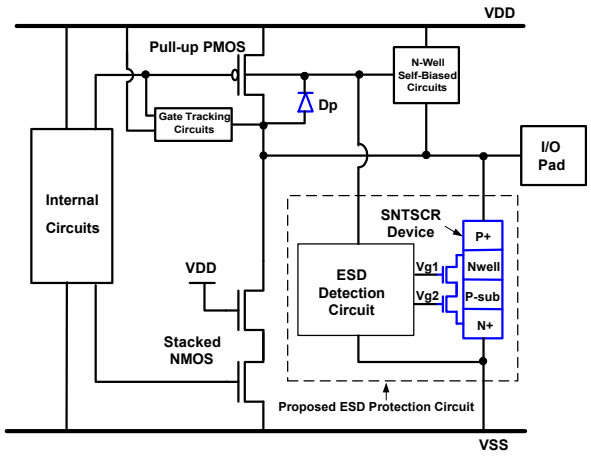


Fig. 17 The modified deign of the ESD protection circuit with the SNTSCR device for the mixed-voltage I/O buffer to have a higher noise margin to the I/O signals.

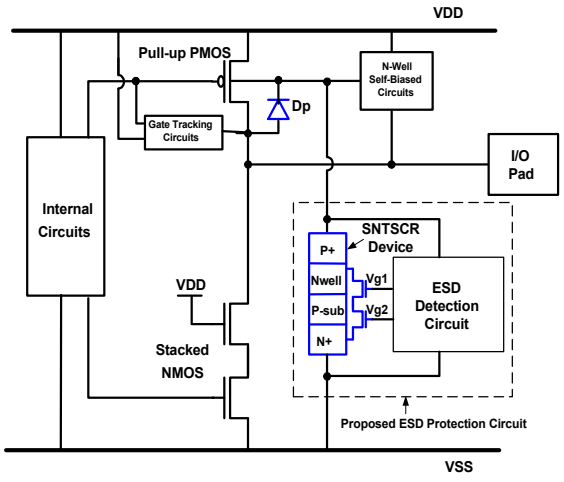


Fig. 18 The modified design of the ESD protection circuit with the SNTSCR device for the mixed-voltage I/O buffer to have no extra additional parasitic capacitance to the I/O pad.

Only the noise, higher than the voltage level of the N-well pulsing the cut-in voltage of a diode, can reach to the ESD detection circuit. Therefore, this modified ESD protection design not only has a high ESD level, but also a better noise margin to the input signals on the I/O pad with overshooting glitch.

Fig. 18 shows another modified connection on the ESD protection circuit with the SNTSCR device to protect the mixed-voltage I/O buffer. The main difference between the circuit connections in Fig. 18 and Fig. 9 is that the anode of the SNTSCR device and the ESD detection circuit are connected to the self-biased N-well of the pull-up PMOS in Fig. 18. With this modified connection, the ESD protection circuit with the SNTSCR device also has a higher noise margin to the overshooting glitch at the I/O pad, during the normal circuit operating condition. Under the positive-to-VSS ESD-stress condition, the ESD current first flows through the parasitic diode Dp to the floating N-well of the pull-up PMOS, and then is discharged to VSS through the turned-on SNTSCR device. The main purpose of this modified connection on the ESD protection circuit is to provide the mixed-voltage I/O buffer with a higher ESD robustness but no extra additional parasitic capacitance to the I/O pad. The coupling capacitance (C1 and C2) in the ESD detection circuit and the parasitic junction capacitance in the SNTSCR device are blocked from the I/O pad by the drain-to-bulk diode Dp in the pull-up PMOS.

IV. Experimental Results

The experimental test chip has been fabricated in a 0.35-μm silicided CMOS process. A practical layout example of the proposed ESD protection circuit including a mixed-voltage I/O buffer is shown in Fig. 19. There is a thin-oxide pull-up PMOS (pull-down stacked-NMOS) device placed between the I/O pad and VDD (VSS). The capacitors (C1 and C2), resistors (R1 and R2), Mp, and Mn3 are composed of the ESD detection circuit for providing suitable gate biases to the SNTSCR device. Capacitor C1 (C2) is designed to couple suitable ESD-transient voltage to the gate of Mn1 (Mn2) to lower snapback-trigger voltage of the SNTSCR device. Resistor R1 (R2) is designed to sustain the coupled voltage longer in time on the gate of Mn1 (Mn2) to trigger the SNTSCR device into its snapback region. In Fig. 19, C1 and C2 are realized by inserting the polysilicon layer right under the metal bond pad without increasing extra layout area to the I/O circuit. Their capacitance can be adjusted by changing the different overlap area

between polysilicon layer and metal bond pad. R1 and R2 are realized by the N-well resistance, and their resistance can be adjusted by changing different length of the N-well region.

The leakage current under normal circuit operating condition is a concern for an ESD protection circuit connected to an I/O pin. The leakage currents of the fabricated mixed-voltage I/O buffers with or without the proposed ESD protection circuit are measured and compared in Fig. 20. The leakage current is measured (using an HP4155) by applying a voltage ramp from 0V to 5V to the I/O pad under the bias condition of 3.3-V VDD and 0-V VSS. In Fig. 20, the maximum leakage current of the mixed-voltage I/O buffer without (with) the proposed ESD protection circuit under 5-V bias at the I/O pad is 175 (215) pA. The increase of the leakage current by adding the ESD protection circuit is only 40 pA, whereas the SNTSCR device in the ESD protection circuit is drawn with a device width of 60μm.

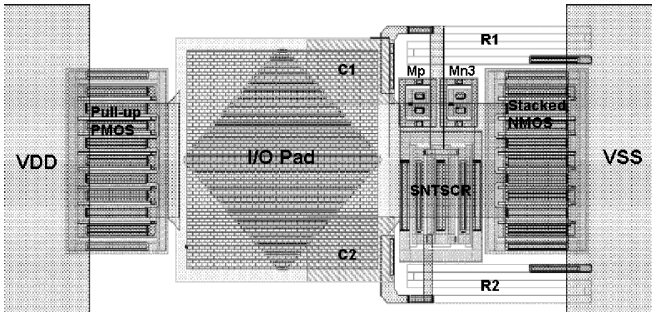


Fig. 19 A practical layout example of a mixed-voltage I/O buffer with the proposed ESD protection circuit realized in a 0.35-μm CMOS process.

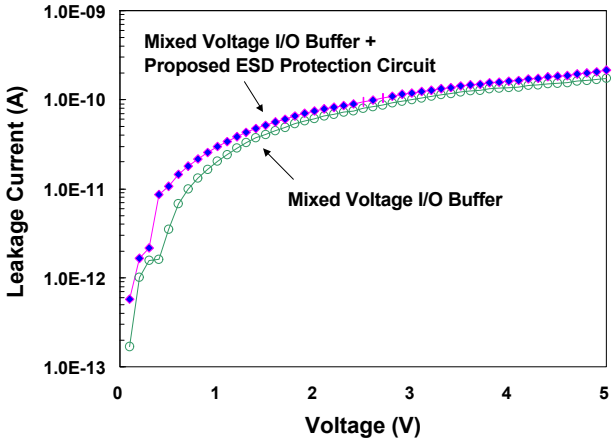


Fig. 20 Comparison on the leakage current of the mixed-voltage I/O buffers with or without the proposed ESD protection circuit. The mixed-voltage I/O buffer in this measurement has a channel width of 180μm in the stacked-NMOS and a channel width of 360μm in the pull-up PMOS.

The positive-to-VSS human-body-model (HBM) ESD levels of the mixed-voltage I/O buffers with or without the proposed ESD protection circuit are measured and compared in Fig. 21. The mixed-voltage I/O buffers with different stacked-NMOS channel widths are also tested as a reference. The HBM ESD level of the mixed-voltage I/O buffer (with stacked-NMOS channel width of 120μm) can be obviously improved from the original ~2kV to become greater than 8kV by the proposed ESD protection circuit with the SNTSCR device.

The TLPG (transmission line pulse generator) with a pulse width of 100ns is also used to verify the secondary breakdown current (It2) of the mixed-voltage I/O buffers with or without the proposed ESD protection circuit, and the measured results are shown in Fig. 22. The It2 of the stacked NMOS with channel width of 180μm is around 2A, but it can be increased up to ~7A by the proposed ESD protection circuit with the SNTSCR device of 60μm. The measured It2 values are consistent to the HBM ESD level with a factor around 1.5 kohm. This has further verified the effectiveness of the proposed ESD protection circuit with the SNTSCR device.

The positive-to-VSS machine-model (MM) ESD levels of the mixed-voltage I/O buffers with or without the proposed ESD protection circuit are also measured and compared in Fig. 23. The mixed-voltage I/O buffers with different stacked-NMOS channel widths are also tested as a reference. From the measured results, the MM ESD level of the mixed-voltage I/O buffer with a channel width of 120μm in the stacked NMOS can be significantly improved from the original ~200V to become ~800V by the proposed ESD protection circuit.

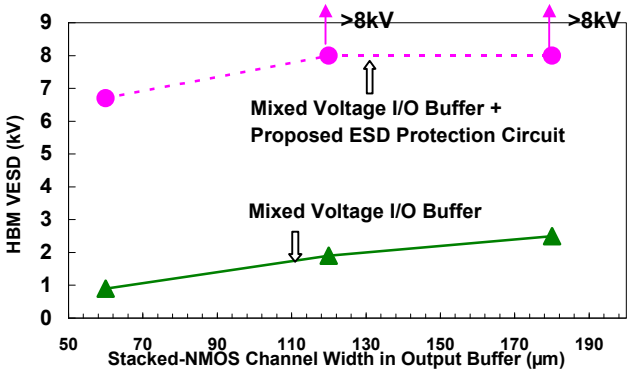


Fig. 21 Comparison on the HBM ESD robustness of the mixed-voltage I/O buffers with or without the proposed ESD protection circuit, under different channel widths of the stacked NMOS in the mixed-voltage I/O buffers.

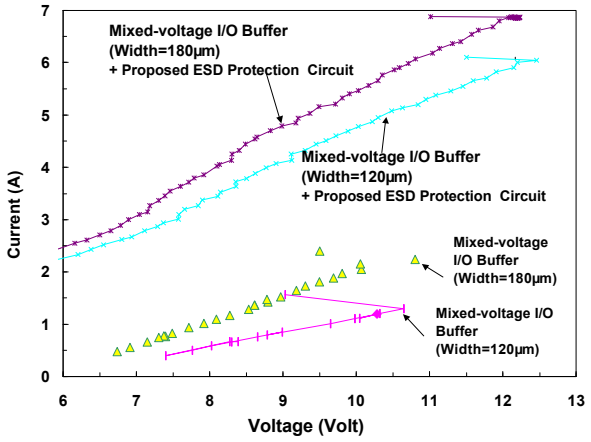


Fig. 22 Comparison on the TLPG-measured I-V curves of the mixed-voltage I/O buffers with or without the proposed ESD protection circuit, under different channel widths of the stacked NMOS in the mixed-voltage I/O buffers.

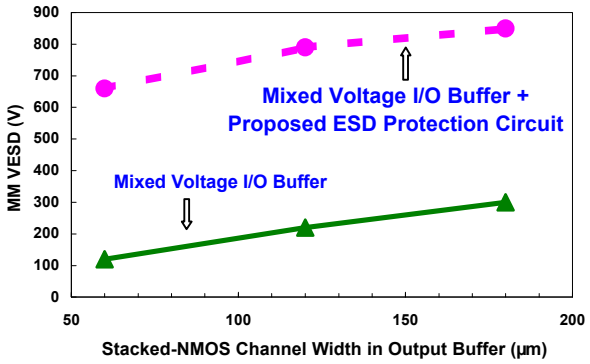
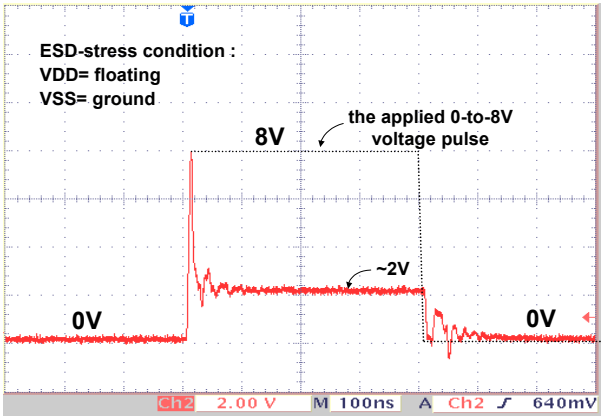


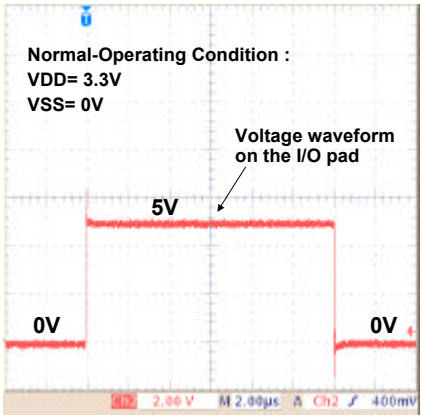
Fig. 23 Comparison on the machine-model (MM) ESD robustness of the mixed-voltage I/O buffers with or without the proposed ESD protection circuit, under different channel widths of the stacked NMOS in the mixed-voltage I/O buffers.

To verify the turn-on efficiency of the proposed ESD protection circuit, a 0-to-8V sharply rising voltage pulse is applied to the I/O pad when VSS is relatively grounded but VDD is floating. The stacked NMOS in the output buffer has a snapback breakdown voltage of ~10V. Such a 0-to-8V voltage pulse applied to the I/O pad does not break down the stacked NMOS of the output buffer. But, the 0-to-8V voltage pulse can trigger on the ESD protection circuit to cause a degraded voltage waveform, as that shown in Fig. 24(a), which is clamped by the turned-on SNTSCR device. In the normal circuit operating condition, a 0-to-5V input voltage pulse is applied to the I/O pad with the VDD (VSS) biased at 3.3V (0V). But, the voltage waveform is not degraded, as that shown in Fig. 24(b). So, the SNTSCR device is not triggered on by the normal input signals of 5V.

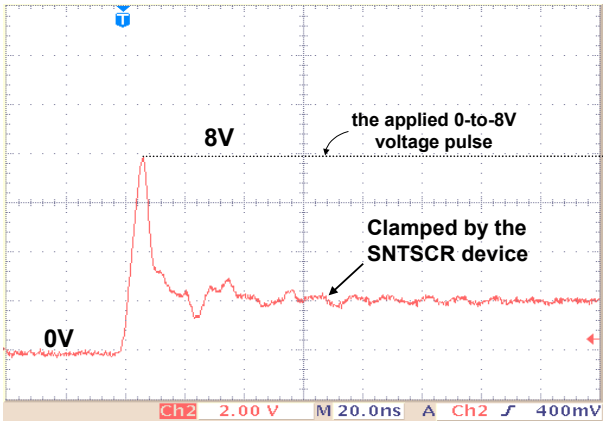
The sharply rising edge of the 0-to-8V voltage pulse in Fig. 24(a) is zoomed in Fig. 24(c), where the applied 0-to-8V voltage pulse is clamped to ~2V by the SNTSCR device. The transition time of ~10ns from 8V to 2V in Fig. 24(c) is the corresponding turn-on speed of the SNTSCR device realized in a 0.35-μm CMOS process. The degraded voltage waveform has further verified the effectiveness of the proposed ESD protection circuit to protect the mixed-voltage I/O circuits.



(a)



(b)



(c)

Fig. 24 The measured voltage waveforms on the I/O pad, triggered by (a) a 0-to-8V, and (b) a 0-to-5V, voltage pulses. The rising edge in (a) of the 0-to-8V voltage pulse clamped by the SNTSCR device is zoomed in (c).

V. Conclusion

A new ESD protection circuit, by using the stacked-NMOS triggered silicon controlled rectifier (SNTSCR) device, has been successfully verified in a 0.35-μm CMOS process. The I-V characteristics of the SNTSCR device with different gate biases and the turn-on behaviors of the ESD protection circuit have been measured to verify its effectiveness. By using ESD detection circuit with suitable design on the coupling capacitance and sustaining resistance, the SNTSCR device can be fully triggered on within 10~15 ns to discharge ESD current. By changing the connection of the ESD protection circuit from the I/O pad to the floating N-well of the pull-up PMOS in the mixed-voltage I/O circuit, the SNTSCR device has a high enough noise margin to the overshooting glitch on the I/O pad, during the normal circuit operating condition. The leakage current by adding this new ESD protection circuit to the mixed-voltage I/O buffer is only increased 40 pA. This new proposed ESD protection circuit is fully process-compatible to general sub-quarter-micron CMOS processes for effectively protecting the mixed-voltage interface circuits on the input and output pins.

References

[1] T. Furukawa, D. Turner, S. Mittl, M. Maloney, R. Serafin, W. Clark, J. Bialas, L. Longenbach and J. Howard, "Accelerated gate-oxide breakdown in mixed-voltage I/O circuits," in *Proc. of IEEE Int. Reliability Physics Symp.*, 1997, pp. 169-173.

[2] E. Takeda and N. Suzuki, "An empirical model for device degradation due to hot-carrier injection," *IEEE Electron Device Letters*, vol. 4, pp. 111-113, 1983.

[3] S. H. Voldman, "ESD protection in a mixed voltage interface and multi-rail disconnected power grid environment in 0.5- and 0.25-μm channel length CMOS technologies," in *Proc. of EOS/ESD Symp.,* 1994, pp. 125-134.

[4] S. Dabral and T. J. Maloney, *Basic ESD and I/O Design*, John Wiley & Sons, Inc., New York, 1998.

[5] M. Hargrove, *et al*., "High-performance sub-0.08 μm CMOS with dual gate oxide and 9.7 ps inverter delay," in *Tech. Dig. of IEEE Int. Electron Devices Meeting*, 1998, pp. 22.4.1-22.4.4.

[6] S. Poon, *et al*., "A versatile 0.25-micron CMOS technology," in *Tech. Dig. of IEEE Int. Electron Devices Meeting*, 1998, pp. 28.2.1-28.2.4.

[7] M. Takahash, T. Sakurai, K. Sawada, K. Nogami, M. Ichida, and K. Matsud, "3.3V-5V compatible I/O circuit without thick gate oxide," in *Proc. of IEEE Custom Integrated Circuits Conference*, 1992, pp. 23.3.1–23.3.4.

[8] M. Pelgrom and E. Dijkmans, "A 3/5 V compatible I/O buffer," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 823-825, 1995.

[9] J. Conner, D. Evans, G. Braceras, J. Sousa, W. Abadeer, S. Hall, and M. Robillard, "Dynamic dielectric protection for I/O circuits fabricated in a 2.5-V CMOS technology interfacing to a 3.3-V LVTTL bus," in *Tech. Dig. of Int. Symp. on VLSI Circuits*, 1997, pp. 119-120.

[10] G. Singh and R. Salem, "High-voltage-tolerant I/O buffers with low-voltage CMOS process," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 1512-1525, 1999.

[11] H. Sanchez, J. Siegel, C. Nicoletta, J. Nissen, and J. Alvarez, "A versatile 3.3/2.5/1.8-V CMOS I/O driver built in a 0.2-μm 3.5-nm Tox 1.8-V CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 1501-1511, 1999.

[12] A-J Annema, G. Geelen, and P. de Jong, "5.5-V I/O in a 2.5-V 0.25-μm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 528-538, 2001.

[13] T. Maloney and W. Kan, "Stacked PMOS clamps for high voltage power supply protection," in *Proc. of EOS/ESD Symp.*, 1999, pp. 70-77.

[14] W. Anderson and D. Krakauer, "ESD protection for mixed-voltage I/O using NMOS transistors stacked in a cascode configuration," in *Proc. of EOS/ESD Symp.*, 1998, pp. 54-71.

[15] J. Miller, M. Khazhinsky, and J.Weldon, "Engineering the cascoded NMOS output buffer for maximum Vt1," in *Proc. of EOS/ESD Symp.*, 2000, pp. 308-317.

[16] T. J. Maloney and S. Dabral, "Novel clamp circuits for IC power supply protection," in *Proc. of EOS/ESD Symp.*, 1995, pp. 1-12.

[17] S. H. Voldman, G. Gerosa, V. Gross, N. Dickson, S. Furkay, and J. Slinkman, "Analysis of snubber-clamped diode-string mixed voltage interface ESD protection network for advanced microprocessors," in *Proc. of EOS/ESD Symp.*, 1995, pp. 43-61.

[18] T. J. Maloney, K. Parat, N. Clark, and A. Darwish, "Protection of high voltage power and programming pins," in *Proc. of EOS/ESD Symp.*, 1997, pp. 246-254.

[19] M-D Ker and W-Y Lo, "Design on the low-leakage diode string for using in the power-rail ESD clamp circuits in a 0.35-μm silicide CMOS process," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 601-611, 2000.

[20] A. Chatterjee and T. Polgreen, "A low-voltage triggering SCR for on-chip ESD protection at output and input pads," *IEEE Electron Device Letters*, vol. 12, pp. 21-22, 1991.

[21] M-D Ker, C-Y Wu, and H-H Chang, "Complementary-LVTSCR ESD protection circuit for submicron CMOS VLSI/ULSI," *IEEE Trans. on Electron Devices*, vol. 43, pp. 588-598, 1996.

[22] M-D Ker, H.-H. Chang, and C.-Y. Wu, "A gate-coupled PTLSCR/NTLSCR ESD protection circuit for deep-submicron low-voltage CMOS IC's," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 38-51, 1997.

[23] M. Corsi, R. Nimmo, and F. Fattori, "ESD protection of BiCMOS integrated circuits which need to operate in the harsh environments of automotive or industrial," in *Proc. of EOS/ESD Symp.*, 1993, pp. 209-213.

[24] M-D Ker, "ESD protection for CMOS ASIC in noisy environments with high-current low-voltage triggering SCR devices," in *Proc. of IEEE Int. ASIC/SOC Conference*, 1997, pp. 283-286.

[25] G. Notermans, F. Kuper, and J. M. Luchis, "Using an SCR as ESD protection without latch-up danger," *Journal of Microelectronics Reliability*, vol. 37, pp.1457-1460, 1997.

[26] M-D Ker and H-H Chang, "How to safely apply the LVTSCR for CMOS whole-chip ESD protection without being accidentally triggered on," in *Proc. of EOS/ESD Symp.*, 1998, pp. 72-85.