Design and Analysis of the On-Chip ESD Protection Circuit with a Constant Input Capacitance for High-Precision Analog Applications

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Abstract

An on-chip ESD protection design is proposed to solve the ESD protection challenge to the analog pins for high-precision applications. A design model to find the optimized device dimensions and layout spacings on the input ESD clamp devices has been developed to keep the total input capacitance almost constant (within 1% variation), even if the analog signal has an input dynamic range of 1V. The device dimension (W/L) of ESD clamp device connected to the I/O pad in the analog ESD protection circuit can be reduced to only 50/0.5 (μm/μm) in a 0.35-μm silicided CMOS process, but it can sustain the HBM (MM) ESD level of up to 6kV (400V). With such a smaller device dimension, the input capacitance of this analog ESD protection circuit can be significantly reduced to only ~1.0 pF (including the bond pad capacitance) for high-frequency applications.

1. Introduction

Due to the low breakdown voltage of the gate oxide in deep-submicron CMOS technologies, efficient electrostatic discharge (ESD) protection circuits should be designed and placed on all pins of an IC to clamp the ESD overstress voltage [1]-[3]. A traditional ESD protection design with the two-stage structure for digital input pin is shown in Fig.1, where a gate-grounded NMOS (ggNMOS) is used as the secondary protection device to clamp the overstress voltage across the gate oxide of the input circuits. Between the primary stage and the secondary stage of the input ESD protection circuit, a resistor is added to limit the ESD current flowing through the short-channel NMOS in the secondary stage. The resistance should be large enough (in the order of kΩ [1]), so the primary ESD clamp device can be triggered on to bypass ESD current before the ggNMOS in the secondary stage was damaged by the overstress ESD current. But the large series resistance and the large junction capacitance in the ESD clamp devices cause a long *RC* timing delay to the input signals, it is not suitable for analog pins, especially for the high-frequency or RF applications.

For some high-precision circuit operations, the input capacitance of an analog input pin is required to be kept as a constant as possible within the input voltage range. A major distortion in high-speed analog circuits, especially in the single-ended input implementations, is the voltage-dependent nonlinear input capacitance associated with the ESD clamp devices at the analog input pad. The typical degradation on the circuit performance due to the nonlinear input capacitance of the input ESD clamp devices had been reported in [4], where the input capacitance varying from 4pF to 2pF due to the input voltage swing from 0V to 2V caused an increase on the harmonic distortion in an analog-to-digital converter (ADC) and therefore degraded the precision of the ADC from 14-bit to become only 10-bit. Therefore, for high-precision analog applications, the input capacitance generated from the input ESD clamp devices on the pad is required to be kept as constant as possible.

In this paper, an on-chip ESD protection design with the advantages of small and constant input capacitance, no series resistance, and high ESD level is proposed for high-precision analog applications. A design model to optimize the device dimensions and layout spacings of the ESD clamp devices has been developed to keep the input capacitance almost constant.

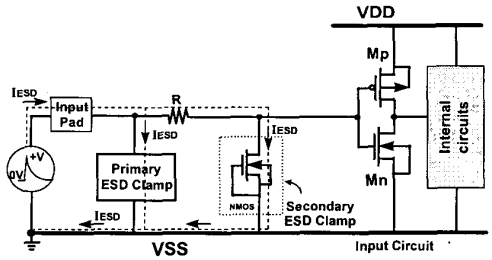

Fig.1 A schematic diagram of the traditional two-stage ESD protection circuit for digital input pin in CMOS IC's.

2. ESD Protection Circuit for Analog Pin

2.1 Circuit Configuration and Operation

The proposed ESD protection circuit for analog pins is shown in Fig. 2, whereas its practical layout in a 0.35-μm silicide CMOS cell library is drawn in Fig.3. In order to reduce the input capacitance of the analog pin, the Mn1 and Mp1 are both designed with a much smaller device dimension of only 50/0.5 (μm/μm) in Fig.2.

To avoid the small Mn1 and Mp1 into the drain-breakdown condition in the PS-mode and ND-mode ESD stresses [5]-[6] to cause a much low ESD level, an efficient ESD clamp circuit between the power rails is co-constructed into the analog ESD protection circuit to increase the overall ESD level. In Fig.2, the *RC*-based ESD detection circuit [6] is used to trigger on the Mn3 device,

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when the input pad is tested in the PS-mode or ND-mode ESD stresses. Because the Mn1 in the PS-mode (Mp1 in the ND-mode) ESD stress is not operated in the drain-breakdown condition, the ESD current is bypassed through the forward-biased drain diode Dp1 in Mp1 (Dn1 in Mn1), the VDD/VSS power rails, and the turned-on Mn3. The Mn3 is especially designed with a larger device dimension (1800/0.5 in Fig.8) to sustain a high ESD level. Although the large-dimension Mn3 has a large junction capacitance, this capacitance does not contribute to the input pad. Therefore, the analog pin can sustain much higher ESD level but only with a much smaller input capacitance.

In Fig.3, the drain-contact-to-poly-gate spacing in both Mn1 and Mp1 is drawn as 3.4μm, whereas the source side spacing is drawn as 1.55μm. With both device dimensions of 50/0.5 in Mn1 and Mp1, the input junction capacitance is only varying from 0.37pF to 0.4pF when the voltage swing is from 0V to 3V. The layout size of the metal bond pad for wire bonding in the 0.35-μm CMOS process is specified as $96\times96\mu m^2$, which contributes a parasitic Cpad of 0.67pF. So, the total Cin of this analog ESD protection circuit including the bond pad is only about 1.04~1.07 pF, even if the input signal has different voltage level. With such a small and almost constant input capacitance, this proposed analog ESD protection circuit is more suitable for high-precision and high-frequency analog applications.

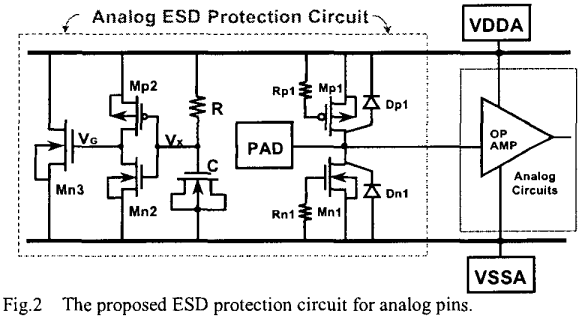


Fig.2 The proposed ESD protection circuit for analog pins.

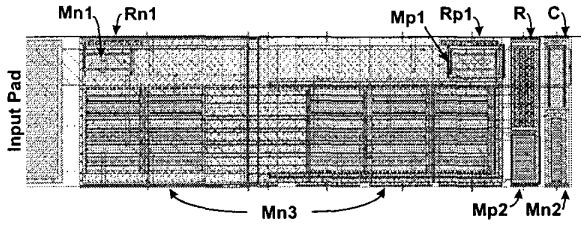


Fig.3 Layout example of the proposed ESD protection circuit for analog input pins in a 0.35-μm silicide CMOS process.

2.2 Experimental Result

This design has been practically fabricated in a 0.35-μm silicide CMOS process with an operational amplifier as its input circuit. Both the inverting and non-inverting input pins are protected by the proposed analog ESD protection circuit. The silicide-blocked mask is also used on the device Mn1, Mp1, and Mn3 to improve their ESD robustness. The HBM (human-body model) and MM (machine model) ESD testing results are summarized in Table I, which includes the analog pin-to-pin ESD stress. As shown in Table I, the proposed analog ESD protection circuit can successfully provide analog input pins with an HBM ESD level of above 6000V in each ESD-stress condition but only has a much smaller input capacitance.

Table I

	Pin Combination in ESD Test				
	PS-mode	NS-mode	PD-mode	ND-mode	Pin-to-Pin
HBM (V)	6000	- 8000	7000	- 7000	6000
MM (V)	400	- 400	400	- 400	400

3. Design on the Input Capacitance

3.1 The Input Capacitance

The input capacitance of this proposed analog ESD protection circuit can be calculated as :

$$Cin = Cpad + Cjp + Cjn\,, \qquad (1)$$

where the *Cpad* is the parasitic capacitance of the bond pad. The *Cjp* (*Cjn*) is the drain junction capacitance and the drain-to-gate overlapped capacitance in the Mp1 (Mn1). The main nonlinear source on the input capacitance is the bias-dependent junction capacitance at the drain regions of the Mn1 and Mp1 of the ESD protection circuit. With a complementary structure, the input capacitance can be kept almost constant if suitable layout dimensions and spacings are selected to draw the Mn1 and Mp1 devices.

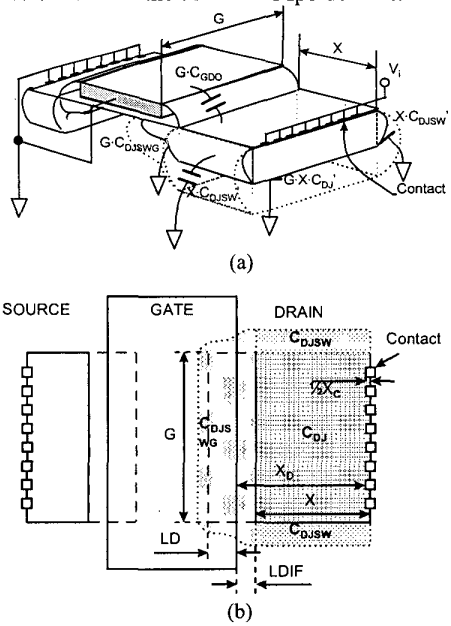


Fig.4 (a) The three-dimension structure of a finger-type MOS device. (b) The corresponding top-view layout of a finger-type MOS device with specified layout spacings.

The realization of the ESD clamp devices are generally drawn in the finger-type structure to save layout area of the I/O cells. The three-dimension structure of an finger-type NMOS (or PMOS) device is drawn in Fig.4(a), whereas the top view of device layout with the specified layout spacings is drawn in Fig.4(b). The device dimension and layout spacings of the finger-type NMOS (or PMOS) are also indicated in Fig.4.

Substituting the capacitance equations into (1) with the relative device parameters for Mn1 and Mp1 [7], the total input capacitance C_{in} of the proposed analog ESD protection circuit can be expressed as

$$C_{in} = C_{PAD} + k_n \cdot \left\{ G_n \cdot CGDO_n + G_n \cdot X_n \cdot CJ_n \left(1+\frac{V_i}{PB_n}\right)^{-MJ_n} + G_n \cdot CJSWG_n \left(1+\frac{V_i}{PBSWG_n}\right)^{-MJSWG_n} + 2 \cdot X_n \cdot CJSW_n \left(1+\frac{V_i}{PBSW_n}\right)^{-MJSW_n} \right\} + k_p \cdot \left\{ G_p \cdot CGDO_p + G_p \cdot X_p \cdot CJ_p \left(1+\frac{V_{DD}-V_i}{PB_p}\right)^{-MJ_p} + G_p \cdot CJSWG_p \left(1+\frac{V_{DD}-V_i}{PBSWG_p}\right)^{-MJSWG_p} + 2 \cdot X_p \cdot CJSW_p \left(1+\frac{V_{DD}-V_i}{PBSW_p}\right)^{-MJSW_p} \right\}$$

where (2)

k_n (k_p) is the finger number of the poly gate in the finger-type Mn1 (Mp1) layout;

G_n (G_p) is the finger length of the poly gate in the finger-type Mn1 (Mp1) layout;

X_n (X_p) is the layout spacing between the drain contact and the poly gat in the finger-type Mn1 (Mp1) layout; and

V_i is the input voltage level on the pad.

3.2 Layout Design to Minimize Capacitance Variation

When the layout spacings in Mn1 and Mp1 are modified, the total input capacitance of the proposed analog ESD protection circuit can be adjusted. The desired layout parameters to minimize the variation on the input capacitance within some input voltage range can be obtained from (2). If the value of the partial differential equation of (2) on the input voltage, $\partial C_{in}/\partial V_i$, is equal to zero, the input capacitance becomes independent to the input voltage level and the input capacitance can be kept as constant. Unfortunately, the layout parameters (K_n, K_p, G_n, G_p, X_n, and X_p) on the Mn1 and Mp1 devices with the HSPICE parameters in the 0.35-μm silicided CMOS process can not keep this $\partial C_{in}/\partial V_i$ term always zero, while the input signal has a voltage swing from 0V to VDD (3V).

In the analog applications, the analog input signal generally has a common reference voltage, indicated as V_{com} in this work. For the symmetrical analog input signals with a maximum amplitude of ΔV, the minimum (V_{min}) and maximum (V_{max}) voltage level of the analog input signals can be written as

$$V_{min} = V_{com} - \Delta V, \text{ and} \quad (3)$$

$$V_{max} = V_{com} + \Delta V. \quad (4)$$

According to the mean value theorem [8], if the input capacitance at the voltage levels of V_{min} and V_{max} are kept the same, the condition of $\partial C_{in}/\partial V_i=0$ is located within this analog input voltage range. Therefore, the input capacitance can have a minimized variation within the analog input voltage range between V_{min} and V_{max}. Substituting the V_{min} and V_{max} into (2), the condition of $C_{in}(V_{max}) = C_{in}(V_{min})$ to keep the minimum variation on the input capacitance can be obtained as

$$k_n \cdot \{\alpha \cdot G_n \cdot X_n + \beta \cdot G_n + 2 \cdot \gamma \cdot X_n\} = k_p \cdot \{\eta \cdot G_p \cdot X_p + \theta \cdot G_p + 2 \cdot \kappa \cdot X_p\}, \quad (5)$$

where

$$\alpha = CJ_n \left[\left(1+\frac{V_{min}}{PB_n}\right)^{-MJ_n} - \left(1+\frac{V_{max}}{PB_n}\right)^{-MJ_n} \right]$$

$$\beta = CJSWG_n \left[\left(1+\frac{V_{min}}{PBSWG_n}\right)^{-MJSWG_n} - \left(1+\frac{V_{max}}{PBSWG_n}\right)^{-MJSWG_n} \right]$$

$$\gamma = CJSW_n \left[\left(1+\frac{V_{min}}{PBSW_n}\right)^{-MJSW_n} - \left(1+\frac{V_{max}}{PBSW_n}\right)^{-MJSW_n} \right]$$

$$\eta = CJ_p \left[\left(1+\frac{V_{DD}-V_{max}}{PB_p}\right)^{-MJ_p} - \left(1+\frac{V_{DD}-V_{min}}{PB_p}\right)^{-MJ_p} \right]$$

$$\theta = CJSWG_p \left[\left(1+\frac{V_{DD}-V_{max}}{PBSWG_p}\right)^{-MJSWG_p} - \left(1+\frac{V_{DD}-V_{min}}{PBSWG_p}\right)^{-MJSWG_p} \right]$$

$$\kappa = CJSW_p \left[\left(1+\frac{V_{DD}-V_{max}}{PBSW_p}\right)^{-MJSW_p} - \left(1+\frac{V_{DD}-V_{min}}{PBSW_p}\right)^{-MJSW_p} \right].$$

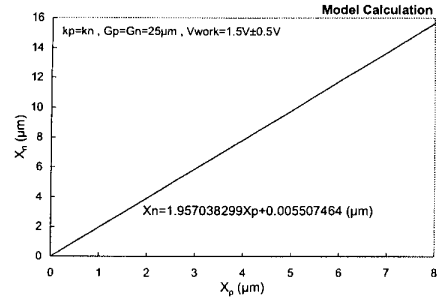
By applying the device parameters of Mn1 and Mp1 in the 0.35-μm silicided CMOS process, the condition to keep the input capacitance with a minimum variation at the voltage levels of V_{DD}=3V, V_{com}=1.5V, and ΔV=0.5V can be found as

$$k_n \cdot \{1.029515 \times 10^{-4} \cdot G_n \cdot X_n + 1.098674 \times 10^{-11} \cdot G_n + 2.204072 \times 10^{-11} \cdot X_n\} = k_p \cdot \{2.011205 \times 10^{-4} \cdot G_p \cdot X_p + 1.156346 \times 10^{-11} \cdot G_p + 4.762930 \times 10^{-11} \cdot X_p\} \quad (6)$$

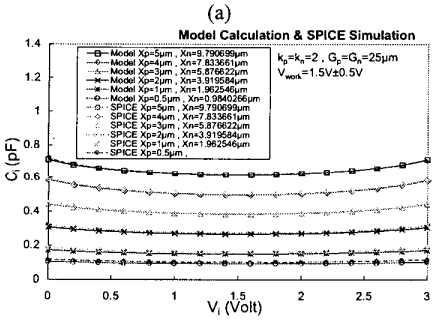
Therefore, if the layout parameters (K_n, K_p, G_n, G_p, X_n, and X_p) on the finger-type Mn1 and Mp1 devices are correctly chosen to meet the condition in (6), the input capacitance of the proposed analog ESD protection circuit can have a minimum variation within the desired input voltage range. This implies that the variation on the input capacitance of the proposed analog ESD protection circuit can be minimized by only choosing the suitable device dimensions and layout spacings in the finger-type Mn1 and Mp1 devices. This is quite easy and useful to design the proposed analog ESD protection circuit with an almost-constant input capacitance for specified analog applications in a given CMOS process.

Now, if k_p=k_n=2 and G_p=G_n=25μm are chosen with the voltage levels of V_{DD}=3V, V_{com}=1.5V, and ΔV=0.5V, the relation between the layout sapcings of X_n and X_p to sustain the condition of (6) is calculated in Fig.5(a), where the X_n is

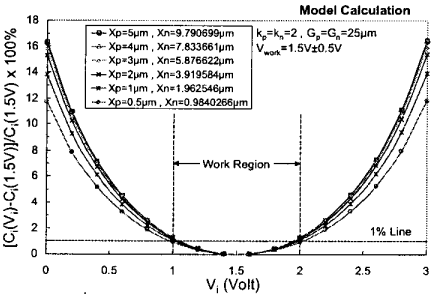
found to be linearly dependent on the X_p. Based on this condition with the specified layout parameters, the relation between the total input capacitance and the input voltage level is calculated and shown in Fig.5(b). The simulation results from HSPICE on the total input capacitance of the proposed analog ESD protection circuit are also compared in Fig.5(b) to verify the accuracy of the derived model equations. This has verified the accuracy of the derived model equations in this work. As shown in Fig.5(b), if the layout parameters X_n and X_p are chosen with smaller values, the proposed analog ESD protection circuit also has a smaller input capacitance. Besides, the analog ESD protection circuit has the smallest input capacitance, when the input voltage level is biased at the analog common reference voltage V_{com}.



(a)



(b)



(c)

Fig.5 (a) The relation between the layout parameters X_n and X_p to meet the condition in equation (21) with the analog common reference voltage biased at 1.5V. (b) The relation between the total input capacitance and the input voltage level under different layout parameters X_n and X_p. (c) The relation between the variation percentage on the input capacitance and the input voltage level under different layout parameters X_n and X_p.

The percentage of variation on the input capacitance in Fig.5(b) with respect to the smallest input capacitance at V_{com}=1.5V under many sets of different layout parameters are calculated and drawn as a function of input voltage in Fig.5(c). If the layout parameters X_n and X_p are chosen with smaller values, the analog ESD protection circuit also has a smaller variation percentage on the input capacitance. Within the desired analog input voltage range of 1 ~ 2V, the variation percentage of the input capacitance is found below 1% in the working region shown in Fig.5(c). With such a small 1% variation on the input capacitance, this proposed analog ESD protection circuit is very suitable for high-frequency and high-precision analog applications.

In Fig.5(a)~5(c), the input capacitance is calculated with the analog common reference voltage (V_{com}) chosen at 1.5V, which is equal to the half of 3-V VDD. If the analog input signals have different common working voltages, the input capacitance with minimum variation within the desired input voltage range can be found by the above equations. This has shown the flexibility of the derived model to find the suitable layout parameters to minimize the voltage-dependent variation on the input capacitance of the proposed analog ESD protection circuit.

4. Conclusion

From the above detailed calculations and analyses on the input capacitance, the derived design model to find the suitable layout parameters for minimizing the input capacitance variation can help the proposed analog ESD protection circuit to be well designed in general CMOS processes. The proposed analog ESD protection circuit with a small and almost constant input capacitance has been practically applied to design the I/O cells in the tsmc cell libraries, which have been widely used in many IC products in both the 0.35-μm and 0.25-μm CMOS processes.

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