

DESIGN OF LOW-CAPACITANCE BOND PAD FOR HIGH-FREQUENCY I/O APPLICATIONS IN CMOS INTEGRATED CIRCUITS

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Abstract

A new structure of bond pad is proposed to reduce its parasitic capacitance in a baseline CMOS process without any process modification. The proposed bond pad has a capacitance less than 50% of that in the traditional bond pad. In addition, this new bond pad also provides better bonding adhesion of 10% improvement than the traditional one. It is greatly useful for high-frequency IC's, which need a very low input capacitance.

I. Introduction

The large input capacitance from the bond pad and input ESD (electrostatic discharge) protection devices often limits the frequency performance of I/O signals in high-speed integrated circuits such as the DRDRAM [1] or RF IC [2]. Although the progress of deep-submicron CMOS technology enables the dimension of integrated circuits dramatically shrunk, the dimension of bond pad is still not reduced as well due to the limitation of bonding machines. The area of a substrate overlapped by the bond pad is sizable in the whole chip area, which results in a large parasitic capacitance to degrade the operating speed of integrated circuits or to require large chip area to construct powerful driver circuits.

Moreover, the input pad must be drawn with the on-chip ESD protection devices to protect the internal circuits against ESD damages. To sustain a high ESD robustness, the ESD protection devices often have larger device dimensions. Therefore, the ESD protection devices contribute large parasitic junction capacitance to the input pad. Recently, a new on-chip ESD protection circuit with a very low input capacitance for analog or RF applications had been reported [3]. This analog ESD protection circuit is drawn in Fig.1, where the Mp1 and Mn1 have a device dimension of only $50\mu\text{m}/0.5\mu\text{m}$ but it can sustain the HBM (human-body-model) ESD level of 6kV in a $0.35\text{-}\mu\text{m}$ CMOS process. With such small ESD protection devices, the total input junction capacitance generated from the ESD protection devices is only 0.37pF. The layout size of the metal bond pad for wire bonding in the $0.35\text{-}\mu\text{m}$ CMOS process is specified as $96\times 96\mu\text{m}^2$, which

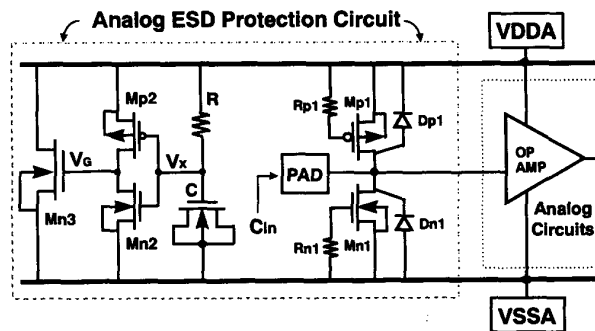


Fig.1 The ESD protection circuit for analog input pin [3].

contributes a parasitic capacitance of 0.67pF. So, the total input capacitance of the analog ESD protection circuit including the bond pad is only 1.04pF, but the bond pad contributes 64% of the total input capacitance [3]. If the bond pad capacitance can be further reduced in this analog ESD protection circuit, the total input capacitance can be significantly reduced for more high-frequency or high-speed circuit applications.

In this paper, a new bond pad structure is proposed to reduce its parasitic capacitance in a baseline CMOS process without any process modification. The proposed new bond pad structure is able to have a capacitance less than 50% of that in the traditional bond pad structure. In addition to reducing the parasitic capacitance, this new bond pad structure also provides better bonding adhesion of 10% improvement than the traditional bond pad.

II. Low-Capacitance Bond Pad

To avoid the peel-off effect that occurs on the bond pad, the present bond pads are mostly constructed by planar multi-metal layers, as shown in Fig.2. Several forms and materials of the via plugs which connect the multi-metal layers had been reported to increase the adhesion of the metal layers on the dielectric layers during wire bonding [4]-[6]. Although the peel-off effect on the bond pad is freer while the more connected metal layers are used, the more parasitic capacitance is induced

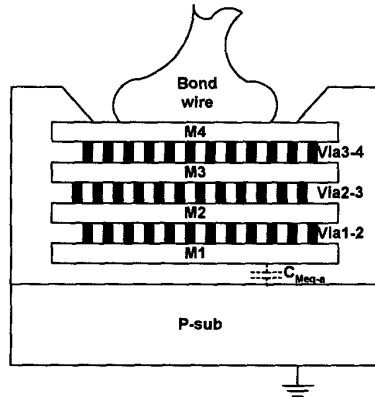


Fig. 2 The cross-sectional view of the traditional bond pad.

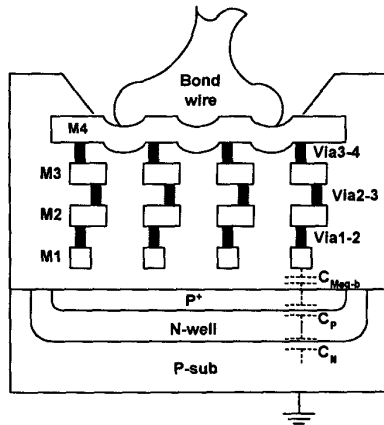


Fig. 3 The cross-sectional view of the proposed bond pad.

because of the metal layer close to the substrate being used. Fig.3 shows the cross sectional view of the structure for the proposed low-capacitance bond pad. This new bond pad is constructed by connecting multi-metal layers to avoid the peel-off effect. The shape of the top metal layer is designed to be a platter for wire bonding, and the underlying metal layers close to the substrate are designed in broken shapes with smaller areas than the top metal layer to reduce the area overlapped with the substrate. Additionally, the diffusion layers are inserted below the multi-metal layers to form the serial capacitance under the pad. Thus, the bond pad has a much lower parasitic capacitance because the area of capacitor constructed by the metal layer overlapping on the substrate is reduced and the junction capacitors are inserted in serial. Besides, the broken shapes of the underlying metal layers can make the

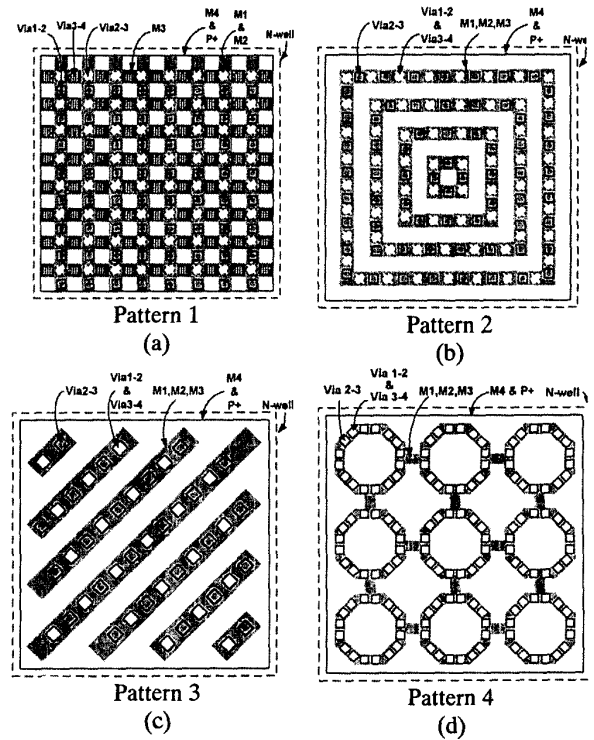


Fig. 4 The schematic layout view of the experimental bond pads.

surface of the top metal layer be irregular to provide a better adhesion between the bond wire and the top metal.

III. Experimental Results

To verify the performance of the new bond pad structure, several experimental bond pads are designed and fabricated in a $0.35\mu\text{m}$ 1P4M standard CMOS process. Figs. 4 and 5 show the schematic layout views and photographs of the experimental bond pads, respectively. The layout area of the top metal for wire bonding is specified as $96 \times 96\mu\text{m}^2$. The relation among the areas of the underlying metal layers overlapping with the substrate is tradition > pattern 1 > pattern 2 > pattern 3 > pattern 4. Fig. 6 shows the photograph of the whole test chip. In this test chip, 9 types of bond pads are fabricated for test. One is the traditional pad, the others are the pads shown in Fig. 4 and their comparing types without the inserted diffusions. For each type of the bond pads, 10 pads are connected together in parallel manner to be measured. Fig. 7 shows the measured capacitance of the experimental bond pads. The measured capacitance of the traditional bond pad is about 0.35pF per pad and that of the new bond

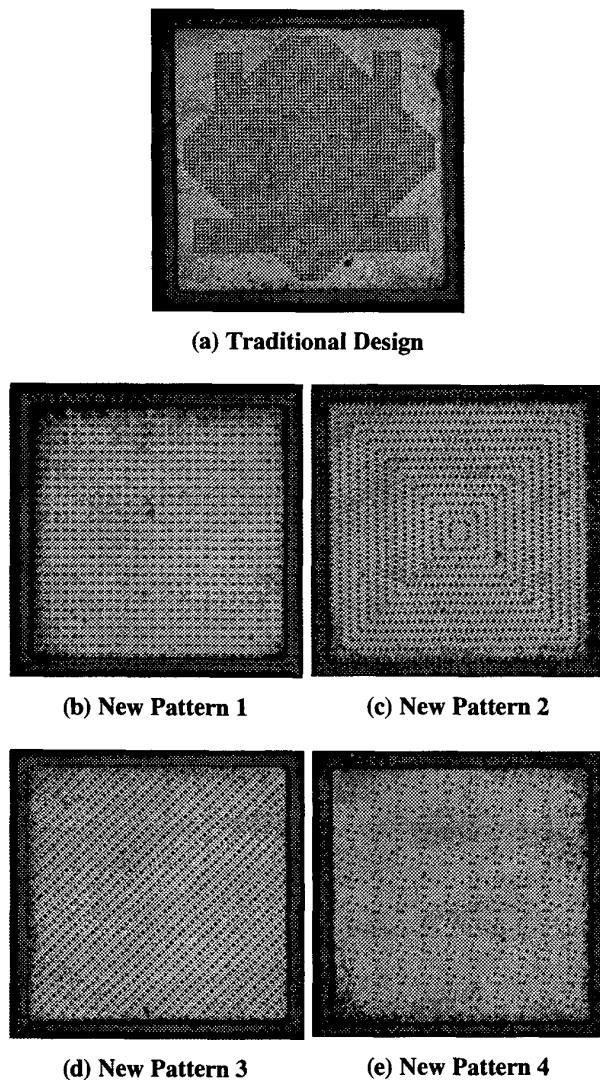


Fig. 5 The photographs of the fabricated bond pads.

pad is from 0.24 to 0.12pF per pad. It can be seen that the smaller areas of the underlying metal layers give the smaller parasitic capacitance indeed, and the inserted serial junction capacitors can provide with smaller parasitic capacitance further. Comparing with the traditional pad, the parasitic capacitance can be reduced to be about 50% under the same pitch area. To show the effect of the bond-pad parasitic capacitance on the I/O of integrated circuits, a simple measurement is done and the result is shown in Fig. 8. It can be seen that the new bond pad provide better step transient response than the traditional pad.

Fig. 9 shows the measurement result of the ball shear

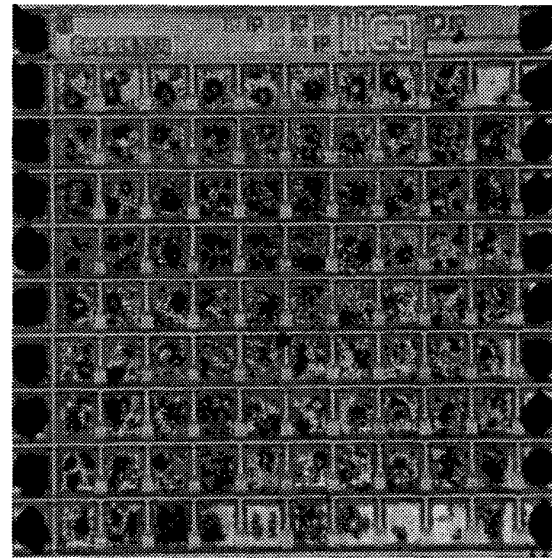


Fig. 6 The photograph of whole test chip.

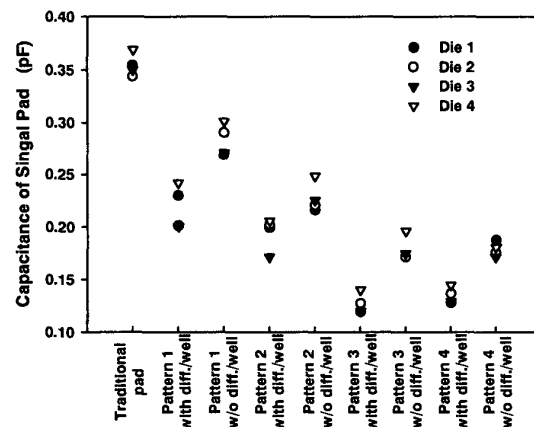


Fig. 7 The measured capacitance for each type of the fabricated pads.

test, as shown in Fig. 10(a), of the MIL-STD-883E bondability test standard [7] on the experimental bond pads. In this test, the failure location codes are all of bond ball lift rather than the peel-off. As shown in Fig. 9, the patterns 2 and 3 provide better bonding reliability than that of the traditional pad structure shown in Fig. 2. The improvement is about 10%. The patterns 1 and 4 do not improve the bonding reliability because they do not provide the enough irregular surface of the top metal layer. Therefore, in order to possess both of low parasitic capacitance and good bonding reliability, the broken

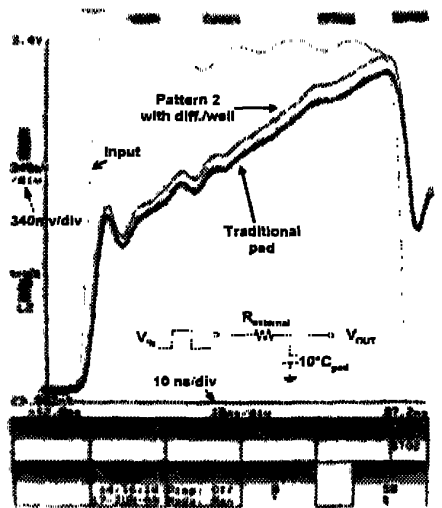


Fig. 8 The step responses of the new pad and the traditional pad.

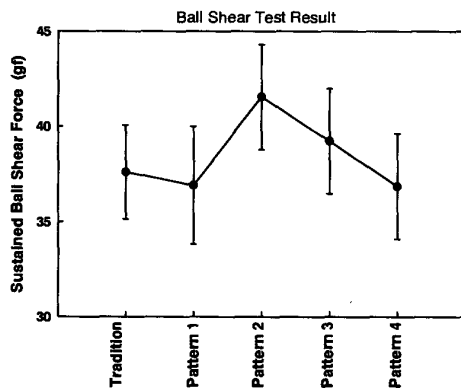


Fig. 9 The measured results of ball shear test.

shapes of the underlying metal layers are recommended to be the same and aligned as the patterns 2 and 3 show, and to be the smallest pieces and spacing that the process can provide. For the another bondability test of the wire pull test, as shown in Fig. 10(b), only the minimum sustained pull force of 8.83 gram-force is measured. The failure location codes for all experimental pads are all of bond ball neck broken which results in the maximum adhesion between the pad and the wire ball to be not able to obtain, and no peel-off occurs on the bond pad too.

IV. Conclusion

From above practical experimental results, the proposed bond pad design can provide a low cost solution for reducing parasitic capacitance on the I/O terminals of chips while the bonding reliability being maintained. This

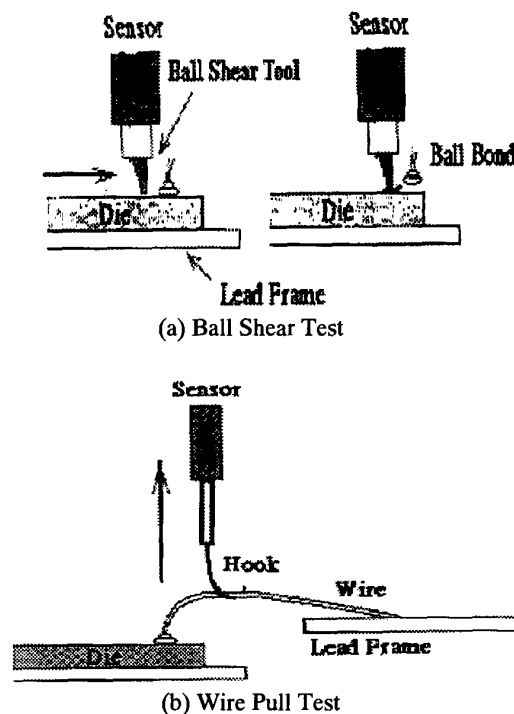


Fig. 10 The MIL-STD-883E bondability test.

is greatly useful for applications in CMOS RF IC's or high-speed memory IC's, where the frequency or speed response is mainly degraded by the parasitic input capacitance.

References

- [1] Rambus Inc. Documentation, "266/288-Mbit Direct RDRAM," Revision 0.7, Apr., 1998, p. 57.
- [2] B. Ballweber, R. Gupta, and D. J. Allstot, "Fully-integrated CMOS RF amplifiers," in *Digest of IEEE ISSCC Conf.*, 1999, pp. 72-73.
- [3] M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD protection design on analog pin with very low input capacitance for RF or current-mode applications," in *Proc. of IEEE International ASIC/SOC Conf.*, 1999, pp.352-356.
- [4] R. Y. Shiue, W. T. Wu, P. C. Shieh, and C. K. Liu, "Method of forming bond pad structure for the via plug process," U. S. Patent # 5700735, Dec., 1997.
- [5] D. Heim, "Composite bond pad for semiconductor devices," U. S. Patent # 5248903, Sept., 1993.
- [6] C. C. Hsue and S. C. Chien, "Polycide bonding pad structure," U. S. Patent # 5734200, Mar., 1998.
- [7] MIL-STD-883E, Method 2011.7, 1996.