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New Diode String Design with Very Low Leakage Current for Using in Power Supply ESD Clamp Circuits

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Abstract

A new diode string design with very low leakage current is proposed for using in the on-chip power supply ESD (electrostatic discharge) clamp circuits. Three traditional designs of the stacked diode strings used in the power supply ESD clamp circuits are also fabricated in the same test chip to verify the improvement of this new design. By adding an NMOS-controlled lateral SCR (NCLSCR) device into the stacked diode string, the leakage current of this new proposed diode string with 6 stacked diodes under a 5-V (3.3-V) forward bias condition can be controlled below 2.1 (1.07) nA at an environment temperature of 125°C. The blocking voltage of this new diode string design with NCLSCR can be linearly adjusted by simply changing the number of the stacked diodes in the diode string for application across the power lines with different voltage levels to achieve the whole-chip ESD protection scheme.

1. Introduction

A CMOS USLI with more integrated functions and circuits in a single chip often has more separated power pins or even has multiple mixed voltage power supplies. In the mixed-mode IC's, the digital power pins are generally separated from the analog power pins to avoid the noise interference between the power lines. But, a mixed-mode CMOS IC with separated power pins had been found to have the ESD damage located on the interface circuits between the analog and digital circuits [1]. Therefore, the bi-directional diode strings was added between every two adjacent separated power lines for conducting the ESD current away from the interface and internal circuits of the mixed-mode IC's [2]. Because the diode in the forward-biased condition can sustain a much higher ESD level than it is stressed in the reverse-biased condition, the diode string with multiple stacked diodes was therefore used to clamp the ESD overstress voltage on the 3V/5V-tolerant I/O pad in *IBM* [3] or between the power lines with different voltage levels in *Intel* [4]-[6].

But, the main issue of using the diode string in the forward-bias stacked connection as the ESD clamp device is the leakage current, which is obviously increased as the operating temperature of the diode string is increased [3]-[6]. The diode string used as the ESD clamp from the VDD to VSS power lines is illustrated in Fig.1(a), whereas the device structure of such a diode string realized in a p-substrate n-well CMOS process is illustrated in Fig.1(b). There is a parasitic vertical p-n-p BJT in every diode structure. The amplification effect of multi-stage Darlington beta gain [7] among the vertical p-n-p BJT's in the diode string causes the more leakage current conducting into the p-substrate, if the voltage difference across VDD and VSS is larger or the temperature is higher.

In this paper, a new design on the diode string is proposed to still keep the excellent ESD protection performance of the diode string for using in the on-chip power supply ESD clamp circuits, but without the disadvantage of leakage current in the traditional diode string designs.

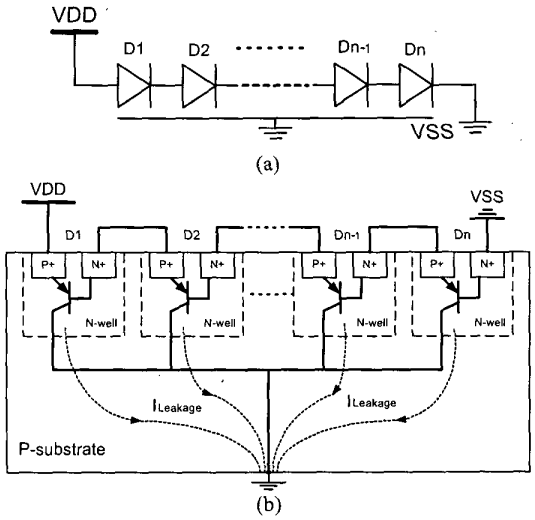

Fig.1 (a) The schematic circuit diagram, and (b) the cross-sectional view, of the pure diode string realized in a p-substrate n-well CMOS technology.

2. Traditional Designs on the Stacked Diode String to Reduce the Leakage Current

To reduce the leakage current of the diode string, especially operating in the high-temperature environment, three designs were previously reported by T. Maloney in *Intel* Corp., which are re-drawn in Fig.2(a) ~ 2(c) with the names of Cladded diode string, Boosted diode string, and Cantilever diode string [6]. These three modified diode strings are also fabricated in the same experimental test chip and compared to

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the proposed new design (this work).

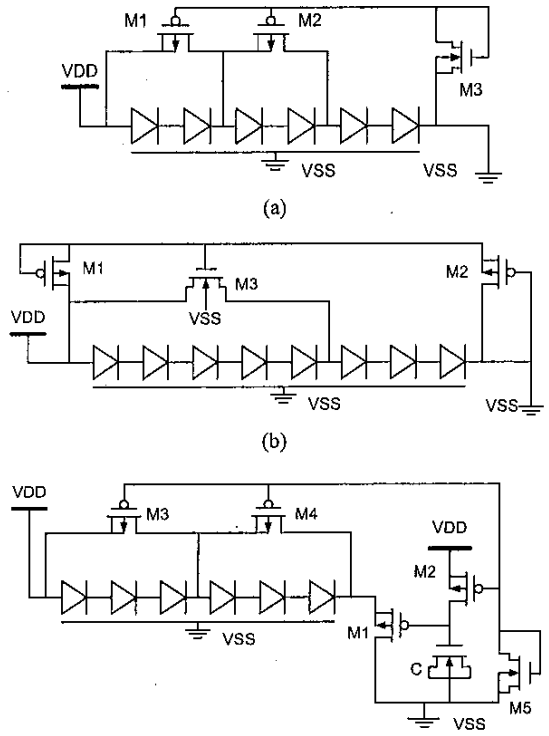


Fig.2 The circuit diagrams of the traditional diode string designs with the names of (a) the Cladded diode string, (b) the Boosted diode string, and (c) the Cantilever diode string [6].

3. New Design of This Work

The proposed new design to reduce the leakage current in the stacked diode string is shown in Fig.3(a), whereas the device structure of this new design is drawn in Fig.3(b). An NMOS-controlled lateral SCR (NCLSCR) device is added on the top of the stacked diode string to block the leakage current from VDD to VSS through the diode string, while the IC is in the normal operating condition. But, the NCLSCR is designed to be quickly turned on to conduct the ESD current from VDD to VSS through the stacked diode string, while the IC is in the ESD-stress condition. To achieve the correct turn-on and turn-off operations of the NCLSCR with the stacked diode string, the *RC*-based ESD-detection circuit [8] is applied to control the gate voltage of the NCLSCR. If the gate of the NCLSCR has a positive voltage with respect to the VSS power line, the NCLSCR will be turned on, therefore the current can flow from VDD to VSS power lines through the NCLSCR and the stacked diode string. If the gate of the NCLSCR is kept at 0V, the NCLSCR is turned off to block the leakage current from VDD to VSS through the stacked diode string. Because the leakage current of the NCLSCR device is not increased when the environment temperature becomes higher, the leakage current of this new design in Fig.3 can be easily reduced to a very low current level without using the complex design methods as those shown in Fig.2(a) ~ 2(c).

This new design with different number of stacked diodes in the diode string and the traditional designs on the diode strings in Fig.1 and Fig.2 are all practically fabricated on a same test chip in a 0.35-μm silicided CMOS process without using neither the ESD- implantation nor the silicide-blocking process modifications to compare the performance among such designs with the diode strings for power supply ESD protection. The typical layout example of the new design in Fig.3 with an NCLSCR and 6 diodes is shown in Fig.4.

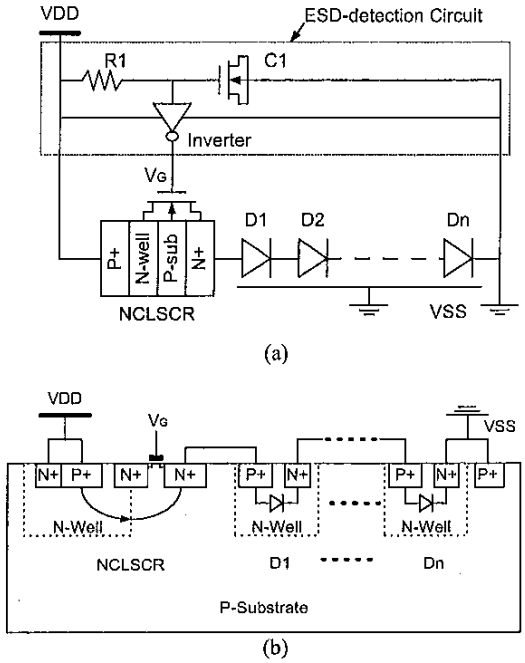


Fig.3 (a) The schematic circuit diagram, and (b) the device structure, of the new proposed diode string realized in a p-substrate CMOS technology.

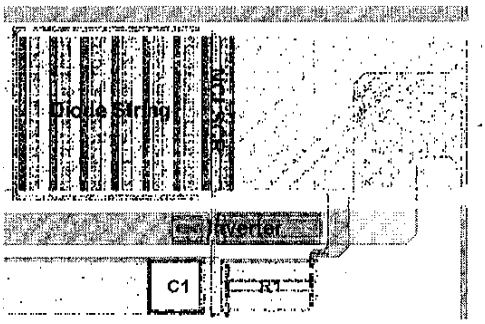


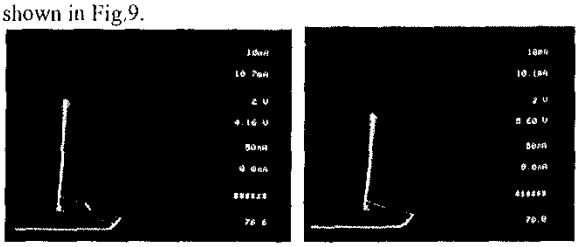
Fig.4 The layout example of the new design with an NCLSCR and 6 stacked diodes in the diode string realized in a 0.35-μm CMOS process.

4. Experimental Results

4.1 I-V Characteristics

The measured I-V curves in the holding regions of the NCLSCR with different number of stacked diodes are shown in Fig.5(a) and 5(b). The relation of the holding voltage of the NCLSCR with different number of diodes is shown in Fig.6 at the temperature of both 25°C and 125°C.

The measured I-V curves of the diode strings with different designs and 6 ~ 8 stacked diodes in Fig.1 ~ Fig.3 are compared in Fig.7 and Fig.8 at the temperature of 25°C and 125°C, respectively. The cut-in voltage measured at 1μA of the pure diode string with different number of stacked diodes in the diode string at the temperature of 25°C and 125°C are shown in Fig.9.



(a) (b)

Fig.5 The measured I-V curves in the holding regions of (a) a single NCLSCR with 4 stacked diodes, and (b) a single NCLSCR with 6 stacked diodes, under the temperature of 125°C.

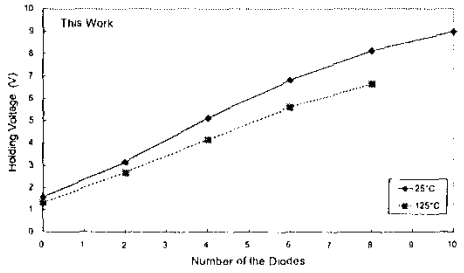


Fig.6 The relation of the holding voltage of the NCLSCR with different number of diodes at the temperature of 25°C and 125°C.

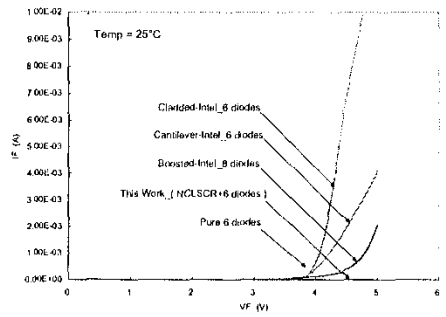


Fig.7 The measured I-V curves of the diode strings with different designs at the temperature of 25°C (Y axis is drawn in the linear scale).

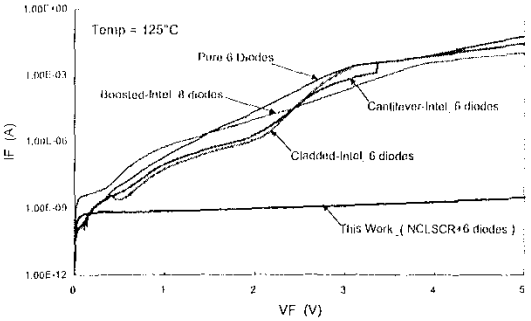


Fig.8 The measured I-V curves of the diode strings with different designs at the temperature of 125°C (Y axis is drawn in the log scale).

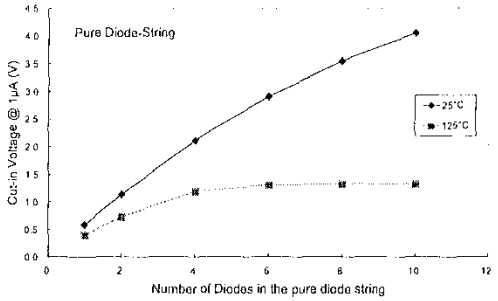


Fig.9 The cut-in voltage measured at 1μA of the pure diode string with different number of stacked diodes in the diode string at the temperature of 25°C and 125°C.

4.2 Leakage Current

The leakage currents under 5-V and 3.3-V voltage biases across the VDD and VSS power lines among the diode strings with different designs at the temperature of 25°C are measured and shown in Fig.10. The leakage currents among the different diode string designs at the temperature of 25°C and 125°C under 3.3-V voltage bias are shown in Fig.11.

The leakage current of the pure diode string with 6 stacked diodes under the VDD bias of 3.3V at the temperature of 25°C (125°C) is 12.45μA (3.46mA). The Cladded diode string with 6 diodes under the VDD bias of 3.3V at the temperature of 25°C (125°C) is 3.5μA (3.33mA). The Boosted diode string with 8 diodes under the VDD bias of 3.3V at the temperature of 25°C (125°C) is 44.03μA (0.61mA). The Cantilever diode string with 6 diodes under the VDD bias of 3.3V at the temperature of 25°C (125°C) is 4.96μA (1.25mA). But, the proposed new design (this work) on the diode string with an NCLSCR and 6 diodes under the VDD bias of 3.3V at the temperature of 25°C (125°C) is only 31pA (1.07nA). With such a very low leakage current in the new diode string design, as compared to the previous designs in Fig.1 and Fig.2, this new diode string is very much suitable for using in the portable or low-power electronics products.

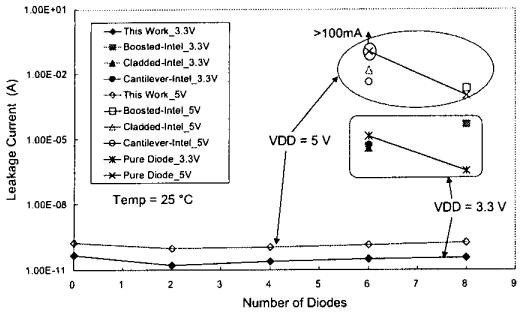


Fig.10 The leakage currents under 5-V and 3.3-V voltage biases among the diode strings with different designs at the temperature of 25°C (Y axis is drawn in the log scale).

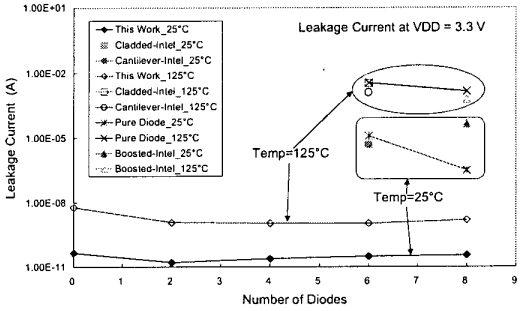


Fig.11 The leakage currents among the different diode string designs at the temperature of 25°C and 125°C under 3.3-V voltage bias (Y axis is drawn in the log scale).

4.3 ESD Level

The fabricated diode strings in different designs have been verified by the *Zapmaster* ESD tester in both the human-body-model (HBM) and the machine-model (MM) ESD stresses. The ESD robustness of the VDD-to-VSS ESD clamp circuits with different number of stacked diodes is listed in Table I. The failure criterion to identify the ESD level is defined as the leakage current of the low-leakage diode string greater than 1μA under 6-V voltage bias. The VDD-to-VSS ESD clamp circuits with different number of the stacked diodes can sustain the HBM ESD stress of greater than 8kV. For the typical application in a 3-V CMOS IC, this new proposed low-leakage diode string with an NCLSCR and 4 diodes can sustain an HBM (MM) ESD level of up to >8kV (1150V), which is much higher than the general HBM (MM) ESD specification of 2kV (200V) in the consumer IC products.

The previous designs, including the cladded diode string with 6 diodes, boosted diode string with 8 diodes, and cantilever diode string with 6 diodes are also investigated by the ESD tester as a reference. The HBM and MM ESD levels of those designs are listen in Table II. Because those previous designs have larger leakage currents, the failure criterion is defined as the relative 20% shift on the voltage at I=1μA of the diode string. Each diode used in those previous designs has the same layout dimension as that used in the proposed low-leakage diode string. As seen in Table II, the boosted diode string with 8 diodes only has an HBM (MM) ESD level of 4.5kV (550V).

As comparing the ESD results between Table I and Table II, the new proposed diode string can still maintain the excellent ESD robustness of the diode string but with a very low leakage current from VDD to VSS.

Table I

The proposed new diode string design						
	NCLSCR	NCLSCR +2 diodes	NCLSCR +4 diodes	NCLSCR +6 diodes	NCLSCR +8 diodes	NCLSCR +10 diodes
HBM ESD Level	> 8kV	> 8kV	> 8kV	> 8kV	> 8kV	> 8kV
MM ESD Level	1650V	1400V	1150V	900V	700V	550V
Failure criterion : $I_{Leakage}$ > 1μA @ 6-V bias						

Table II

The diode string designs provided by T. Maloney [6]			
	Cladded Diode String	Boosted Diode String	Cantilever Diode String
HBM ESD Level	> 8kV	4.5 kV	> 8kV
MM ESD Level	1250V	500V	550V
Failure criterion : V_{shift} > 10% @ 1-μA bias			

5. Conclusion

A new diode string design has been successfully verified in a 0.35-μm silicided CMOS process, and practically compared to the previous designs. The leakage current of a diode string with 6 stacked diodes under the VDD bias of 3.3V at the temperature of 25°C (125°C) is reduced to only 31pA (1.07nA), whereas the leakage current of the previous Cantilever diode string with 6 diodes is as high as 4.96μA (1.25mA). This new diode string design still keeps the excellent performance on the ESD level and quick turn-on speed. Thus, this new diode string is very much suitable for applying in the portable or low-power CMOS IC's.

6. References

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