On-Chip ESD Protection Design by Using Polysilicon Diodes in CMOS Technology for Smart Card Application

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Abstract -- A novel on-chip ESD protection design by using polysilicon diodes for smart card application is reported in this paper. By adding an efficient VDD-to-VSS clamp circuit, the HBM ESD level of the smart card IC with polysilicon diodes as the ESD protection devices have been successfully improved from the original ~300V to become ≥3kV. Different process splits have been experimentally evaluated to find the suitable doping concentration for optimizing the polysilicon diodes for both smart card application and on-chip ESD protection design.

1. Introduction

In the smart card application, the electrical power for circuit operations is generated from the transformer (formed by several loops of planner inductor on the circuit board) and the on-chip bridge rectifying circuit into the smart card IC. The traditional full-wave bridge rectifying circuit formed by four diodes to convert the AC power into DC power is shown in Fig. 1. An AC voltage between terminals Vs1 and Vs2 is rectified into a DC voltage and stored in the capacitor Cs for application across the load. When the smart card is close to a card reader (or detector), the electromagnetic field generated from the card reader is coupled by the transformer in the smart card and charges up the electrical power of the smart card for circuit operation. The coupled AC power is converted into DC power by the on-chip four-diode bridge rectifying circuit in the smart card IC. With the converted DC power, the information stored in the smart card IC can be emitted out and detected by the card reader for personal identification or other applications.

When the on-chip rectifying circuit is realized in a CMOS IC with a p-type substrate, the diodes D1 and D2 are often made by the p-n junctions across P+ diffusion and N-well. The diodes D3 and D4 are often made by the p-n junctions across N+ diffusion and p-substrate. The diode device structures in a CMOS IC with a common p-substrate are illustrated in Fig. 2.

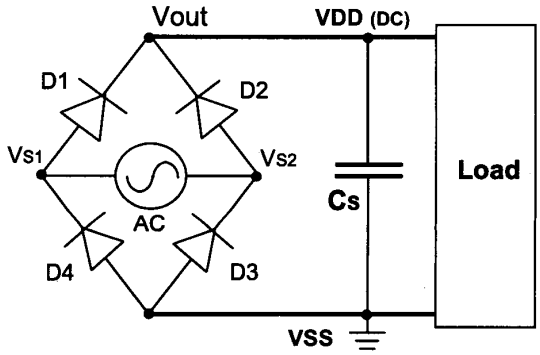


Fig.1 The traditional full-wave bridge rectifying circuit formed by four diodes to convert the AC power into DC power.

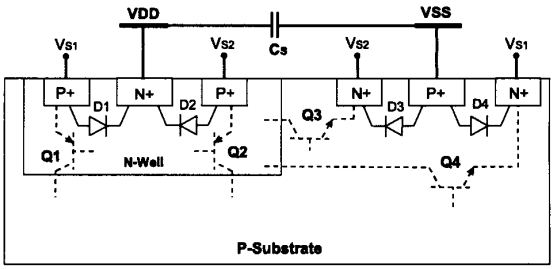


Fig.2 Device cross-sectional view of the four p-n junction diodes of the full-wave bridge rectifying circuit realized in a CMOS IC with a common p-type substrate.

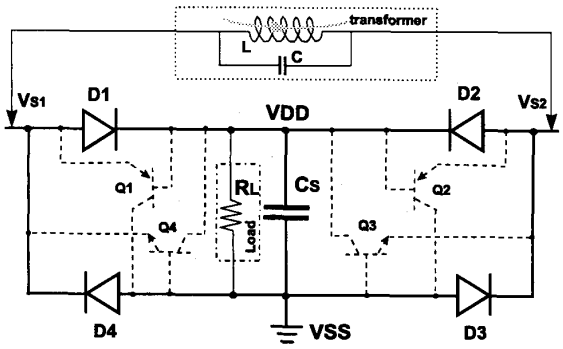


Fig.3 The leakage current paths along the parasitic BJT's in the traditional full-wave bridge rectifying circuit realized in CMOS IC with a common p-type substrate.

Due to the common p-substrate of a CMOS IC, besides the diode structures in Fig.2, there are four parasitic bipolar junction transistors (BJT's) Q1, Q2, Q3, and Q4 in this structure. Q1 (Q2) is a parasitic vertical p-n-p BJT between the Vs1 (Vs2) and the common p-substrate. Q3 (Q4) is a parasitic lateral n-p-n BJT between the Vs2 (Vs1) and the VDD-biased N-well. These parasitic BJT's would cause the decreased rectification efficiency, or even no rectification at all, for the full-wave bridge rectifying circuit. The parasitic BJT's are drawn into the full-wave bridge rectifying circuit and illustrated in Fig. 3 to show its influence.

When the transformer-coupled AC voltage is in its positive half-wave period (Vs1 > Vs2), the diodes D1 and D3 are turned, while the diodes D2 and D4 are off. During this condition, the current flowing from Vs1 to Vs2 through the D1, Cs, and D3 charges up the capacitor Cs. When the coupled AC voltage is in its negative half-wave period (Vs1 < Vs2), the diodes D2 and D4 are turned on, but the diodes D1 and D3 are off. During this time, the current flowing from Vs2 to Vs1 through the D2, Cs, and D4 charges up the capacitor Cs. The two charge states therefore create a DC power source across the capacitor Cs for use by the load circuits.

However, the parasitic BJT's (Q1 ~ Q4) in Fig. 2 with a common substrate cause serious degradation on the rectification efficiency of this full-wave bridge rectifying circuit. When the AC voltage is in its positive half-wave period (Vs1 > Vs2), the base-emitter junction (the diode D3) of the parasitic BJT Q3 is forward biased to turn on the BJT Q3. Thereby, a great amount of charge current is created that directly flows through the parasitic BJT Q3 (from VDD node to Vs2) instead of through the capacitor Cs. During the positive half-wave period (Vs1 > Vs2), the diode D1 is also forward biased and therefore turns on the parasitic BJT Q1. Some of the charge current is directly flowing through the parasitic vertical BJT Q1 (from Vs1 to VSS node) instead of through the capacitor Cs. Similarly, the same problem caused by the parasitic BJT's Q2 and Q4 occurs during the negative half-wave period (Vs1 < Vs2). Therefore, the rectification efficiency of this full-wave bridge rectifying circuit realized in the CMOS IC with a common substrate is seriously decreased, and can even have no rectification at all.

In some modified design, the diodes may be changed to NMOS or PMOS devices in the full-wave bridge rectifying circuit for realization in CMOS IC [1]. The parasitic vertical or lateral BJT's still exist among device structures to degrade its rectification efficiency. Moreover, the different connections between the bulk and the source of NMOS or PMOS devices in the full-wave bridge rectifying circuit cause the body effect to degrade the power converting speed and results in a poor rectification efficiency [1].

If the diodes in the full-wave bridge rectifying circuit are realized by the polysilicon diodes, which have no any parasitic BJT in their device structures, the aforementioned problem can be totally eliminated. Therefore, the rectification efficiency can become much high to convert the coupled AC power into DC power for circuit operation in a smart card. However, due to the low heat dissipation capability of the polysilicon layer, the polysilicon diodes connected at the VS1 and Vs2 nodes (which are wire-bonded to the circuit board in final application) result in a very low human-body-model (HBM) ESD level of around 200~300V. With such an low ESD level, the die of smart card IC assembled into the smart card by the COB (chip-on-board) bonding is very susceptible to ESD events. This limits the ability to mass produce the smart card IC.

In this paper, the breakdown voltage, leakage current, and ESD performance of the polysilicon diodes are well evaluated by performing different n- or p-type doping concentrations with experimental process splits. The dependence between the It2 (measured by transmission line pulse generator) and layout spacing in the polysilicon diodes is also characterized in detail. The HBM ESD level of the smart card IC can be finally improved to ≥3kV by using a novel ESD power clamp network between VDD and VSS with the polysilicon diodes.

2. Original Design in a Smart Card IC

Due to the aforementioned concerns on both leakage and substrate current in the practical smart card applications, the four-diode bridge rectifying circuit cannot be simply realized by using the n+/ P-substrate or the p+/N-well junction diodes in a bulk CMOS process to convert the coupled AC power into DC power. Therefore, the four-diode bridge rectifying circuit in smart card IC's is often realized by using the polysilicon diodes, which do not cause any leakage or substrate current in the chip. The on-chip bridge rectifying circuit in a smart card IC realized by four polysilicon diodes is shown in Fig. 4.

The electromagnetic field generated from the card reader is coupled by the off-chip transformer. The coupled AC voltage across the pad1 and pad2 has a maximum voltage swing of 12V and a frequency of 125 kHz in the smart card application. This coupled AC voltage is converted into DC voltage by the on-chip full-wave bridge rectifying circuit with four polysilicon diodes and temporarily stored in the on-chip capacitor (Cs) for circuit operation. The memorized data or number in the smart card IC for identification is emitted out by the output PMOS (Mp2) in cooperation with the off-chip transformer. The diodes (Dp1, Dn1, Dp2, and Dn2) to form the four-diode bridge rectifying circuit are all realized by the polysilicon layer with p+ / n- / n+ doping concentration. The device structure and layout top view of the polysilicon diodes realized in a CMOS process are shown in Fig. 5(a) and 5(b), respectively. The polysilicon layer has a thickness of 1500Å in a 0.8-μm CMOS process. The layout spacing S of the lightly doped center region in polysilicon diode in Fig. 5 is originally drawn as 3 μm. The anode and cathode contacts of the polysilicon diode have a clearance of 4 μm to the lightly doped center region.

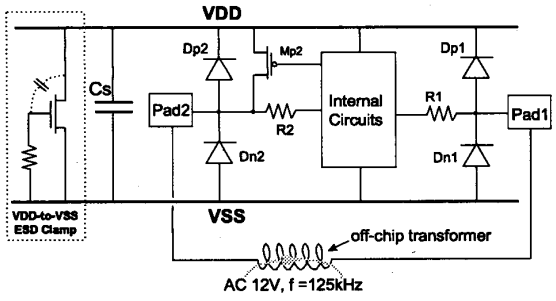


Fig.4 The on-chip bridge rectifying circuit in a smart card IC realized by four polysilicon diodes with the original design of on-chip ESD protection circuits.

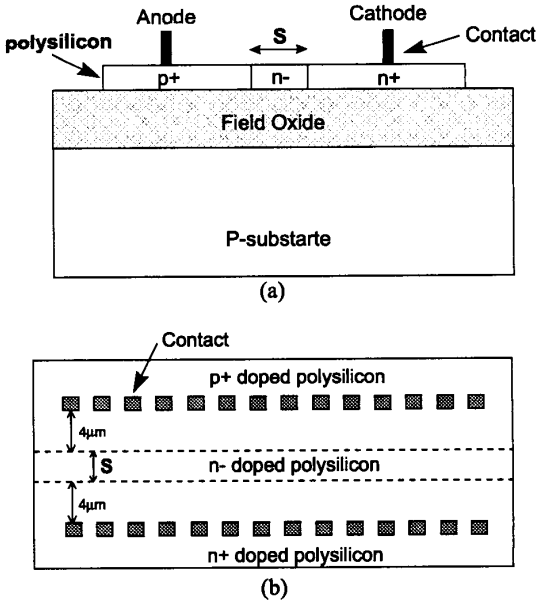


Fig.5 (a) The device structure, and (b) the layout top view, of the p+/n-/n+ polysilicon diode realized in a 0.8-μm CMOS process.

To sustain a higher breakdown voltage (>12V) of the polysilicon diode for smart card application, an extra mask layer is added into the CMOS process flow to implant the n- region in the polysilicon diode. The p+ (n+) region in the polysilicon diode is implanted with a doping concentration of 6E15 (3.5E15) cm^{-3}, which is the same as the drain/source implantation of PMOS (NMOS) in the CMOS process.

Due to the limitation of using the bulk p-n junction diodes to realize the bridge rectifying circuit, the on-chip ESD protection circuits for pad1 and pad2 are therefore also realized by the polysilicon diodes (Dp1, Dn1, Dp2, and Dn2) with an input series resistor (R1, R2) of 500Ω. Each polysilicon diode has a total perimeter of 250μm. The n- region has a width of 3μm between the p+ and n+ regions of the polysilicon diode. A gate-coupled NMOS with a device dimension (W/L) of 300μm/2μm is also added into the chip across VDD and VSS power lines as the VDD-to-VSS clamp circuit for ESD protection.

However, due to the low heat dissipation capability of the polysilicon layer, the human-body-model (HBM) ESD level of this smart card IC fabricated in a 0.8-μm CMOS process is only around ~300V, especially on the pad1 pin with the polysilicon diodes fully isolated from the p-substrate. With an ESD level

below 500V, the die of smart card IC assembled into the smart card by the COB (chip-on-board) bonding is very susceptible to ESD events. Such a low ESD level had gotten a lot of complaints from the smart card manufactory.

To improve the ESD level of the smart card IC, a process split on increasing the doping concentration of the n- region in the polysilicon diode had been investigated in the 0.8-μm CMOS process. The increased doping concentration of the n- region can lower the breakdown voltage of the polysilicon diode, therefore reducing the ESD-generated heat located on the polysilicon diode. The experimental results are summarized in Table 1, where the HBM ESD level of pad1 pin in VSS(+) test mode is only varying from 150V to 300V when the n- doping concentration is increased from 3E13 to 9E13 cm^{-3}. Even in the VSS(-) ESD test mode, where the polysilicon diode is forward stressed, the HBM ESD level of pad1 pin is varying from 400V to 600V only. This is quite low for a diode with a perimeter of 250μm in forward-biased condition. The high turn-on resistance of the polysilicon diode would limit the ESD current discharged through the polysilicon diode and cause ESD damage located on the internal devices.

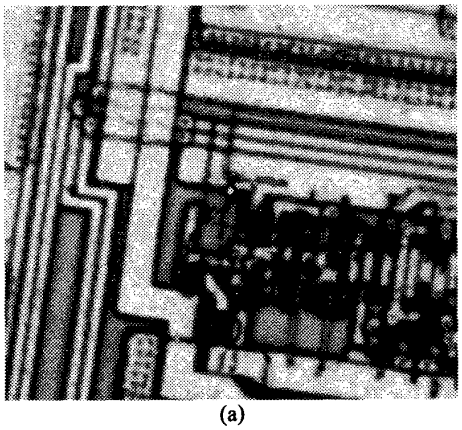
The EMMI pictures of failure locations on the smart card IC after the VSS(+) and VDD(-) ESD stresses are shown in Fig. 6(a) and 6(b), respectively. In Fig. 6(a) [Fig. 6(b)], the ESD failure is located on the NMOS (PMOS) gate oxide of the first input stage that connected to the pad1 pin through the resistor R1, rather than on the polysilicon diodes Dp1 or Dn1. The PMOS and NMOS in the 0.8-μm CMOS process have a gate-oxide thickness of 250Å. The high breakdown resistance of polysilicon diodes cannot effectively protect the 250-Å gate oxide of the input circuits.

Therefore, only simply changing the n- doping concentration can not effectively improve ESD level of the pad1 pin in such a smart card IC. A more efficient ESD protection design should be developed to overcome this problem in the smart card IC with the polysilicon diodes.

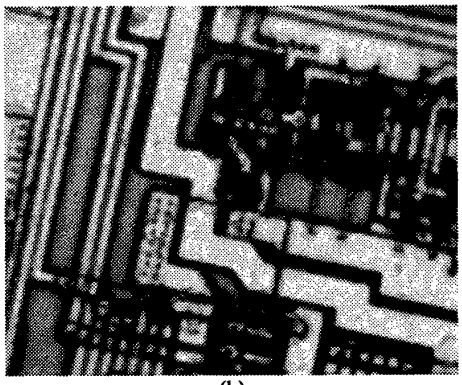
Table 1

n- Doping Concentration (cm-3)	HBM ESD Level (Volt)			
	VDD(+)	VDD(-)	VSS(+)	VSS(-)
9E13	600	300	300	600
5E13	550	300	250	500
3E13	400	250	150	400

(Failure criterion : ILeakage > 1μA @ 5-V bias)



(a)



(b)

Fig.6 The EMMI pictures to show the ESD failure location on the input circuits after the (a) VSS(+) test mode, and (b) VDD(-) test mode, HBM ESD stresses.

3. New On-Chip ESD Protection Design

To still apply the polysilicon diodes as the ESD protection devices at the pad1 pin, the concept of whole-chip ESD protection by using a more efficient VDD-to-VSS ESD clamp circuit to significantly improve ESD level of I/O pin [2]-[4] is applied into this smart card IC. The new proposed on-chip ESD protection circuit is shown in Fig. 7 with a novel VDD-to-VSS ESD clamp circuit [5], where the ESD protection circuit for pad1 pin has two-stage protection diodes. The VDD-to-VSS ESD clamp circuit is formed by the NMOS Mn3 and its corresponding ESD-detection circuit. The gate of Mn3 is controlled by a stacked diode string, which is also realized by the polysilicon diodes. If the stacked diodes were realized by the p+ diffusion in N-well in

CMOS process with a common p-substrate, there was a significant leakage current on the order of mA from VDD to VSS due to the parasitic vertical BJT effect in CMOS process [6]-[8]. But, when the stacked diodes are realized by the polysilicon layer, the leakage current can be reduced below 1μA under 5-V VDD bias. Therefore, the leakage current from VDD to VSS through the diode string and the resistor R3 of 10kΩ in Fig. 7 can be controlled smaller than 1μA, if the diode number in the stacked diode string is large enough.

For use in the smart card IC with a converted VDD power, 8 polysilicon diodes are used in the diode string to control the gate voltage of Mn3, which has a device dimension (W/L) of 300μm/2μm in the practical IC. When the VDD is charged to no more than 5V, the Mn3 is kept off. But when the VDD is charged up greater than 5V, the Mn3 is turned on to clamp the VDD voltage level. By changing the number of polysilicon diodes in the stacked diode string, the clamped voltage level on VDD can be adjusted for different applications.

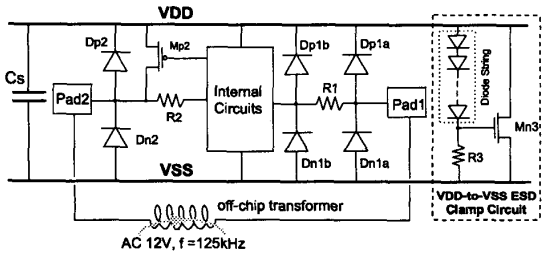


Fig.7 The new design of on-chip ESD protection circuit with a novel VDD-to-VSS ESD clamp circuit in the smart card IC.

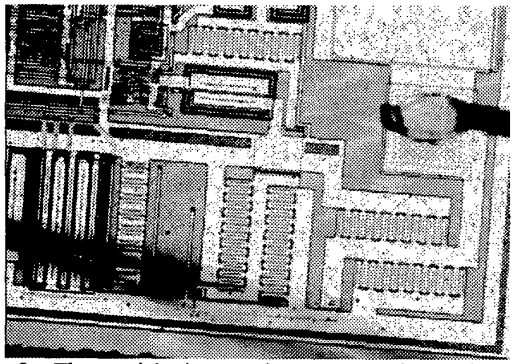


Fig.8 The partial picture of a smart card IC with the realization of ESD protection circuit on the pad1 pin and the VDD-to-VSS ESD clamp circuit.

With the novel VDD-to-VSS ESD clamp circuit, the ESD current under the VSS(+) ESD stress is discharged through the forward-biased Dp1a to VDD, and then discharged through the turned-on Mn3 to VSS, rather than the breakdown of polysilicon diode Dn1a. In the VDD(-) ESD stress, the negative ESD current is conducted to VSS through the forward-biased Dn1a, and then discharged to the grounded VDD through turned-on Mn3, without causing breakdown on polysilicon diode Dp1a. The second diode stage with Dp1b and Dn1b is used to further clamp overstress voltage across the gate oxide of the input circuits for more safe ESD protection. The partial picture of a smart card IC with realization of ESD protection circuit on the pad1 pin and the VDD-to-VSS clamp circuit is shown in Fig. 8, where the polysilicon diodes of pad1 pin are all drawn in the multiple-fingers style with a total perimeter of 300μm for each diode.

To choose a better doping concentration for the n-region in the polysilicon diode for smart card application, a comprehensive process split with different implantation energy is investigated in Table 2. If the n- region has a higher doping concentration or a higher implantation energy, the polysilicon diode has a lower breakdown voltage and a higher forward-biased current, which will be better for ESD protection. But, because the transformer-coupled AC voltage could have a maximum voltage swing of 12V, the breakdown voltage of polysilicon diode is selected to be greater than 12V for safe application. Therefore, the split case of #n2 in Table 2 is suitable for using in this smart card IC.

Besides, the polysilicon diode can be also realized with a p-type lightly doping region, as that shown in Fig. 9(a) and 9(b). The process split is also used to investigate the characteristics of such a p+ / p- / n+ polysilicon diode. The experimental results are listen in Table 3, where the polysilicon diode has a layout spacing (the p- doping region) S of 3μm. Due to the concern for the transformer-coupled maximum AC voltage swing of 12V, the split case of #p2 in Table 3 is suitable for using in this smart card IC.

Table 2

Split Case	N- Doping Concentration (cm-3)	Current @1-V forward-bias	Breakdown Voltage @1-μA current
# n1	7E13, 80KeV	3.4 μA	23 V
# n2	9E13, 80KeV	24.2 μA	15.6 V
# n3	2E14, 80KeV	807.8 μA	7.8 V
# n4	9E13, 50KeV	7.7 μA	16.5 V
# n5	2E14, 50KeV	706.2 μA	7.8 V

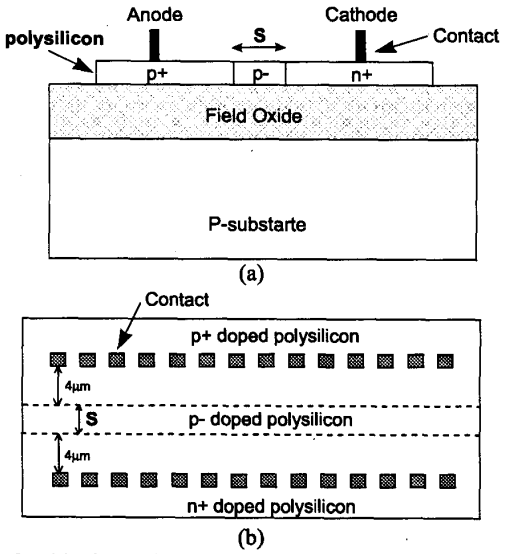


Fig.9 (a) The device structure, and (b) the layout top view, of the p+ / p- / n+ polysilicon diode realized in a CMOS process.

Table 3

Split Case	P- Doping Concentration (cm-3)	Current @1-V forward-bias	Breakdown Voltage @1-μA current
# p1	1E13, 80KeV	8.4 μA	21.5 V
# p2	5E13, 80KeV	252 μA	12.4 V
# p3	9E13, 80KeV	928 μA	9.3 V

4. Dependence of Layout Parameters on the It2 of Polysilicon Diodes

Although the process splits can find the optimized doping concentration for the lightly doped center region in the polysilicon diode, the ESD performance of the polysilicon diode can be further improved by suitably choosing its layout parameters. Under a fixed process split condition with the n- (of 1.5E14 cm^{-3}) doped center region, a lot of polysilicon diodes are fabricated in a test wafer with different layout spacings S of the lightly-doped center region and different total perimeters Wt. A polysilicon diode with a large device dimension is drawn in the multiple-fingers layout style, in which every finger has a layout length of 30 μm. For a polysilicon diode with a total perimeter (Wt) of 300 μm, there are 10 fingers drawn in parallel in the device layout.

The measured I-V curves of the polysilicon diodes with a fixed Wt of 300 μm but different S spacings are shown in Fig. 10. The polysilicon diode with a narrower spacing S has a smaller cut-in voltage in the forward-bias condition, and a smaller (in magnitude) breakdown voltage in the reverse-biased condition.

To further investigate ESD performance of the fabricated polysilicon diodes, the transmission line pulse (TLP) generator (according to the prior art of [9]) has been successfully set up with a pulse width of 100ns [10]-[11] and used to measure It2 of the polysilicon diodes. The TLP-measured I-V curves of the polysilicon diodes with a fixed Wt of 300 μm but different S spacings are shown in Fig. 11(a) and 11(b) in the forward- and reverse-biased conditions, respectively. The dependence of It2 on the layout parameter S in both the forward- and reverse-biased conditions is summarized in Fig. 12. The TLP-measured I-V curves of the polysilicon diodes with a fixed spacing S of 3 μm but different total perimeters Wt are shown in Fig. 13(a) and 13(b) in the forward- and reverse-biased conditions, respectively. The dependence of It2 on the total perimeter Wt of the polysilicon diode in both forward- and reverse-biased conditions is compared in Fig. 14. A polysilicon diode with a wider perimeter Wt also has a larger volume for heat dissipation, therefore it has a higher It2 value.

As seen in Fig. 12 and Fig. 14, the polysilicon diode in forward-biased condition has a much higher It2 value than it does in the reverse-biased condition. This is due to the different power ($\approx$ IESD $\times$ Vop) generated by the ESD current on the polysilicon diode in the forward- and reverse-biased conditions. The diode in the reverse-biased condition has a higher operating voltage (Vop) across itself than it in the forward- biased condition. Therefore, the ESD current generates more heat on the polysilicon diode in the reverse-biased condition to cause a lower It2.

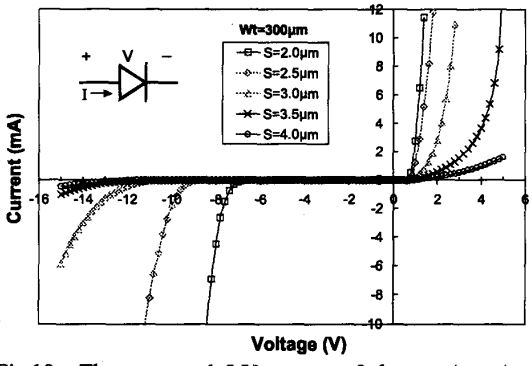
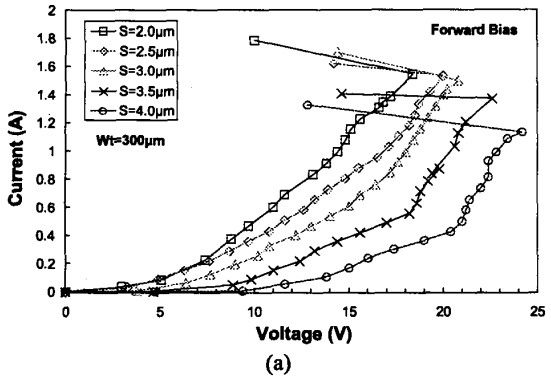
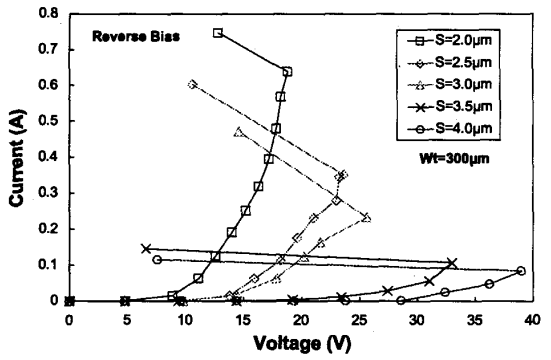


Fig.10 The measured I-V curves of the p+ / n- / n+ polysilicon diodes with a fixed Wt of 300 μm but different S spacings in a CMOS process.



(a)



(b)

Fig.11 The TLP-measured I-V curves of the polysilicon diodes, in (a) the forward-biased condition; and (b) the reverse-biased condition, with a fixed Wt of 300 μm but different S spacings.

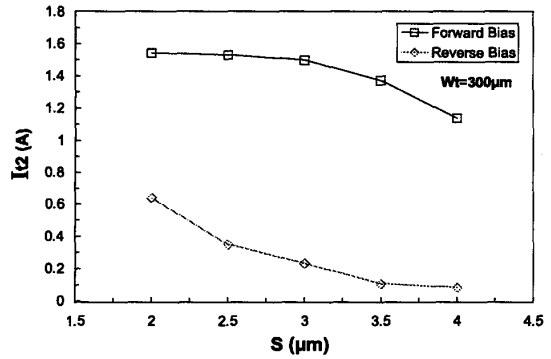
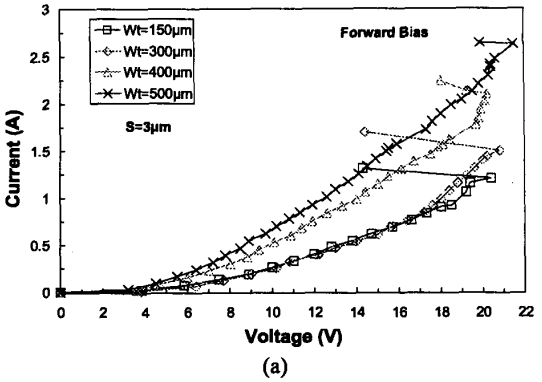
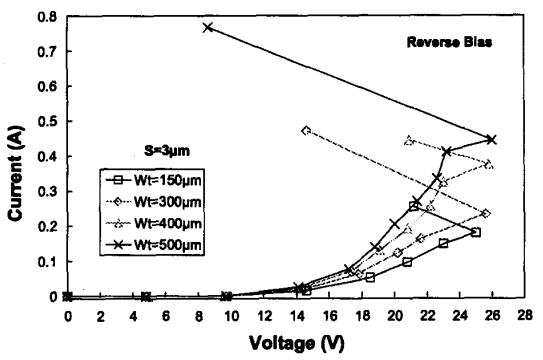


Fig.12 Dependence of the TLP-measured It2 on the layout parameter S of the polysilicon diodes in both the forward- and reverse-biased conditions.



(a)



(b)

Fig.13 The TLP-measured I-V curves of the polysilicon diodes, in (a) the forward-biased condition; and (b) the reverse-biased condition, with a fixed spacing S of 3 μm but different total perimeters Wt.

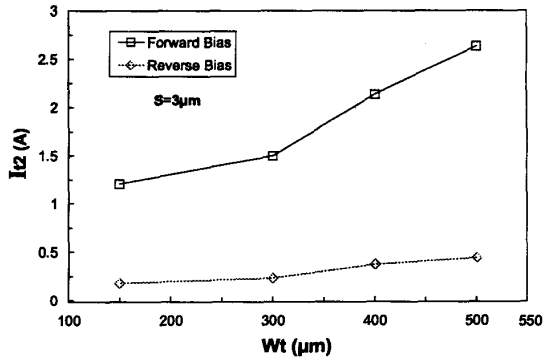


Fig.14 Dependence of the TLP-measured It2 on the layout parameter Wt (total perimeter) of the polysilicon diodes in both the forward- and reverse-biased conditions.

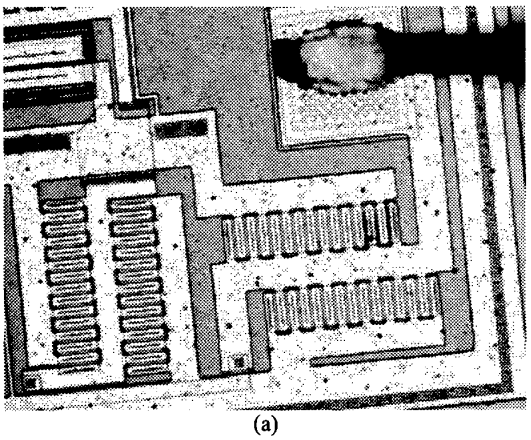
When the spacing S increases in the polysilicon diode, the It2 is also decreased, even if the diode is stressed in the forward-biased condition. In the forward-biased condition, the power ($\approx I_{ESD} \times R^2$) generated by ESD current on the polysilicon diode is mainly decided by the turn-on resistance of the diodes. A polysilicon diode with a smaller layout spacing S has a lower turn-on (breakdown) resistance, therefore it has a relatively higher It2 in the forward- (reverse-) biased condition. With well understood and detailed investigation on It2 of the polysilicon diodes under different bias conditions and layout parameters, ESD robustness of the smart card IC can be effectively improved by arranging the polysilicon diodes to discharge ESD current in its forward-biased condition. This can be achieved by designing a more efficient VDD-to-VSS ESD clamp circuit into the chip, as that shown in Fig. 7. The efficient VDD-to-VSS ESD clamp circuit should have a fast turn-on speed and a low turn-on voltage to discharge the ESD current from VDD to VSS.

5. Experimental Results and Discussion

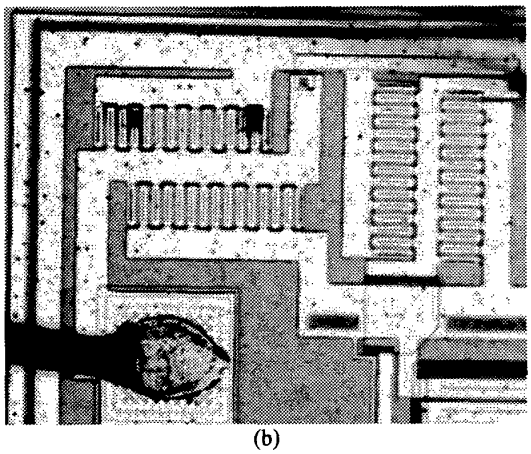
5.1 ESD Test and Failure Analysis

The smart card IC's with the polysilicon diodes and the new proposed ESD protection design in Fig. 7 have been fabricated. The polysilicon diodes realized with the n- or p- doped center regions can perform the desired circuit function for smart card application. The HBM ESD test results of this new ESD protection design with the polysilicon diodes of n- or p- doped center regions are listed in Table 4. While the polysilicon diodes are realized by the n- (p-) doped center region with a doping concentration of 9E13 (5E13) cm^{-3}, the HBM ESD-sustained level of pad1 pin in the VSS(+) ESD test mode is improved to 3kV (3.5kV). In the VDD(-) ESD test mode, the HBM ESD-sustained level is improved to >4kV (3kV). In both the VSS(-) and VDD(+) ESD test modes, the smart card IC with the polysilicon diodes can sustain the ESD-stress voltage of greater than 4kV. The HBM ESD-sustained voltage level of this smart card IC under the direct VDD-to-VSS ESD stress is also greater than 4kV.

The picture showing the failure location on the smart card IC with the p- doped polysilicon diodes after the pad1 pin is zapped with a 4-kV VSS(+) HBM ESD stress is shown in Fig. 15(a), where the ESD failure is located on the polysilicon diode Dp1a, rather than on the Dn1a or the gate oxide of input circuits. In Fig. 15(b), it shows that the ESD failure is located on the polysilicon diode Dn1a, rather than the diode Dp1a, after the pad1 pin is zapped with a 4-kV VDD(-) HBM ESD stress. From the ESD failure analysis, it has conformed that the ESD current is actually discharged through the polysilicon diodes in the forward-biased conditions. This is achieved by adding the more efficient VDD-to-VSS ESD clamp circuit into the chip, as that shown in Fig. 7. The ESD test results have successfully verified the proposed ESD protection design in the smart card IC with the polysilicon diodes.



(a)



(b)

Fig.15 The pictures to show the ESD failure location on the smart card IC with the p- doped polysilicon diodes after the pad1 pin is zapped with a 4-kV HBM ESD stress in (a) the VSS(+), and (b) the VDD(-), ESD test conditions.

Table 4

Polysilicon-Diode Doping Concentration (cm-3)	HBM ESD Level (Volt)			
	VDD(+)	VDD(-)	VSS(+)	VSS(-)
N-, 9E13	> 4kV	> 4kV	3kV	> 4kV
P-, 5E13	> 4kV	3kV	3.5kV	> 4kV

(Failure criterion : $I_{Leakage}$ > 1μA @ 5-V bias)

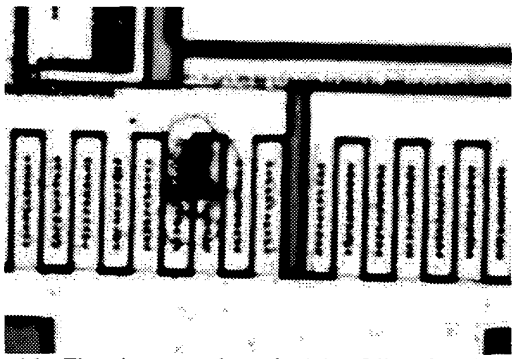


Fig.16 The picture to show the ESD failure location on the smart card IC with the n- doped polysilicon diodes after a negative 700V CDM ESD stress.

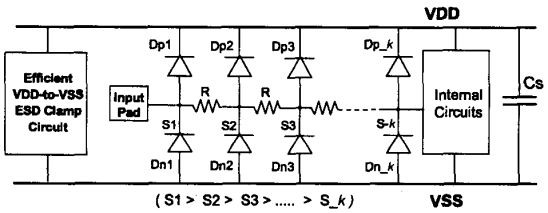


Fig.17 The alternative input ESD protection design with the polysilicon diodes in a multi-stage configuration to achieve better ESD protection.

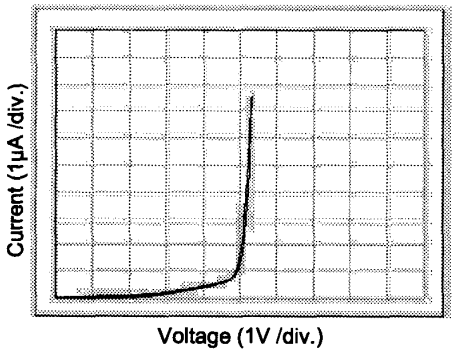


Fig.18 The measured I-V curve from VDD to VSS of the new proposed VDD-to-VSS ESD clamp circuit with 8-stacked n- doped polysilicon diodes.

The smart card IC with the n- doped polysilicon diodes has been also verified by the charged-device-model (CDM) ESD test. The maximum CDM ESD-sustained voltage level of the fabricated smart card IC is 750V and 600V in the positive and negative CDM stresses conditions, respectively. The picture to indicate the ESD failure location on the smart card IC with the n- doped polysilicon diodes after a negative 700V CDM ESD stress is shown in Fig. 16, where the ESD failure is located on the polysilicon diode Dn1a, not on the gate oxide of the first input stage. To sustain a higher CDM ESD level, the layout spacing S of the lightly doped center region has to be reduced to lower the breakdown voltage and to decrease the ESD-generated heat on the polysilicon diodes. The polysilicon diode with a reduced spacing S also has a faster turn-on speed and a smaller turn-on resistance. But, the minimum breakdown voltage of the polysilicon diode in this smart card application is limited to 12V, due to the coupled maximum AC voltage. This requirement can be further achieved by arranging the polysilicon diodes into the multi-stage configuration [5], as that shown in Fig. 17. The polysilicon diode in every stage has different layout spacing S. The polysilicon diode close to the first input stage of the internal circuits has a narrower spacing S, but the polysilicon diode close to the bond pad has a wider spacing S. The resistance R between every stage can be further reduced to improve CDM ESD level but without degrading its HBM ESD level.

5.2 Turn-on Verification

The I-V curve of the new proposed VDD-to-VSS ESD clamp circuit with 8-stacked n- doped polysilicon diodes is measured in Fig. 18. When the applied voltage across VDD and VSS is increased higher to bias the gate of Mn3 greater than its threshold voltage, the NMOS Mn3 is turned on to conduct current from VDD to VSS. So, the measured I-V curve in Fig. 18 has a sharp current increase when the applied voltage is greater than 5V.

In order to investigate the turn-on efficiency of the polysilicon diodes at the pad1 (Fig. 7) with the help of the new proposed VDD-to-VSS ESD clamp circuit, a 0-to-8V voltage pulse is directly applied to the pad1 with the VSS pin relatively grounded. The original 0-to-8V voltage pulse is generated from a pulse generator with a pulse width of 4μs and a rise time of ~10 ns, as the dashed line shown in Fig. 19. When such a voltage pulse is applied to the pad1, it is clamped to the voltage level shown in Fig. 19.

Because the polysilicon diodes of pad1 have a breakdown voltage around 12V, the applied 8-V voltage does not cause any breakdown on the polysilicon diodes of pad1. But, the 0-to-8V voltage pulse is actually clamped to about 6.5V in Fig. 19. This is due to the turn-on of the VDD-to-VSS ESD clamp circuit. Therefore, the overstress voltage on the pad1 is discharged from the pad1 to VDD through the forward-biased polysilicon diode, and then discharged to VSS through the turned-on VDD-to-VSS ESD clamp circuit. This has successfully verified the effectiveness of the new proposed VDD-to-VSS ESD clamp circuit with the stacked polysilicon diodes to significantly improve ESD level of the I/O pad.

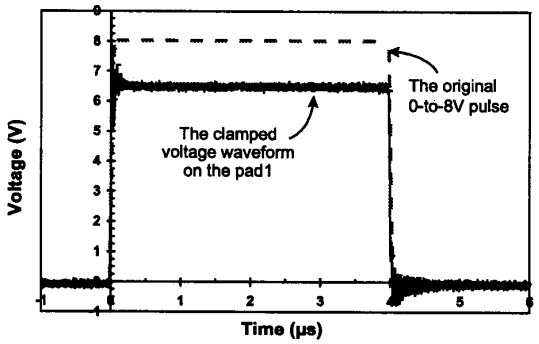


Fig.19 The measured voltage waveform at the pad1 when a 0-to-8V voltage pulse is applied to the pad1 with the VSS grounded.

6. Conclusion

The device characteristics of the polysilicon diodes in CMOS process has been experimentally evaluated by process splits with different doping concentrations. The It2 of the polysilicon diodes under different bias conditions and different layout parameters has been clearly investigated. The HBM ESD level of the smart card IC with the polysilicon diodes as ESD protection devices has been successfully improved up to ≥ 3kV in cooperation with a more efficient VDD-to-VSS ESD clamp circuit. Such ESD-improved smart card IC's have been in mass production with a large sale volume to offer smart card manufacturability without any ESD problem.

Acknowledgement

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