Compact Layout Rule Extraction for Latchup Prevention in a 0.25-μm Shallow-Trench-Isolation Silicided Bulk CMOS Process

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Abstract

An experimental extraction to find the area-efficient compact layout rules to prevent latchup in bulk CMOS IC's is proposed. The layout rules are extracted from the test patterns with different layout spacings or distances. A new efficient latchup prevention design, by adding the additional internal guard rings between the I/O cells and the internal core circuits, has been successfully proven in a 0.25-μm shallow-trench-isolation (STI) silicided bulk CMOS process. Through detailed experimental verification including temperature effect, the proposed extraction method to define compact layout rules has been established to save the silicon area of CMOS IC's, but still to maintain high enough latchup immunity in bulk CMOS IC's.

1. Introduction

Latchup, one of the main reliability concerns in the bulk CMOS IC's, is formed by the parasitic p-n-p-n structure between the VDD and VSS of CMOS circuits [1]-[3]. This parasitic structure inherently exists in the bulk CMOS technology. When the parasitic p-n-p-n structure is triggered to cause latchup, it generates a low impedance path from VDD to VSS and a high current to burn out the chip. The device cross-sectional view of a latchup path in a p-substrate bulk CMOS technology is shown in Fig. 1(a), where the 1st-order equivalent circuit of the latchup path is illustrated in Fig. 1(b). The latchup equivalent circuit is formed by a vertical p-n-p BJT (Qpnp) coupled with a lateral n-p-n BJT (Qnpn). When one of the BJT's is turned on, the mechanism of positive feedback regeneration in the latchup structure will be initiated [3]. If the product of beta gains of these two BJT's can be kept greater than one, the p-n-p-n structure will hold in a stable latching state [1]-[3].

To prevent the occurrence of latchup in CMOS IC's, some advanced process technologies (such as the epitaxial substrate, retrograde well, trench isolation, or silicon-on-insulator) had been reported to increase the holding voltage of the parasitic p-n-p-n structures [1]. Although such advanced techniques can effectively solve the latchup issue in CMOS IC's, the fabrication cost of CMOS IC's with such advanced techniques becomes more expensive. Thus, the most consumer IC products are still manufactured by bulk CMOS processes. In the bulk CMOS process, the latchup issue is mainly prevented by the guard rings, which has been specially specified in the design rules of a given CMOS process. The wider guard rings used to surround the I/O devices in the I/O cells of CMOS IC's generally cause a higher latchup immunity, but they also occupy a larger layout area.

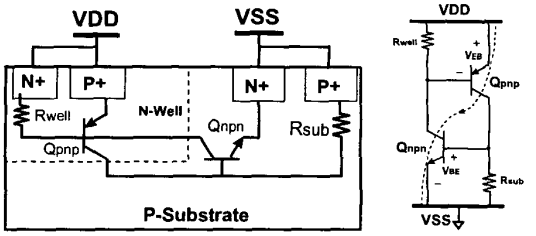

Fig. 1 (a) The cross-sectional view, and (b) the equivalent circuit, of the latchup structure in a p-substrate bulk CMOS technology.

When more complex functions and circuit blocks are integrated into a single chip, a CMOS IC often has the pin count of several hundreds. Especially, in the communication IC's or chip set IC's, more I/O pins are designed to provide the desired system connections. In such high-pin-count IC's, the whole chip size is often decided by the pad-limited effect but no longer the core-limited effect. Therefore, the pad pitch is critically limited to reduce the total chip size of a high-pin-count CMOS IC. To further reduce the pad pitch for high-pin-count CMOS IC's, the staggered bond pad had been widely used in CMOS IC's to reduce the whole chip size. With the staggered bond pad design, the layout pitch for a corresponding I/O cell has been scaled down

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to only ~50μm. With such a narrow layout pitch, the cell height of an I/O cell including the output buffer circuit (or ESD protection circuit) and the latchup guard rings becomes much longer. The much longer cell height of the I/O cells causes a more increase on the whole chip size. Therefore, the compact layout rules for I/O cells to prevent latchup are highly demanded by the high-pin-count CMOS IC's.

In this paper, a new extraction method to define compact layout rules for latchup prevention and therefore to save the chip size is proposed. An experimental setup to observe the latchup occurrence in time domain, during the triggering of the applied trigger current at I/O pin but fire latchup in internal core circuits, is also demonstrated.

2. Design Rules and Latchup Test

In CMOS circuits, the latchup p-n-p-n path exists from the source (p+ diffusion connected to VDD) of a PMOS, through the n-well and p-substrate, to the source (n+ diffusion connected to VSS) of an NMOS. Therefore, there are many parasitic p-n-p-n paths existing in CMOS circuits, because the CMOS logics always have many PMOS devices connected to VDD and NMOS devices connected to VSS. If one of such parasitic p-n-p-n paths between VDD and VSS is firing, it causes the latchup problem to burn out the CMOS IC. Latchup can occur at the I/O cells or at the internal circuits of a CMOS IC, because the parasitic latchup p-n-p-n paths exist in both I/O cells and internal circuits of a CMOS IC. In the bulk CMOS IC's, the latchup prevention is achieved by adding the guard rings in the I/O cells and placing the substrate/well pickups in the internal circuits.

2.1. Design Rules

To define the latchup layout rules in CMOS process, some test structures with different layout spacings had been used to investigate the latchup immunity [4]-[8]. The typical latchup test structure to define the layout rules on the n-well or p-substrate pickups for internal core circuits is shown in Fig. 2 [4], where the trigger nodes are drawn in the p-substrate or the n-well of the test structure. The test structures are drawn with different distances (*Xp*, *Xn*) between two adjacent pickups, or with different distances (*hp*, *hn*) from the pickups to the n-well edge. By applying different trigger current or voltage into the trigger nodes of the test structure, where the p-n-p-n path is biased at a desired VDD voltage level, the threshold trigger current to initiate latchup occurrence in the test structure can be found.

The I/O cells, which are connected to the bond pads in CMOS IC's, are often triggered by the external overshooting or undershooting voltage/current glitches. Therefore, the double guard rings are often specified in the design rules to prevent latchup in the I/O cells. The test structure used to investigate the layout rules of double guard rings for I/O cells is shown in Fig. 3 [7]. The test structures are drawn with different widths of the guard rings or different distances between the guard rings to extract the layout rules for I/O cells. With suitable layout rules on the double guard rings to surround the NMOS and PMOS in the I/O cell layout, the latchup p-n-p-n path in such an I/O cell is blocked by the guard rings. Therefore, the holding voltage of the parasitic p-n-p-n path in such an I/O cell can be increased up to greater than VDD voltage level of the CMOS IC. With a holding voltage greater than VDD, the parasitic p-n-p-n path in the I/O cell becomes free to latchup.

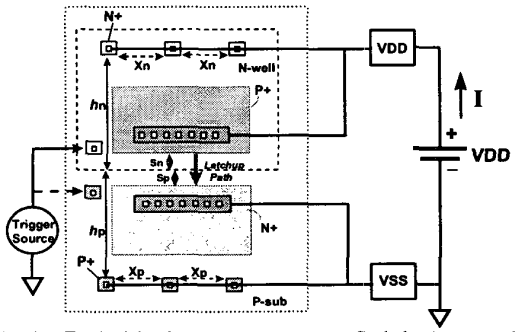


Fig. 2 Typical latchup test structure to find the layout rules on the substrate and well pickups for using in the layout of internal circuits of CMOS IC.

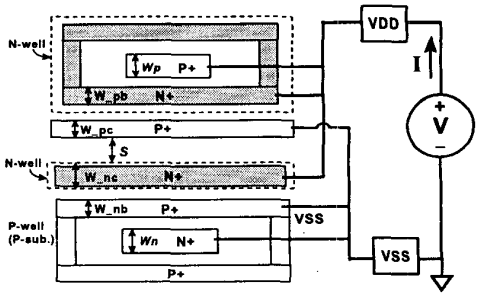


Fig. 3 Test structure to find the layout rules on the double guard rings for I/O cells in the bulk CMOS process.

2.2. Latchup Test

To verify the latchup immunity of a CMOS IC, an overshooting (positive) current or undershooting (negative) current are applied to every I/O pin of a CMOS IC to investigate whether the latchup is fired, or not. The detailed latchup test procedure and specifications had been clearly specified in the EIA/JEDEC Standard No. 78 [9]. The schematic

diagram to show such latchup test on an output pin is illustrated in Fig. 4(a). If the CMOS IC is fired into latchup by the trigger current applied on the I/O pin, the current flowing from VDD power supply has an obvious increase. The obvious increase on the VDD current can be detected by the latchup tester to judge the occurrence of latchup.

In Fig. 4(a), the overshooting/undershooting trigger current on the pad is conducted into the drain regions of the output devices. When the overshooting (undershooting) current is applied to the I/O pin, the P+ drain / n-well (N+ drain / p-substrate) junction in the output PMOS (NMOS) is forward biased to further generate the trigger current into the substrate. This substrate current, indicated by the gray dashed line in Fig. 4(a), can fire the latchup paths in the I/O cell or in the internal circuits.

Latchup in CMOS IC's is also sensitive to voltage transition on VDD supply [10]-[11]. To verify the latchup immunity of CMOS IC's due to such power-transient trigger, the test configuration is illustrated in Fig. 4(b). The trigger voltage is added onto the VDD power supply of the CMOS IC under test, and the current flowing from the VSS pin of the CMOS IC is monitored by the latchup tester. The power-transition trigger voltage often generates the displacement current through the junction capacitance into the n-well and p-substrate to fire the latchup paths in the CMOS IC. If the CMOS IC is fired into latchup by the trigger voltage on the VDD pin, the current flowing out from VSS pin has an obvious increase. In general, CMOS IC's for consumer applications should not be triggered into latchup by a trigger current of ±100mA on the I/O pins or a trigger voltage of 1.5×VDD on the VDD pin [9].

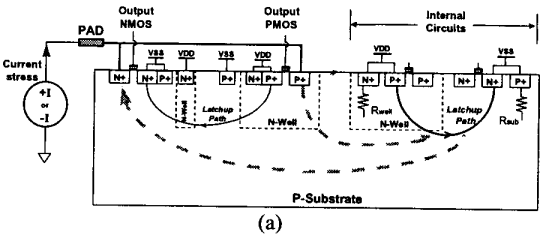
3. Compact Layout Rules Extraction

3.1. Layout Rules Design for I/O Cells

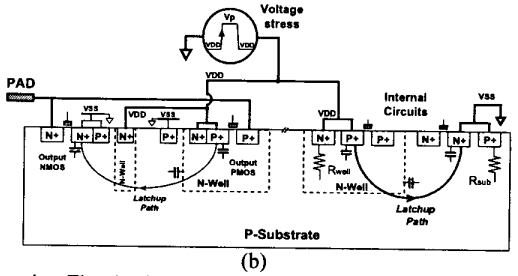
To avoid the latchup paths in I/O cells fired by the overshooting or undershooting current on the I/O pins, the double guard rings are often used to block the latchup path between the PMOS and NMOS in the I/O cells. However, the wider double guard rings surrounding the I/O cells often occupy more layout area in CMOS IC's.

To further reduce layout area of the I/O cell for high-pin-count applications, one set of I/O cells with double guard rings, single guard ring, or no guard ring, are drawn with different anode-to-cathode distances between the output PMOS and NMOS to investigate their latchup immunity. The testchip for I/O cells with double guard rings, single guard ring, or no guard ring in a 0.25-μm shallow-trench-isolation silicided bulk CMOS process is shown in Fig. 5.

If the holding voltage of the parasitic p-n-p-n path in the I/O cell is increased greater than VDD by a compact guard ring design, the I/O cell can be free to latchup. The I-V characteristics of the latchup paths in such test structures with different guard ring designs are measured and shown in Section 4.



(a)



(b)

Fig. 4 The latchup test for a CMOS IC with (a) the overshooting or undershooting trigger current at each I/O pin, and (b) the voltage-transient trigger at the VDD pin.

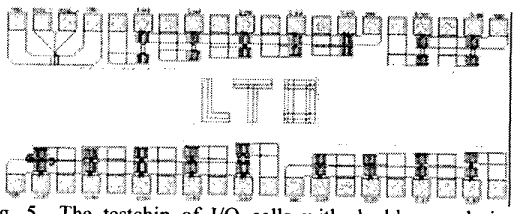


Fig. 5 The testchip of I/O cells with double guard rings, single guard ring, or no guard ring to investigate compact layout rules for latchup prevention in the I/O cells.

3.2. Layout Rules Design for Internal Circuits

The I/O cells can be free to latchup if suitable guard rings are added in the I/O cells, but the internal circuits in the bulk CMOS IC's are still sensitive to latchup. As shown in Fig.4(a), the overshooting or undershooting trigger currents applied at the I/O pins will generate substrate current to cause latchup occurrence in the internal circuits. To avoid the substrate current generated from the I/O cells to fire latchup in the internal circuits, the internal circuits should keep an enough distance away from the I/O cells. To investigate the suitable distance from the I/O cells to the internal circuits, a new test method is proposed in Fig. 6.

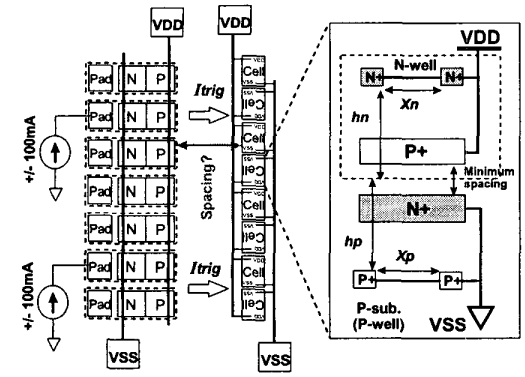


Fig. 6 A new test method to find layout spacing from the I/O cell to internal circuits and the pickup distances in the internal circuits.

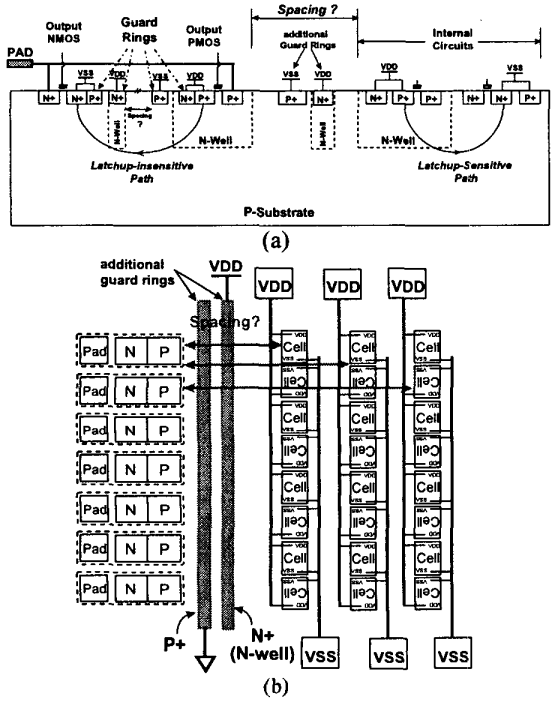


Fig. 7 (a) The cross-sectional view, and (b) the schematic layout, of the additional internal guard rings placed between the I/O cells and the internal circuits to avoid latchup in internal circuits.

The latchup sensor cells (zoomed in the box) are especially drawn and placed in parallel to the I/O cells. The latchup sensor cells with specified pickup distances (*Xn*, *hn*, *Xp*, *hp*) are used to simulate the latchup structure in the internal circuits. When the trigger current is applied at the I/O pins, the VDD that connected to the latchup sensor cells is monitored to judge whether latchup is triggered on, or not. The threshold trigger current applied at the I/O cells to fire latchup in the internal circuits (simulated by the latchup sensor cells) can be measured by this new test method. Thus, the design rules on the pickup distances (*Xn*, *hn*, *Xp*, *hp*) for internal circuits can be extracted more meaningfully to meet the actual circuit operating condition in CMOS IC's.

To further reduce the distance between the I/O cells and the internal circuits to save layout area, the additional guard rings are proposed to be placed between the I/O cells and the internal circuits, as those shown in Figs. 7(a) and 7(b). The additional p+ diffusion (n+ diffusion with n-well) guard ring is used to collect the hole (electron) current, generated from the I/O cells, in the substrate before they may reach the internal circuits to fire latchup. In order to find such important layout rules on the additional internal guard rings between the I/O cells and internal circuits, some testchips are drawn and fabricated with different layout spacings in the 0.25-μm bulk CMOS process. The I/O cells in such testchips are only surrounded by single guard ring.

4. Experimental Results

4.1. I-V Characteristics of the I/O Cells

The I-V characteristics of the I/O cells with double guard rings, single guard rind, and no guard ring fabricated in the 0.25-μm STI silicided bulk CMOS process are measured by the *Tek*370A curve tracer. The holding voltages of these I/O cells are used to define their latchup hardness. If the holding voltage of the I/O cells greater than VDD, the I/O cell is latchup-free. Moreover, a *ThermoChuck* system with a temperature range up to 200°C and a temperature accuracy of ± 0.5°C is used to investigate the latchup behaviors of the testchips under different temperatures.

The measured I-V characteristics of the I/O cell with single guard ring at a temperature of 30°C and a anode-to-cathode spacing of 17.7μm is shown in Fig. 8(a), where it has a holding voltage of 13.8V in the 0.25-μm STI silicided bulk CMOS process. The I-V characteristics of the I/O cell with no guard ring at a temperature of 125°C and a anode-to-cathode spacing of 5μm is shown in Fig. 8(b), where it has a holding voltage of only 2.46V in this 0.25-μm process.

The relations between the holding voltage and the anode-to-cathode spacing for the I/O cells with different guard rings design at the temperature of 125°C in the 0.25-μm STI silicided bulk CMOS process are shown in Fig. 9. In Fig. 9, the I/O cell with single guard ring and the anode-to-cathode spacing from 17.7 μm to 55.7 μm has a holding voltage about ~13.8V, which is much higher than VDD (3.3V) of CMOS IC in this 0.25-μm CMOS process. The I/O cell with double guard rings has

no higher holding voltage than that only with single guard ring. Therefore, the I/O cells in this 0.25-μm bulk CMOS process drawn with only single guard ring are enough to prevent latchup and to save layout area.

4.2. I-V Characteristics of the Internal Circuits

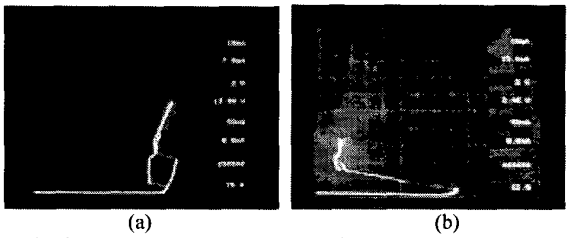
The I-V characteristics of the test structures to simulate latchup path in the internal circuits with different pickups distances (*Xp*, *Xn*, *hp*, and *hn*, as shown in Fig. 2) are measured by the *Tek*370A curve tracer. The measured I-V curve of the latchup test structure with a pickup distance of 15μm in this 0.25-μm STI silicided bulk CMOS process is shown in Fig. 10. The holding voltage in Fig.10 is 1.6V at a temperature of 30°C, but it reduces to only 1.2V when the environment temperature is increased up to 125°C.

The holding voltages of the latchup test structures with different distances between two adjacent pickups for internal circuits in this 0.25-μm CMOS process are also investigated. But, the distances between two adjacent pickups don't significantly increase the holding voltage of latchup test structures. All the holding voltages of the latchup test structures with different pickup rules are around 1~2 V at the room temperature, which is smaller than VDD. Therefore, the internal circuits drawn only with well/substrate pickups are always sensitive to latchup.

4.3. Latchup Occurrence at Internal Circuits Due to the Trigger Current at I/O Pins

From above measured results, the I/O cell with single or double guard rings has a holding voltage much greater than VDD. Therefore, the I/O cells with guard rings can be free to latchup in CMOS IC. But, the internal circuits with pickups are still sensitive to latchup, because the holding voltage of the parasitic p-n-p-n paths in the internal circuits with the specified pickup rules is still about 1~2V, as that shown in Fig. 10. In the latchup test, as shown in Fig. 4(a), the trigger current applied to the I/O pin will generate the substrate or well currents to fire latchup in the internal circuits, even if the I/O cells have no latchup problem.

The experimental setup shown in Fig. 11 is used to investigate the trigger current at I/O pins but cause latchup in the internal circuits. The *Keithley* 2410 current source with a current source range from ± 50pA to ± 1.05A is used to provide the required current pulse at the I/O cells. Three independent DC power supplies are used to bias the I/O cells, the internal guard rings, and the latchup sensor cells, separately. The testchips are designed with different spacings from the I/O cells to the internal latchup sensor cells. The latchup sensor cells are the same as the latchup test structures with specified pickups to simulate the latchup path in the internal circuits. A resistor of 100 ohm is connected between the VDD power supply and internal latchup sensor cells to limit the large latchup current to burn out latchup sensor cells.



(a) (b)

Fig. 8 The measured I-V characteristics of the I/O cells with (a) single guard ring at a temperature of 30°C, and (b) no guard ring at a temperature of 125°C. (X axis= 2V/div.; Y axis= 10mA/ div.)

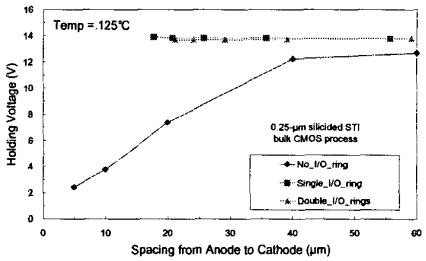


Fig. 9 The relations between the holding voltage and the anode-to-cathode spacing for the I/O cells with different guard rings design at the temperature of 125°C in a 0.25-μm STI silicided bulk CMOS process.

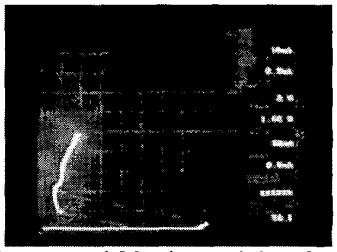


Fig. 10 The measured I-V characteristics of a latchup test structure at a temperature of 30°C for internal circuits with pickups to prevent latchup . (X axis= 2V/div.; Y axis= 10mA/div.)

The *HP*54602A oscilloscope is used to monitor the voltage waveform of the input current pulse on the I/O pin (CH1) and the voltage across the latchup sensor cells (CH2). If latchup is fired in the internal latchup sensors by the trigger current applied at the I/O pins, the voltage level of CH2 will drop from VDD to the voltage level around the holding voltage (~1.6V) of the latchup sensors. By adjusting the current magnitude of the trigger current applied at the I/O pins, the critical

(threshold) trigger current at the I/O pins to fire latchup in the internal latchup sensors can be found.

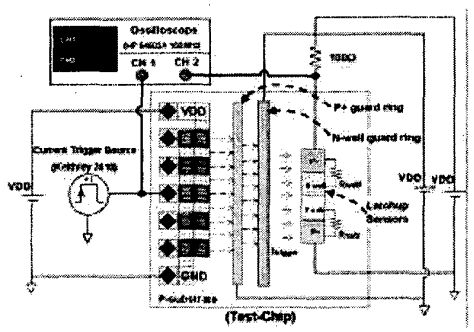


Fig. 11 The experimental setup used to find the relation that the trigger current applied at the I/O pin but to fire latchup in the internal circuits.

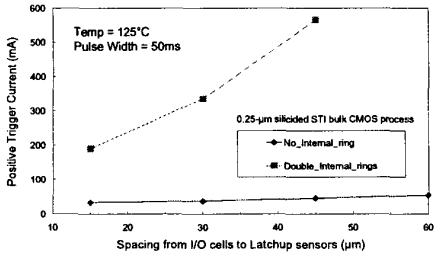


Fig. 12 The relations between the positive trigger current at the I/O pins to fire latchup in the internal latchup sensors and the layout spacing from the I/O cells to latchup sensors with or without the additional internal guard rings.

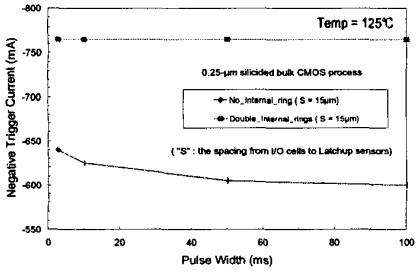


Fig. 13 The relation between the negative trigger current at the I/O pins to fire latchup in the internal latchup sensors and the pulse width of the trigger current with or without the additional internal guard rings.

The test patterns with or without the additional internal double guard rings are also verified in this 0.25-μm shallow-trench-isolation silicided bulk CMOS process, and the measured results are shown in Figs. 12 and 13 at the temperature of 125°C. The I/O cells in these testchips are all drawn with only single guard ring to surround the NMOS and PMOS. In Fig. 12, the positive threshold trigger current at the I/O pins to fire latchup in the internal circuits can be increased from the original 38mA to become 335mA by the additional internal guard rings, when the test pattern has a fixed spacing of 30μm from the I/O cells to internal circuits. In Fig.13, the relation between the magnitude and the pulse width of threshold negative trigger current at the I/O pins to fire latchup in the internal circuits is investigated, when the test pattern has a fixed spacing of 15μm from the I/O cells to the internal circuits. From Figs. 12 and 13, the efficiency of the additional internal guard rings to prevent latchup has been successfully proven.

5. Conclusion

A new extraction method has been proposed and experimentally proven to find the compact layout rules for latchup prevention in bulk CMOS processes. The I/O cells with single guard ring can have holding voltages greater than VDD. But, the internal circuits even drawn with narrower pickup rules are still sensitive to latchup. Moreover, the additional internal guard rings added between the I/O cells and the internal circuits can significantly increase latchup immunity of internal circuits in bulk CMOS IC's.

6. References

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