Design on ESD Protection Circuit with Very Low and Constant Input Capacitance

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Research Motivation

Effective on-chip ESD design to solve the ESD protection challenge on the analog pins for high-frequency or current-mode applications is studied. The device dimension of ESD clamp devices in analog ESD protection circuit can be reduced to have a much small input capacitance for high-frequency applications, but it can still sustain a high HBM and MM ESD level. To find the optimized device dimensions and layout spacings on ESD clamp devices, a design model is developed to keep the input capacitance as constant as possible (within 1% variation).

1. Technical Background

Efficient input electrostatic discharge (ESD) protection circuit should be designed and placed on every input pad to clamp the ESD overstress voltage across the gate oxide of input circuits. A conventional ESD protection design with the two-stage structure for digital input pin is shown in Fig.1, where a gate-grounded short-channel NMOS is used as the secondary protection device to clamp the overstress voltage across the gate oxide of the input circuits. To provide a high ESD level, a robust device (such as SCR, field-oxide device, or long- channel NMOS) is used in the primary protection stage to discharge ESD current. Between the primary stage and the secondary stage of the input ESD protection circuit, a resistor is added to limit the ESD current flowing through the secondary ESD clamp device. The resistance value of this resistor is dependent on the turn-on voltage of the primary ESD clamp device and the It2 (secondary breakdown current) of the secondary ESD clamp device. Such resistance was designed large enough (in the order of kΩ [1]), so the primary ESD clamp device can be triggered on to bypass ESD current before the secondary ESD clamp device was damaged by ESD. Such two-stage ESD protection design can provide high ESD level for the digital input pins. But the large series resistance and the large junction capacitance in the ESD clamp devices cause a long *RC* time delay to the input signals, it is not suitable for analog pins, especially for the high-frequency or current-mode applications.

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For current-mode input signal or GHz applications, the series resistance between the input pad and input circuits is forbidden. Therefore, the two-stage ESD protection design in Fig.1 is no longer suitable for analog input pins. To protect the analog input pin, the typical ESD protection circuit with a single-stage ESD protection design is shown in Fig.2, where a gate-grounded NMOS (ggNMOS) is used as the ESD clamp device. Because ESD robustness of NMOS is seriously degraded by the advanced deep-submicron CMOS technologies [2], such a ggNMOS is often designed with a larger device dimension to sustain an acceptable ESD level. But the ggNMOS with a larger device dimension contributes a larger parasitic drain capacitance to the input pad. Such a parasitic junction capacitance is nonlinear and dependent on the input voltage level. This nonlinear input capacitance can cause serious distortion on the analog circuit performance or resolution, such as the harmonic distortion [3]. Thus, it has become an emergent challenge to design an effective ESD protection circuit for high-performance analog input and output pins.

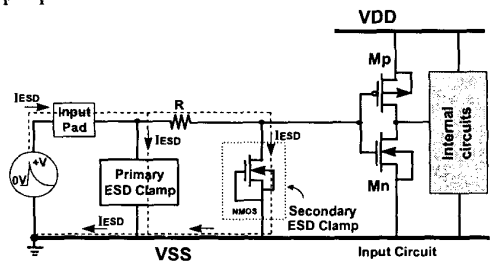

Fig.1 The traditional two-stage ESD protection circuit for digital input pin in CMOS IC's.

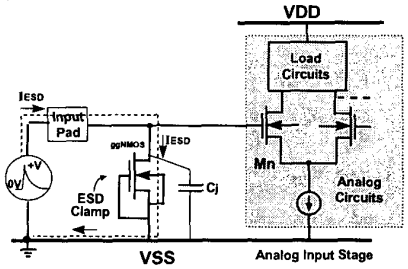

Fig.2 The traditional single-stage ESD protection circuit for analog input pin in CMOS IC's.

2. Research Goals

In this research, an effective ESD protection design with the requests of small input capacitance, no series resistance, constant input capacitance, and high ESD level, is studied to protect the analog pins for high-frequency and high-precision analog applications.

3. Brief Results

3.1. ESD Protection Circuit for Analog Pin

The ESD protection circuit for high-frequency analog pins has been studied, and one of the solutions is shown in Fig. 3. The design and operation principles of this analog ESD protection circuit had been described in [4] in details. The device dimension (W/L) of ESD clamp device connected to the I/O pad in the analog ESD protection circuit can be reduced to only 50/0.5 (μm/μm) in a 0.35-μm silicided CMOS process. The HBM (human-body model) and MM (machine model) ESD test results are summarized in Table 1. As shown in Table 1, the proposed analog ESD protection circuit can successfully provide analog input pins with an HBM (MM) ESD level of above 6000V (400V). With such a smaller device dimension, the input capacitance of this analog ESD protection circuit can be significantly reduced to only ~1.0 pF (including the bond pad capacitance) for high-frequency applications.

3.2. Design to Minimize Capacitance Variation

When the layout spacings in Mn1 and Mp1 are modified, the total input capacitance of the proposed analog ESD protection circuit can be adjusted. The desired layout parameters to minimize the variation on the input capacitance within the specified input voltage range had been studied in [5]. By choosing the device parameters and layout spacings of Mn1 and Mp1, the condition to keep the input capacitance with a minimum variation under the voltage condition of V_{DD}=3V and an input voltage swing of 1.5V±0.5V had been found as [5]

$$k_n \cdot \{1.029515\times10^{-4}\cdot G_n\cdot X_n + 1.098674\times10^{-11}\cdot G_n + 2.204072\times10^{-11}\cdot X_n\} = k_p \cdot \{2.011205\times10^{-4}\cdot G_p\cdot X_p + 1.156346\times10^{-11}\cdot G_p + 4.762930\times10^{-11}\cdot X_p\} \quad (1)$$

If the layout parameters (K_n, K_p, G_n, G_p, X_n, and X_p) on the Mn1 and Mp1 devices are correctly chosen to meet this equation (1), the input capacitance of the proposed analog ESD protection circuit can have a minimum variation within the desired input voltage range. The typical calculated result is shown in Fig.4, where the variation on the input capacitance is smaller than 1%. It is quite useful for real circuit design that the variation on the input capacitance of the proposed analog ESD protection circuit can be minimized by simply choosing the suitable device dimensions and layout spacings in the Mn1 and Mp1 devices for a given CMOS process.

Table 1

	Pin Combination in ESD Test				
	PS-mode	NS-mode	PD-mode	ND-mode	Pin-to-Pin
HBM (V)	6000	-8000	7000	-7000	6000
MM (V)	400	-400	400	-400	400

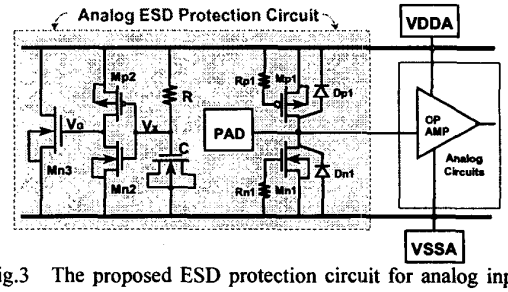

Fig.3 The proposed ESD protection circuit for analog input pins.

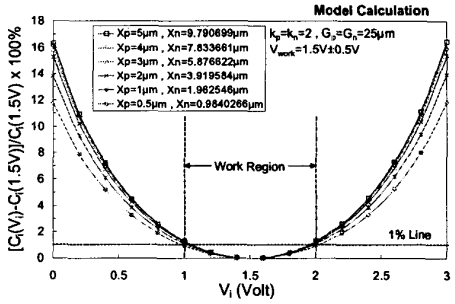

Fig. 4 The relation between the variation percentage on the input capacitance and the input voltage level under different layout parameters X_n and X_p.

4. Conclusion

A design model to find suitable layout parameters for minimizing the capacitance variation had been derived. The proposed analog ESD protection circuit with small and constant input capacitance, as well as a high ESD level, had been practically applied in tsmc I/O cell libraries and successfully used in many IC products.

5. References

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