ESD PROTECTION DESIGN IN A 0.18-μm SALICIDE CMOS TECHNOLOGY BY USING SUBSTRATE-TRIGGERED TECHNIQUE

Ming-Dou Ker, *Tung-Yang Chen*, *and Chung-Yu Wu*

Integrated Circuits & Systems Laboratory, Institute of Electronics
National Chiao Tung University, Hsinchu, Taiwan

ABSTRACT

A novel substrate-triggered technique, as comparing to the traditional gate-driven technique, is proposed to effectively improve ESD (electrostatic discharge) robustness of IC products. The on-chip ESD protection circuits designed with the substrate-triggered technique for input, output, and power pads have been fabricated and verified in a 0.18-μm salicide CMOS process. The HBM ESD level of the ESD protection NMOS with a W/L of 300μm/0.3μm can be improved from the original 0.8kV to become 3.3kV by this substrate-triggered technique.

1. INTRODUCTION

ESD level of commercial IC products is generally requested to be higher than 2kV in the human-body-model (HBM) [1] ESD stress. Therefore, on-chip ESD protection circuits had been built on the chip to protect the devices and circuits against ESD damages. To sustain the requested ESD overstress without causing damage in IC, on-chip ESD protection circuits are often drawn with larger device dimensions. With a large device dimension, the ESD protection NMOS is often realized by multiple fingers in layout. But, during the ESD stress, the multiple fingers of ESD protection NMOS cannot be uniformly turned on. Only several fingers of the NMOS were turned on and therefore damaged by ESD [2]. This often causes a low ESD level, even if the NMOS has a large device dimension. To improve the turn-on uniformity among the multiple fingers, the gate-driven design had been widely used to increase ESD level of the large-device-dimension NMOS [2], [3].

Recently, ESD level of the gate-driven NMOS had been found to be decreased dramatically when the gate voltage is somewhat increased [4-6]. The gate-driven design causes ESD current flowing through the surface channel of NMOS, therefore NMOS becomes more sensitive to be burned out by ESD energy.

In this paper, a novel substrate-triggered technique is proposed to significantly increase ESD level of the ESD protection NMOS in a 0.18-μm salicide CMOS process. The comparison between the gate-driven and substrate-triggered effects on the It2 of NMOS has been first reported.

2. GATE-DRIVEN AND SUBSTRATE-TRIGGERED EFFECTS

2.1 Structures of ESD Protection Devices

To investigate ESD robustness, the device cross-sectional views and corresponding finger-type layout patterns of the traditional gate-driven and the new proposed substrate-triggered NMOS's are shown in Fig.1 and Fig.2, respectively. Such NMOS's with different channel widths but a fixed channel length of 0.3μm are fabricated in a 0.18-μm salicide CMOS process [7] with silicide-blocking mask.

In Fig.2, a p+ diffusion is located in the center of NMOS device. This p+ diffusion is used as the substrate-triggered point of ESD protection device. And two N-wells are diffused in the source regions of this device as shown in Fig.2 to form higher substrate resistances. Then this device can be applied in substrate-triggered design.

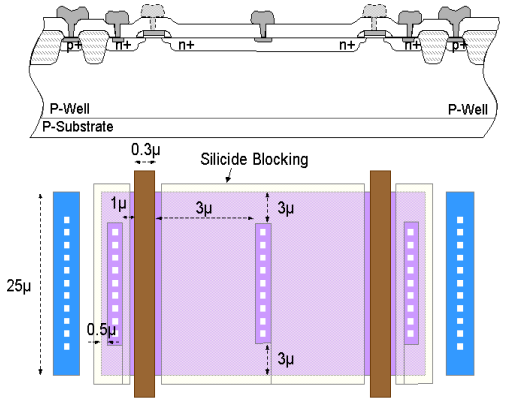


Fig. 1. Device structure and layout pattern of the traditional finger-type NMOS used as the ESD protection device.

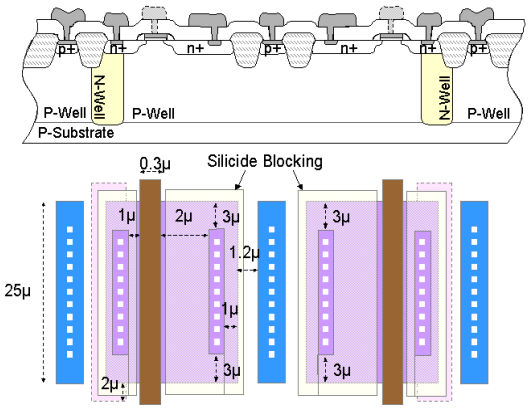


Fig. 2. Device structure and layout pattern of the proposed substrate-triggered NMOS.

2.2 Characteristics of ESD Protection Devices

The I-V curves of the fabricated substrate-triggered NMOS under different substrate biases are measured in Fig.3. The TLPG

This work was supported by the National Science Council (NSC), Taiwan, R.O.C., under the Grant NSC-89-2215-E-009-103; and partially supported by TSMC.

(transmission line pulse generator) with a pulse width of 100nS is used to find the It2 (second breakdown current) of the fabricated NMOS's under different gate or substrate biases. The TLPG-measured I-V curves of NMOS under different gate (substrate) biases are shown in Fig.4 (Fig.5). The dependence of It2 on the gate (substrate) biases is shown in Fig.6 (Fig.7).

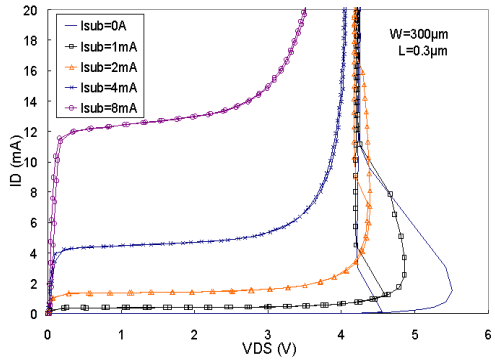


Fig. 3. The I-V curves of the substrate-triggered NMOS under different substrate current biases.

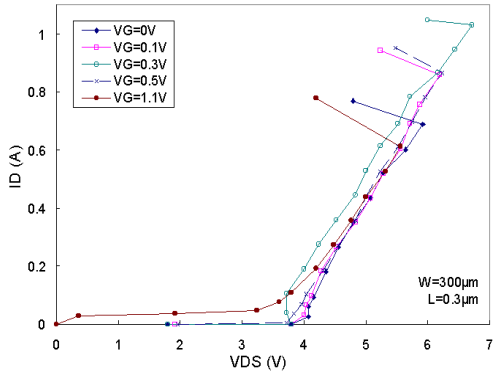


Fig. 4. The TLPG-measured I-V curves of the traditional finger-type NMOS under different gate biases.

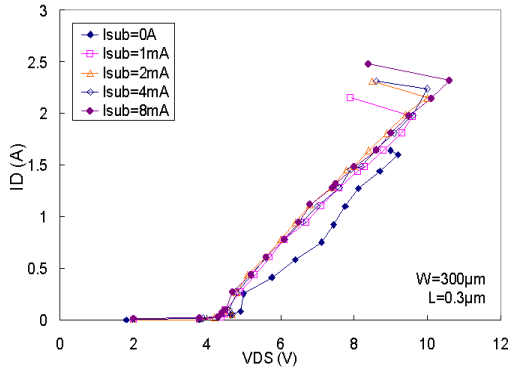


Fig. 5. The TLPG-measured I-V curves of the substrate-triggered NMOS under different substrate current biases.

It2 of the gate-driven NMOS is first increased when the gate bias is increased from 0V. But, the It2 is dropped suddenly, when the gate bias is greater than some critical value. In Fig.6, the NMOS with a W/L of 300/0.3 under 0.8-V gate bias has an It2 even smaller than that under 0-V gate bias. This implies that the gate-driven design [2-4] is no longer suitable for using to improve ESD robustness in such very deep submicrom CMOS technologies. In Fig.7, the It2 of substrate-triggered NMOS can be continually increased when the substrate current is increased without sudden degradation.

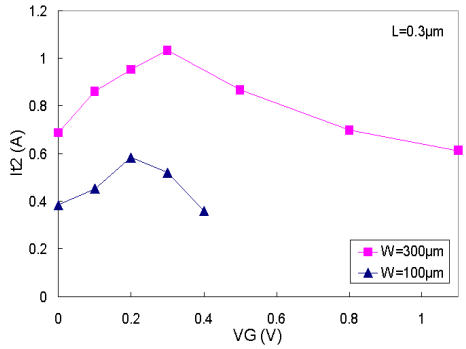


Fig. 6. The dependence of It2 on the gate bias of the traditional finger-type NMOS.

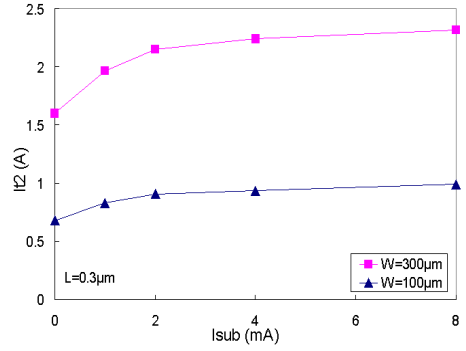


Fig. 7. The dependence of It2 on the substrate current bias of the substrate-triggered NMOS.

2.3 Explications on Triggering Mechanism

The energy-band diagrams with different gate-driven voltage are illustrated in Fig.8. The cross-sectional view of NMOS device is shown in Fig.8 (a). Energy-bands of some positions (A-A', B-B', and C-C' as shown in Fig.8 (a)) in NMOS are analyzed with different gate-biases (V_{GS}=0, V_{GS}>0, and V_{GS}>>0 with the same V_{DS} bias) as shown in Fig.8 (b), (c), and (d). In the V_{GS}=0 case, the ESD current is discharged by the lateral-BJT. When the V_{GS} is increased, energy bands of the interface between gate-oxide and substrate will be lowered by gate bias (V_{GS}) as shown in Fig.8 (b). If the gate-bias is increased larger enough, channel current will be formed as shown in the region G of Fig.8 (c) and (d). Then, the ESD current from drain of MOSFET has two paths to discharge. If the gate bias is continually increased, the discharge region G and S will be extended and combined together as shown in Fig.8 (d). But this

is depended on the doping profile of impurities in the substrate under the gate-oxide in this NMOS. Then ESD protection devices can sustain higher ESD robustness by gate-driven.

But the electric field ($\mathcal{E}_{ox}$) in gate-oxide will be increased by the accumulation charges and gate bias (V_{GS}) as shown in Fig.8 (d). The high electric field may destroy the gate-oxide and damage the interface of NMOS's channel. And, the doping profile of impurities under gate-oxide is an important issue to affect the quantities of channel current and lateral-BJT current. This can also determinate that the ESD protection devices are suitable for the gate-coupled circuits. In gate-driven circuits, coupled-voltage on the gate of ESD protection device must be optimized to avoid damage the gate-oxide and the interface between gate-oxide and substrate.

To explain the effect of substrate-triggered design, the energy-band diagrams with different substrate-triggered biases under the same drain bias are shown in Fig.9. Different from the gate-driven devices, the energy-band diagrams of substrate-triggered devices can hardly be lowered as shown in Fig.9 (c) and (d), because the gate bias of MOSFET is held on ground. In Fig.9 (b), there is no bias on substrate. The current flow region S of lateral-BJT as shown in Fig.9 (b) is far small than those of substrate-triggered devices as shown in Fig.9 (c) and (d), because the substrate bias will lower the energy bands in substrate and extend the current flow region S. Device has the more current flow region; the power dispersion has the more space to sustain the heat dispersion. So, substrate-triggered devices can sustain higher ESD robustness. By the explication, substrate bias will not damage gate-oxide and channel interface of MOSFET, and the doping profile of impurities under gate-oxide can't clearly affect the effect of substrate-triggered design. Therefore, the device triggered by substrate bias will have a much higher ESD level.

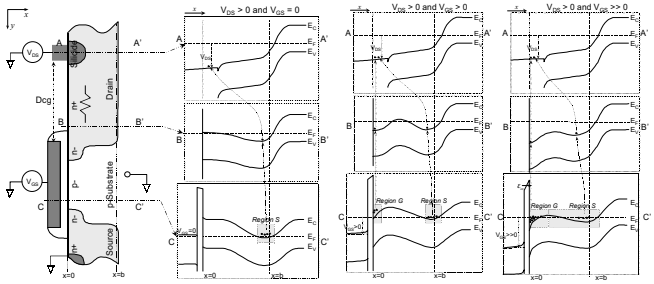


Fig. 8. Illustrate the energy band variations of NMOS device under different gate-driven operations.

3. ON-CHIP ESD PROTECTION CIRCUITS

3.1 Substrate-triggered Input ESD Protection Circuit

Based on above investigation, the on-chip ESD protection circuits can be designed with the substrate-triggered effect to improve ESD robustness. The input ESD protection circuit with the substrate-triggered design is shown in Fig.10. When a positive-to-VSS ESD zapping on the pad, the RC circuit keeps the gate voltage of Mp2 in Fig.10 around 0V. Therefore, Mp2 is simultaneously turned on to conduct a trigger current into the substrate of NMOS Mn1 to initiate the substrate-triggered effect. When the IC is operating in normal condition with power biases, the gate of Mp2 is biased at VDD. Therefore, Mp2 is kept off, and the substrate of NMOS is biased at VSS.

3.2 Substrate-triggered Output ESD Protection Circuit

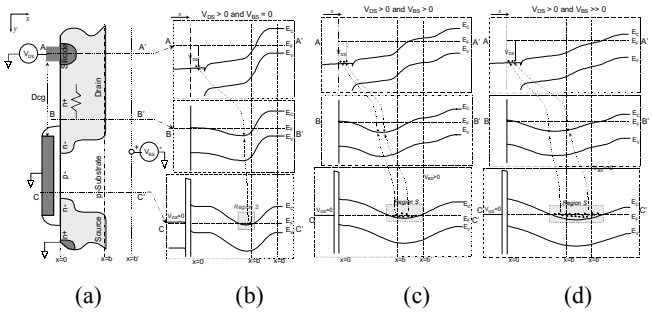


Fig. 9. Illustrate the energy band variations of NMOS device under different substrate triggered operations.

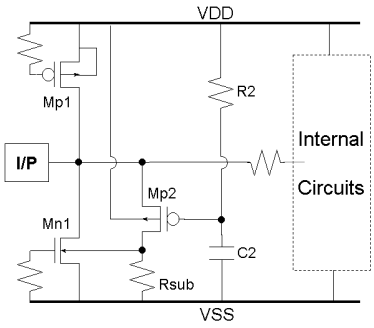


Fig. 10. Input ESD protection circuit with the proposed substrate-triggered technique.

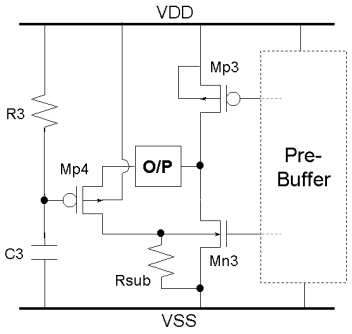


Fig. 11. Output ESD protection circuit with the proposed substrate-triggered technique.

The output ESD protection circuit with the substrate-triggered design is shown in Fig.11. When a positive-to-VSS ESD zapping on the pad, the RC circuit keeps the gate voltage of Mp4 in Fig.11 around 0V. Therefore, Mp4 is simultaneously turned on to conduct a trigger current into the substrate of NMOS Mn3 to initiate the substrate-triggered effect. When the IC is operating in normal condition with power biases, the gate of Mp4 is biased at VDD. Therefore, Mp4 is kept off, and the substrate of NMOS is biased at VSS.

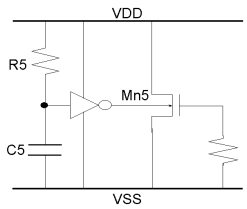
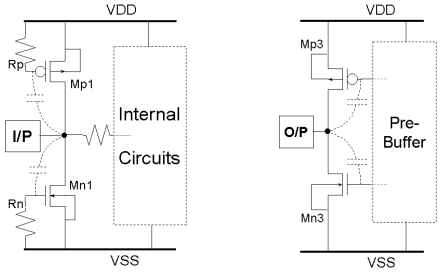


Fig. 12. Power-rail ESD clamp circuit with the proposed substrate-triggered technique.



(a) (b)

Fig. 13. (a) Input and (b) output ESD protection circuits with the traditional gate-driven NMOS.

3.3 Substrate-triggered Power-Rail ESD Clamp Circuit

The power-rail ESD clamp circuit with such substrate-triggered design is shown in Fig.12. An RC-inverter circuit is used to trigger the ESD protection device (Mn5) with substrate-triggered structure. When a positive-to-VSS ESD zapping on VDD, the RC circuit keeps the inverter in Fig.12 turn-on. Therefore, a trigger current flows into the substrate of NMOS Mn5 to initiate the substrate-triggered effect. When the IC is operating in normal condition with power biases, the inverter is kept at off state. Therefore, the substrate of NMOS is biased at VSS.

The input (output) ESD protection circuit with the traditional gate-driven design, shown in Fig.13 (a) (Fig.13 (b)), is also fabricated in the same testchip as a reference.

4. EXPERIMENTAL RESULTS

The positive-to-VSS HBM ESD levels of the fabricated input (output) ESD protection circuits with the substrate-triggered or the gate-driven designs have been tested and compared in Fig.14 (Fig.15). The NMOS with substrate-triggered design has a very obvious improvement on its ESD level, as compared to the traditional gate-driven design. In Fig.14, the substrate-triggered NMOS (W/L= 300μm/0.3μm) can sustain an ESD level of 3.3kV. The NMOS with the same device dimension under gate-driven design has an ESD level of only 0.8kV. This has verified the excellent effectiveness of the proposed substrate-triggered technique to improve ESD robustness in a 0.18-μm salicide CMOS technology.

5. CONCLUSION

From the principle of triggering mechanism and experimental results, the substrate-triggered technique can improve the ESD robustness of ESD protection devices and did not induce the ESD level with suddenly degradation under high-triggered voltage stress. This substrate-triggered technique will replace the traditional gate-driven design as the most effective solution to increase ESD robustness of IC products in sub-quarter-micron CMOS technologies.

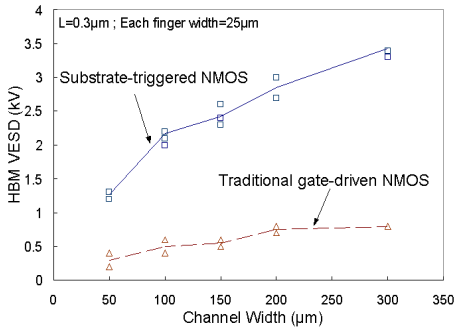


Fig. 14. Comparison on ESD robustness of the input ESD protection circuits with the substrate-triggered NMOS or the traditional gate-driven NMOS.

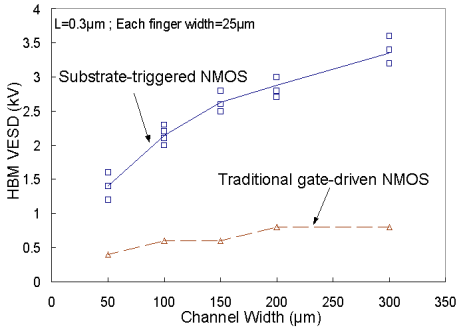


Fig. 15. Comparison on ESD robustness of the output ESD protection circuits with the substrate-triggered NMOS or the traditional gate-driven NMOS.

6. REFERENCES

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