DESIGN ON THE TURN-ON EFFICIENT POWER-RAIL ESD CLAMP CIRCUIT WITH STACKED POLYSILICON DIODES

Ming-Dou Ker and Tung-Yang Chen

Integrated Circuits & Systems Laboratory, Institute of Electronics
National Chiao Tung University, Hsinchu, Taiwan

ABSTRACT

A novel power-rail ESD clamp circuit design by using stacked polysilicon diodes to trigger ESD protection device is proposed to achieve excellent on-chip ESD protection. Design methodology of this novel ESD clamp circuit has been derived in detail. Some controlled factors in the novel ESD clamp circuit can be exactly calculated to design a suitable ESD clamp circuit for different power supply applications. By adding this efficient power-rail ESD clamp circuit, the HBM ESD level of a CMOS IC product has been successfully improved from the original ~200V to become ≥ 3kV.

1. INTRODUCTION

Whole-chip ESD protection has become an important reliability issue of CMOS IC's. Even if there are suitable ESD protection circuits around the input and output pads, the internal circuits are still vulnerable to the ESD damages [1]-[3]. The pin-to-pin ESD stress, as shown in Fig.1, often causes some unexpected ESD damage located in the internal circuits, rather than the input or output ESD protection circuits. In Fig. 1, a positive ESD voltage is applied to some input pin with some output pin relatively grounded, while the *VDD* and *VSS* pins are floating. The ESD current will be diverted from the input pad to the floating *VDD* power line through the forward-biased diode in the input ESD protection circuit. The ESD current flowing in the *VDD* power line can be conducted into the internal circuits through the connection of *VDD* line. Then, the ESD current is discharged through the internal circuits and may cause random ESD damage in the internal circuits, as the **Path_1** current path shown in Fig.1. If there is an effective ESD clamp circuit across the *VDD* and *VSS* power lines, the ESD current can be discharged through the **Path_2** current path in Fig.1. Therefore, the internal circuits can be safely protected against ESD damages. Thus, an effective ESD clamp circuit between the power rails is necessary for protecting the internal circuits against ESD damage [4], [5]. If the IC has no ESD clamp circuit between the *VDD* and *VSS* power rails, the ESD current is discharged through the Path_1, which often causes ESD damage located at the internal circuits. To overcome this unexpected ESD damage on the internal circuits beyond the input or output ESD protection circuits, some ESD clamp circuits had been proposed to be added between the *VDD* and the *VSS* power rails [6]-[10].

In [6], the gate-coupled design had been used to turn on an NMOS to bypass the ESD current from *VDD* to *VSS*. The schematic circuit diagram of such design is illustrated in Fig. 2(a). When a positive ESD is charged to *VDD*, the gate of NMOS (*Mn*) will be coupled with a positive voltage. Then, the NMOS is turned on to discharge ESD current from *VDD* to *VSS*. But the coupled efficiency of this design may be degraded by the parasitic power line capacitance (C_{VDD}).

In another method [7]-[10], a RC-based circuit had been used to turn on an NMOS to bypass the ESD current from *VDD* to *VSS*. The schematic circuit diagram of such design is illustrated in Fig. 2(b). When the positive ESD is charged to *VDD*, the gate of the NMOS has a positive bias. The positive gate voltage turns on the NMOS to discharge the ESD current. To design suitable RC-based circuit, the R-C time constant must be designed about 1μ second. To satisfy this specification, *R* is typically realized about 50KΩ by n-well resistance and C is realized about 20pF by poly-gate of NMOS. The large resistance and capacitance often occupy a large silicon area. The triggering efficiency on the NMOS by the RC-based control circuit is also degraded by the parasitic power line capacitance (C_{VDD}).

In this paper, a novel control circuit with stacked polysilicon diodes is proposed to achieve excellent on-chip ESD protection design.

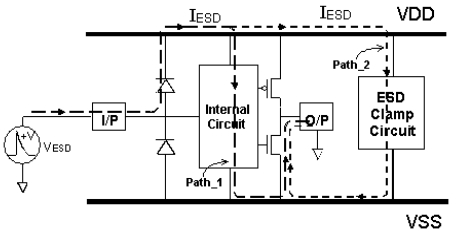
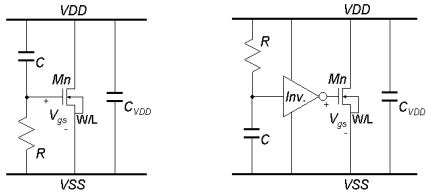


Fig. 1. The ESD current discharging paths in a IC during the pin-to-pin ESD stress condition.



(a) (b)

Fig. 2. Traditional VDD-to-VSS ESD clamp circuits with (a) gate-coupled, and (b) RC-based, control circuit designs.

2. NEW VDD-to-VSS ESD CLAMP CIRCUIT

The proposed ESD clamp circuit is shown in Fig. 3. The stacked polysilicon diodes are operating in forward-biased condition during ESD stress, so the gate-triggering mechanism of NMOS is operated by using DC voltage level detection. Therefore, it is not degraded by the parasitic power line capacitance (C_{VDD}).

If the stacked diodes were realized by the P+ diffusion in n-well, there was a significantly leakage current in the order of mA from *VDD* to *VSS* due to the parasitic vertical BJT effect in CMOS process [4], [11]. But, when the stacked diodes are realized by the

This work was supported by the National Science Council (NSC), Taiwan, R.O.C., under the Grant NSC-89-2215-E-009-103.

0-7803-6685-9/01/$10.00©2001 IEEE

polysilicon layer, the leakage current can be reduced below 1μA under 5-V *VDD* bias. Therefore, the leakage current from *VDD* to *VSS* through the diode-string and the *Mn* device in Fig. 3 can be controlled smaller than 1μA, if the diode number in the stacked diode-string is large enough. The device structure and layout top view of the polysilicon diode realized in a CMOS process are shown in Fig. 4(a) and 4(b), respectively. A polysilicon is doped by using P+, N-, and N+ implantations to realize the polysilicon diode as shown in Fig. 4(a).

To design a suitable ESD clamp circuit, some factors, such as *n*, *R*, diode dimensions, NMOS dimensions, and leakage current, must be well calculated. In next section, the analysis of this circuit and design methodology will be discussed in detail.

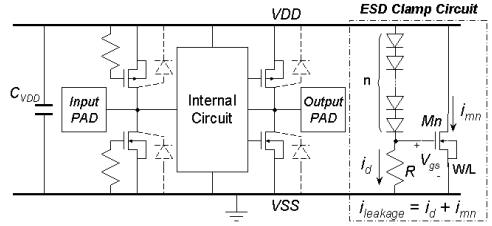
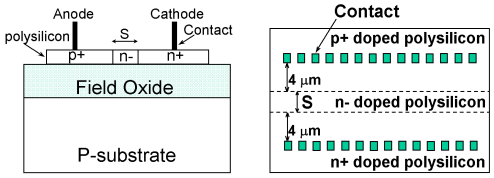


Fig. 3. The proposed VDD-to-VSS ESD clamp circuit with stacked polysilicon diodes to trigger NMOS device.



(a) (b)

Fig. 4. (a) The device structure, and (b) the layout top view, of the P+/N-/N+ polysilicon diode realized in a CMOS process.

3. DESIGN METHODOLOGY

3.1 Analysis of Leakage Current

In Fig. 5(a), a diode-string with *n* diodes is used to trigger the gate of NMOS. The model of each forward-bias diode is shown in Fig. 5(b), where a series resistor is connected with an ideal diode. The current of each ideal diode is:

$$i_d = I_S\left(e^{v_d/\eta v_T} - 1\right). \tag{1}$$

The voltage drop on each ideal diode (v_d) is the same to each other's. I_S is the saturation current, v_T is the thermal voltage, and the factor η generally has a value between 1 and 2. The total voltage drop across the stacked diodes and resistor *R* can be expressed as:

$$V_{drop} = i_d \cdot R + n \cdot \left(i_d \cdot r_d + v_d\right) = i_d\left(R + n \cdot r_d\right) + n\eta v_T \ln\left(1 + \frac{i_d}{I_S}\right) \quad , \tag{2}$$

where *n* is the stacked number of diodes and *R* is the series resistance, which is connected between the gate of NMOS and *VSS*. This equation can be re-written to find the *n* as function of the gate voltage (v_{gs}) of NMOS:

$$n = \frac{V_{drop} - v_{gs}}{\eta v_T \ln\left(1 + \frac{v_{gs}}{R \cdot I_S}\right) + \frac{r_d}{R} \cdot v_{gs}}, \tag{3}$$

where

$$v_{gs} = i_d R. \tag{4}$$

From circuit connection of Fig. 3, the V_{drop} equals to *VDD*. So, we need to adjust the number (*n*) of stacked diodes to reduce the leakage current through the stacked diodes, when IC is operating in normal condition.

To limit the leakage current through NMOS, the gate voltage of NMOS has to be less than the threshold voltage under normal IC operating condition. The NMOS is operated in the subthreshold region ($v_{gs}<v_{th}$). The model of NMOS can be drawn in Fig. 5(c). The subthreshold current of NMOS is [12]

$$i_{mn} = \frac{1}{2}\mu_n C_{OX} a v_T^{\,2} \frac{W_{eff}}{L_{eff}}\left(\frac{n_i}{N_A}\right)^2\left(1 - e^{-\frac{VDD - i_{mn}\cdot(r_D + r_S)}{v_T}}\right) e^{\frac{\psi_s}{v_T}}\left(\frac{\psi_s}{v_T}\right)^{-1/2} \quad . \tag{5}$$

Therefore, the total leakage current of this proposed power-rail ESD clamp circuit can be expressed as:

$$i_{leakage} = i_d + i_{mn}, \tag{6}$$

where the leakage current through stacked diodes (i_d) can be got from (4), and the leakage current through the NMOS (i_{mn}) can be got from (5). Finally, the total leakage current ($i_{leakage}$) can be further expressed as function of v_{gs}:

$$i_{leakage} = \frac{v_{gs}}{R} + K \cdot \sqrt{\frac{v_T}{\psi_s(v_{gs})}} \cdot e^{\frac{\psi_s(v_{gs})}{v_T}} \quad , \tag{7}$$

where

$$\psi_s(v_{gs}) = \left(v_{gs} - V_{FB}\right) - \frac{1}{2}\xi\left\{\sqrt{1 + \frac{4}{\xi}\left(v_{gs} - V_{FB} - v_T\right)} - 1\right\} \quad . \tag{8}$$

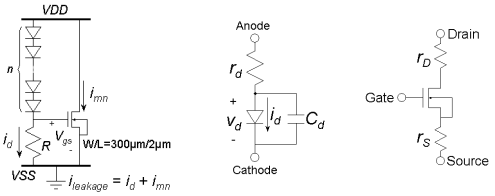
In these equations, the parameters of *K* and ξ are constant factors for a CMOS process, and they are defined as:

$$K \equiv \frac{1}{2}\mu_n C_{OX} a v_T^{\,2} \frac{W_{eff}}{L_{eff}}\left(\frac{n_i}{N_A}\right)^2\left(1 - e^{-\frac{VDD - i_{mn}\cdot(r_D + r_S)}{v_T}}\right) \quad , \tag{9}$$

and

$$\xi \equiv a^2 v_T. \tag{10}$$

For a given CMOS process, the value of *K* and ξ can be determined from process parameters. From (3) and (7), the relation between *n* and $i_{leakage}$ can be calculated.



(a) (b) (c)

Fig. 5. (a) ESD clamp circuit with stacked polysilicon diode in this design and the models of (b) diode and (c) NMOS in this circuit.

3.2 Design Sequence

From (7), there is a complex relation between the factors of *VDD*, *R*, *n*, diode dimensions, and NMOS dimensions. NMOS dimensions are the major factor of ESD robustness for the ESD clamp circuit. A suitable size of NMOS, W/L=300μm/2μm, is considered in this design example. The value of *VDD* is determined by the IC specification. In normal operating condition, the gate voltage of

NMOS must be as small as possible to limit the leakage current through NMOS. So, the value of n and R are the major design factors to limit the leakage current of this ESD clamp circuit. To determine the value of R and n, the relation between v_{gs} and n can be calculated from (3).

First, some suitable series resistances (R) are temporarily chosen to calculate the relation between v_{gs} and n from (3). The condition of choosing R is considered to limit the gate voltage (v_{gs}) of NMOS as small as possible. If NMOS is turned off, the leakage current will appear through the diode-string and resistor R. For example, when v_{gs} is smaller than 0.01V, R=10KΩ will be chosen under the condition of $i_{leakage}$<1μA. If v_{gs} is smaller than 0.1V, R=100KΩ can be chosen. The relation between v_{gs} and n under VDD=5V and R=10KΩ or 100KΩ is plotted in Fig. 6. To verify the calculation results, SPICE simulation results are also drawn together in Fig. 6.

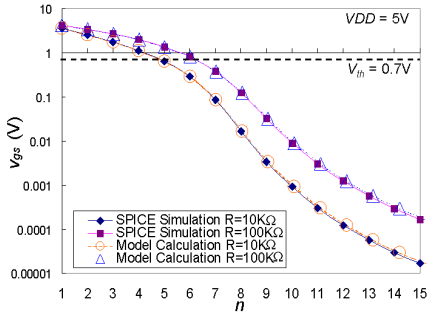


Fig. 6. Model calculation and SPICE simulation results between gate voltage (v_{gs}) of NMOS and stacked number (n) of polysilicon diode.

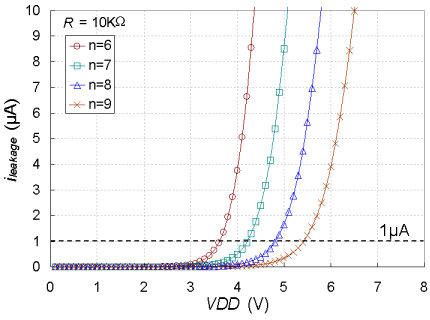


Fig. 7. The relation between leakage current and power supply (VDD) in the proposed power-rail ESD clamp circuit with different number (n) of stacked polysilicon diodes and a fixed R=10KΩ.

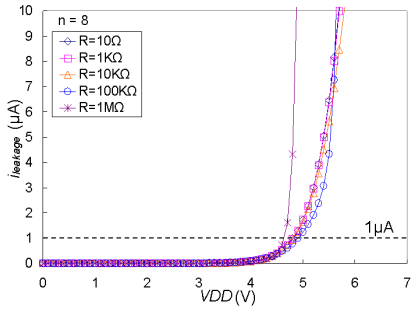


Fig. 8. The relation between leakage current and power supply (VDD) in the proposed power-rail ESD clamp circuit with different series resistance (R) and a fixed n=8.

Second, the relation between gate voltage (v_{gs}) of NMOS and the total leakage current ($i_{leakage}$) must be calculated to determine the exact value of n. From (2) and (4), the relation between v_{gs}, i_d, and R can be calculated. Only some values of R (10K~100K) will be chosen to calculate the values of v_{gs}. Using these values of v_{gs}, the total leakage current ($i_{leakage}$) can be calculated from (7).

The relations between the total leakage current ($i_{leakage}$) and the bias of VDD under different n and R are shown Fig. 7 and Fig. 8. In Fig. 7, the R is fixed at 10KΩ, but the n varies from 6 to 9 to investigate the leakage current. In Fig. 8, the n is fixed at 8, but the R varies from 10Ω to 1MΩ to investigate the leakage current. From these calculations, the n can be chosen as 8 to meet the design specification of $i_{leakage}$<1μA under VDD=5V bias. For different VDD voltage level, the suitable n and R can be calculated from the derived equations in this paper.

4. APPLICATION EXAMPLE

The proposed power-rail ESD clamp circuit has been successfully used to rescue the ESD level of a CMOS IC product, which has an original HBM ESD level of only ~200V by using the traditional gate-coupled NMOS as its power-rail ESD clamp circuit.

The rescued design for the CMOS IC product with 5-V VDD is shown in Fig. 9, where 8-stacked polysilicon diodes are used in the diode-string to control the gate voltage of $Mn3$ with a W/L of 300μm/2μm. When the VDD is charged no more than 5V, the $Mn3$ is kept off. But when the VDD is charged up greater than 5V, the $Mn3$ is turned on to clamp the VDD voltage level.

With the proposed power-rail ESD clamp circuit, the ESD current in VSS(+) ESD stress at the Pad1 is discharged through the forward-biased $Dp1a$ to VDD, and then discharged through the turned-on $Mn3$ to VSS, rather than the breakdown of the diode $Dn1a$. In VDD(-) ESD stress at the Pad1, the negative ESD current is conducted to VSS through the forward-biased $Dn1a$, and then discharged to the grounded VDD through the turned-on $Mn3$, without causing the breakdown on the diode $Dp1a$. The second diode stage with $Dp1b$ and $Dn1b$ is used to further clamp the overstress voltage across the gate oxide of the input circuits for more safe ESD protection. The partial picture of this IC with the realization of the ESD protection circuit on Pad1 pin and the power-rail ESD clamp circuit is shown in Fig. 10.

The I-V curve of the new proposed power-rail ESD clamp circuit with 8-stacked polysilicon diodes is measured in Fig. 11. When the applied voltage across VDD and VSS is increased higher to bias the gate of $Mn3$ greater than its threshold voltage, the NMOS $Mn3$ is turned on to conduct current from VDD to VSS. So, the measured I-V curve in Fig. 11 has a sharp current increase when the applied voltage is greater than 5V.

In order to investigate the turn-on efficiency of the proposed power-rail ESD clamp circuit with the polysilicon diodes, a 0-to-8V voltage pulse (generated from a pulse generator with a pulse width of 4μs and a rise time of ~10ns, as the dashed line shown in Fig. 12) is applied to the Pad1. The clamped voltage waveform on the Pad1 is measured and shown in Fig. 12. Because the diodes of Pad1 have a breakdown voltage around 12V, the applied 8-V voltage does not cause any breakdown on the diodes of Pad1. But, the 0-to-8V voltage pulse is actually clamped to about 6.5V in Fig. 12. This is due to the turn-on of the power-rail ESD clamp circuit across the VDD and VSS power lines. Therefore, the overstress voltage on the Pad1 is discharged from the Pad1 to VDD through the forward-

biased diode *Dp1a*, and then discharged to *VSS* through the turned-on power-rail ESD clamp circuit. This has successfully verified the effectiveness of the new proposed power-rail ESD clamp circuit with the stacked polysilicon diodes.

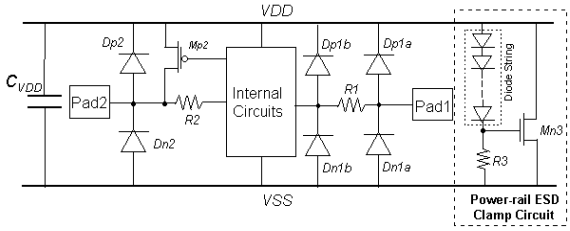


Fig. 9. The application of on-chip ESD protection design with this proposed power-rail ESD clamp circuit.

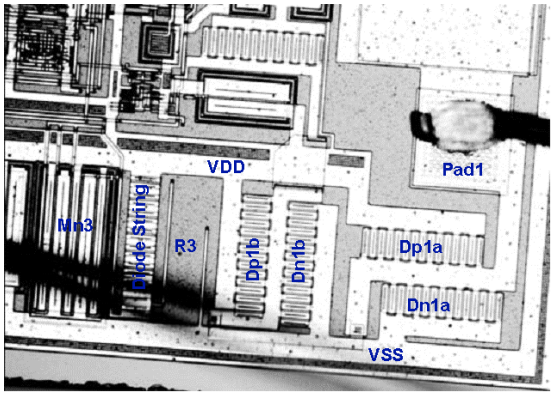


Fig. 10. The partial picture of a CMOS IC with the proposed power-rail ESD clamp circuit.

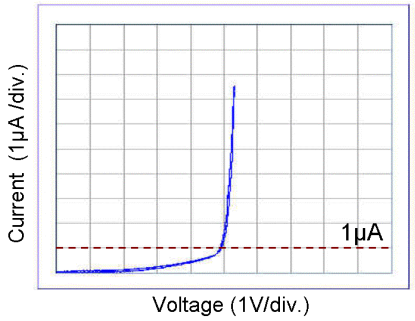


Fig. 11. The measured I-V curve from *VDD* to *VSS* of the new proposed power-rail ESD clamp circuit with 8-stacked polysilicon diodes.

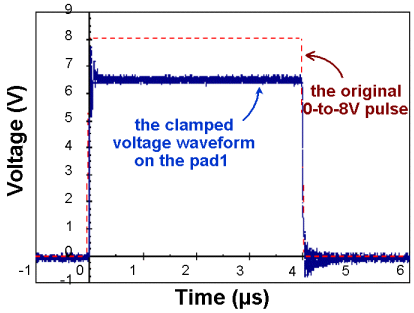


Fig. 12. The measured voltage waveform at the Pad1 when a 0-to-8V voltage pulse is applied to the Pad1 with the *VSS* grounded.

The HBM ESD level of this rescued CMOS IC product in VSS(+) test mode is improved to 3kV. In the VDD(-) ESD test mode, the HBM ESD level is >4kV. The VDD-to-VSS HBM ESD stress of this IC is greater than 4kV.

5. CONCLUSION

The design on a novel power-rail ESD clamp circuit has been explored in detail. The experimental results have verified that the analysis and design model can exactly implement the ESD clamp circuit with a controllable leakage current between the power lines. Using this design method, the HBM ESD level of a CMOS IC product has been successfully improved up to 3kV. By using the stacked polysilicon diodes to control the turn-on of ESD clamp NMOS, this design can be widely and more feasibly used in future SOC (System-On-a-Chip) IC's with multiple or mixed-voltage power supplies.

6. REFERENCES

[1] C. Duvvury, R. Rountree, and O. Adams, "Internal chip ESD phenomena beyond the protection circuit," *IEEE Trans. on Electron Devices*, vol. 35, pp. 2133-2139, 1988.

[2] C. Johnson, T. Maloney, and S. Qawami, "Two unusual HBM ESD failure mechanisms on a mature CMOS process," in *Proc. of EOS/ESD Symp.*, 1993, pp. 225-231.

[3] M.-D. Ker and T.-L. Yu, "ESD protection to overcome internal gate-oxide damage on digital-analog interface of mixed-mode CMOS IC's," *Microelectronics Reliability*, vol. 36, pp. 1727-1730, 1996.

[4] T. Maloney and S. Dabral, "Novel clamp circuits for IC power supply protection," *IEEE Trans. on Components, Packaging, and Manufacturing Technology – Part C*, vol. 19, no. 3, pp. 150-161, 1996.

[5] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. on Electron Devices*, vol. 46, no. 1, pp. 173-183, 1999.

[6] J. Chen, A. Amerasekera, and C. Duvvury, "Design methodology and optimization of gate-driven NMOS ESD protection circuits in submicron CMOS processes," *IEEE Trans. on Electron Devices*, vol. 45, no. 12, pp. 2448-2456, 1998.

[7] M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD protection design on analog pin with very low input capacitance for high-frequency or current-mode applications," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1194-1199, 2000.

[8] R. Merrill and E. Issaq, "ESD design methodology," in *Proc. of EOS/ESD Symp. Proc.*, 1993, pp. 233-237.

[9] S. Dabral, R. Aslett, and T. Maloney, "Core clamps for low voltage technologies," in *Proc. of EOS/ESD Symp. Proc.*, 1994, pp. 141-149.

[10] E. Worley, R. Gupta, B. Jones, R. Kjar, C. Nguyen, and M. Tennyson, "Sub-micron chip ESD protection schemes which avoid avalanching junctions," in *Proc. of EOS/ESD Symp. Proc.*, 1995, pp. 13-20.

[11] M.-D. Ker and W.-Y. Lo, "Design on the low-leakage diode string for using in the power-rail ESD clamp circuits in a 0.35-μm silicide CMOS process," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 4, pp. 601-611, 2000.

[12] S. M. Sze, *Physics of semiconductor devices*, A Wiley-Insterscience Publication, 1981.