Investigation on ESD Robustness of CMOS Devices in a 1.8-V 0.15-μm Partially-Depleted SOI Salicide CMOS Technology

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ABSTRACT

Electrostatic discharge (ESD) robustness of CMOS devices with four different layout structures fabricated in a 0.15-μm partially-depleted silicon-on-insulator (SOI) salicide CMOS process are verified by ESD tester. The second breakdown current (It2) of fabricated CMOS devices is also measured by the transmission line pulse generator (TLPG). The dependences of ESD robustness on the layout parameters of CMOS devices in this SOI CMOS process have been investigated to find the optimum layout rules for on-chip ESD protection design. The effectiveness of ESD clamp circuits designed with the gate-driven and substrate-triggered techniques are also compared in this SOI CMOS process.

INTRODUCTION

SOI (Silicon-on-Insulator) is expected as a promising technology for advanced ULSI in terms of high speed and low power dissipation. But, ESD reliability in sub-quarter-micron SOI CMOS technology becomes a challenge due to the low thermal conductivity of the buried oxide underneath the top layer silicon film and the STI (Shallow-Trench-Isolation) structure on the insulating layer [1]. When the circuit design transiting from bulk to SOI CMOS process, some new ESD protection designs with the Lubistor diode or B/G-coupled MOS in the thin film SOI technology had been reported [2]. However, an output buffer in the SOI CMOS process is still often formed by a pull-up PMOS and a pull-down NMOS, which are directly connected to the bond pad. The ESD overstress voltage zapping to the output pin of a CMOS IC is conducted to the output PMOS and NMOS. Therefore, the output PMOS and NMOS still need to be designed and carefully drawn in layout to sustain a reasonable ESD stress. ESD level of commercial IC products is generally requested to be higher than 2kV in HBM ESD stress [3]. Thus, the device characteristics in a new SOI CMOS process still need to be investigated in details for defining one set of design rules for on-chip ESD protection design.

Table I

Gate OxideThickness (thin, for 1.8V)	26 Å
NMOS/PMOS Threshold Voltage (Vtn/Vtp)	0.45V/0.5V
Buried Oxide (BOX) Thickness	1000 Å
Silicon Thickness on BOX	1500 Å
n+, p+ Doping Concentration	10^{21}~10^{22} cm^{-3}
N-well, P-well Doping Concentration	5E17 cm^{-3}

In this work, both NMOS and PMOS with four different device structures and different layout parameters have been fabricated in a 0.15-μm partially-depleted SOI salicide CMOS process to verified their ESD robustness. The effectiveness of ESD clamp circuit designed with the gate-driven or the substrate-triggered techniques in this 0.15-μm partially-depleted SOI salicide CMOS process is also investigated.

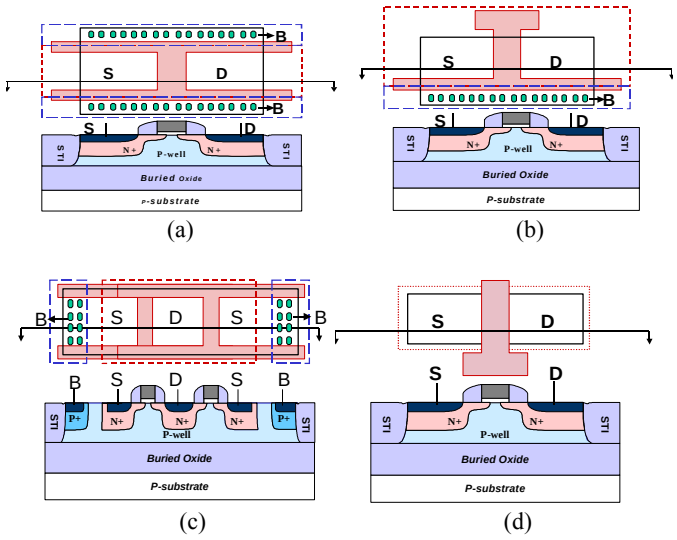

Fig.1 The layout top view and device cross-sectional view for (a) H-gate, (b) T-gate, (c) sided-body, and (d) floating-body MOSFETs used for ESD investigation in a 0.15-μm partially-depleted SOI salicide CMOS process.

DEVICE STRUCTURES UNDER TEST

The device structures used to realize the NMOS or PMOS in the partially-depleted SOI salicide CMOS process are shown in Figs. 1(a) ~ 1(d). The process features of this partially-depleted SOI salicide CMOS process are listed in Table I, where the gate-oxide thickness is only 26Å and the silicon body on buried oxide layer is only 1500Å In Fig.1(a), the device structure is called as H-gate NMOS. The H-gate MOSFET has the body contacts presented at both top and bottom ends of the channel. In Fig. 1(b), the device structure is called as T-gate MOSFET. The T-gate MOSFET has the body contacts presented only at the bottom end of the channel. In Fig. 1(c), the device structure is called as a sided-body MOSFET. The sided-body MOSFET has the body contacts presented at both left and right sides of the channel. In Fig. 1(d), the device structure is called as a floating-body MOSFET, which has no connection to the body of MOSFET.

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These devices are drawn with different layout parameters, which include the channel width (W), channel length (L), each finger length (Wf), silicide-blocking spacing at drain side (Cd), silicide-blocking spacing at source side (Cs), and silicide-blocking spacing from drain side to the top/bottom poly gate (Sd). The typical layout example of a H-gate NMOS with multiple fingers to realize a large channel width is shown in Fig.2, where the layout parameters are clearly defined and marked on the layout top view. The four different device structures are used to draw both the NMOS and PMOS devices with different layout parameters and fabricated in the partially-depleted SOI salicide CMOS process. There are total 11 testchips drawn for this investigation. Each testchip has 40 bond pads and assembled in a DIP 40-pin package for ESD verification.

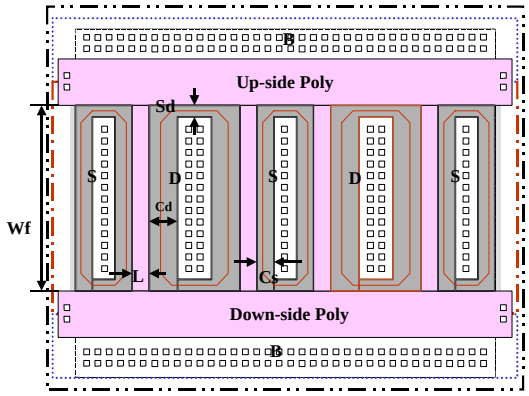
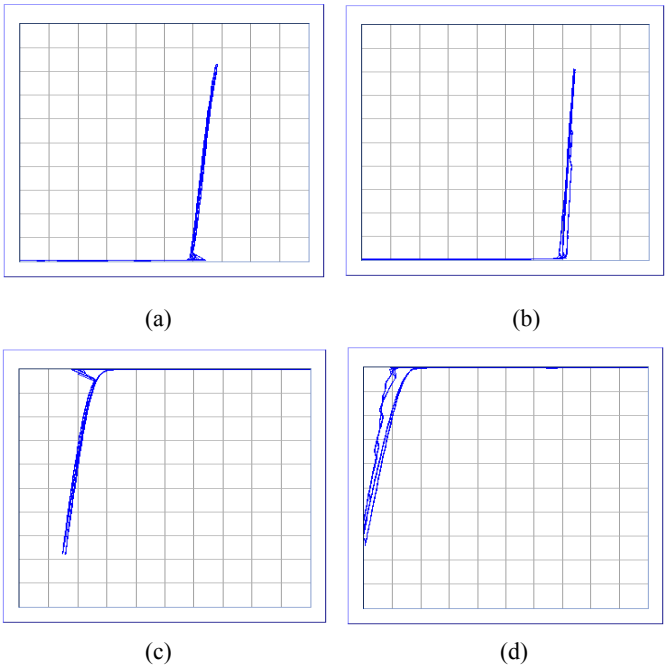


Fig.2 The layout example of an H-gate NMOS with multiple fingers to realize a large channel width. The layout parameters used to investigate the effect on ESD robustness are also indicated in this figure.



(a) (b)

(c) (d)

Fig.3 The measured breakdown I-V curves of (a) H-gate NMOS with L=0.25μm, (b) H-gate NMOS with L=0. 5μm, (c) T-gate PMOS with L=0.25μm, and (d) T-gate PMOS with L=0.5μm. (X-axis : 0.5V/div.; Y-axis: 2mA/div.)

EXPERIMENTAL RESULTS

A. DC Breakdown Characteristics

To investigate the dc breakdown characteristics of the fabricated SOI MOSFETs, the curve tracer Tek370 is used to measure the I-V curves of NMOS and PMOS. A positive (negative) voltage is applied to the drain of NMOS (PMOS) with its source and gate connected to ground to measure its breakdown I-V curves. The breakdown I-V curves of the fabricated H-gate NMOS with channel length of 0.25μm and 0.5μm are shown in Figs.3(a) and 3(b), respectively. The breakdown I-V curves of the fabricated T-gate PMOS with channel length of 0.25μm and 0.5μm are shown in Figs.3(c) and 3(d), respectively. The dependences of H-gate NMOS / T-gate PMOS drain breakdown voltage on its channel length are shown in Fig.4. A SOI MOSFET with a shorter channel length has a lower breakdown voltage.

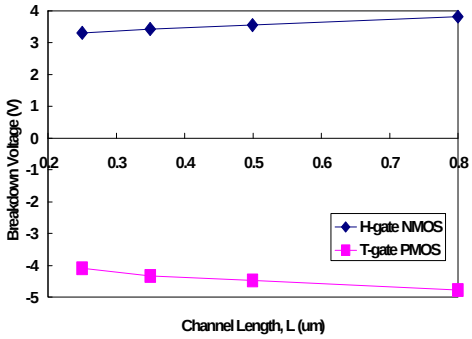
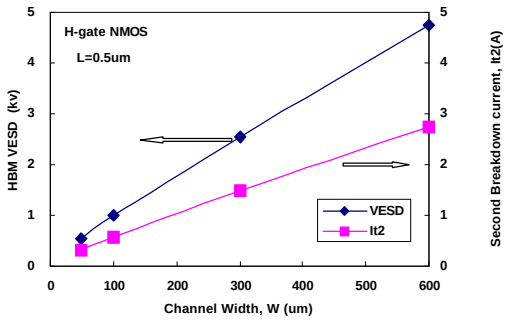
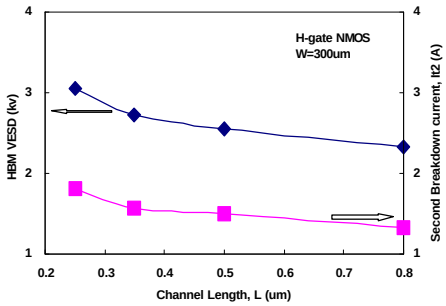


Fig.4. The dependences of drain breakdown voltage on the channel length of H-gate NMOS and T-gate PMOS devices.



(a)



(b)

Fig. 5. Dependence of HBM ESD level on (a) the channel width (L is fixed at 0.5μm), and (b) the channel length (W is fixed at 300μm), of H-gate NMOS.

B. ESD Robustness

The fabricated NMOS and PMOS devices with different device structures and layout parameters are tested by *KeyTek* ESD simulator in the human-body-model (HBM) ESD stress [3]. The ESD robustness of H-gate NMOS with different channel width and channel length is shown in Figs. 5(a) and 5(b). The ESD level is defined as the ESD voltage that the device can sustain without causing damage. The failure criterion is defined as that the off-state leakage current is greater than 1μA under 2-V voltage biased. The It2 of H-gate NMOS measured by 100-ns TLPG is also shown in Fig.5 for reference. The correlation between the ESD level and It2 value of the H-gate NMOS is plotted in Fig.6, where the slope is almost the same as 1.5kohm. This has also confirmed the accuracy of ESD robustness measurement on the fabricated SOI MOSFET. In Fig5(b), the NMOS with a shorter channel length has a higher ESD level. This is quick different to the previous results measured in the bulk CMOS process [4].

An NMOS with a larger channel width is often drawn with multiple fingers in layout. The finger length (Wf) may affect the ESD level of a MOSFET. In Fig.7, it shows the variation on the ESD level of the H-gate and floating-body NMOS's, which are drawn with a fixed W/L=300μm/0.5μm but with different finger length (Wf). From Fig. 7, the NMOS has a higher ESD level when its finger length is chosen around 50~75 μm.

The ESD levels of NMOS devices under four different device structures are measured and compared in Figs.8(a) and 8(b). The ESD levels of PMOS devices under four different device structures are measured and compared in Figs.9(a) and 9(b).In Figs.8(a) and 9(a), the channel length is fixed at 0.5μm, and the ESD levels of the four different NMOS / PMOS devices are almost linearly increased when its channel width increases. In Figs.8(b) and 9(b), the channel width is fixed at 300μm, but the ESD levels of the four different NMOS / PMOS devices are degraded when its channel length is increased. Both the NMOS and PMOS with T-gate structure have a little higher ESD level than the others. Still now, there is no any abnormal in ESD robustness of the floating-body NMOS and PMOS, which have the floating body effect.

C. Gate-Driven and Substrate-Triggered Design

The well-designed power-rail ESD clamp circuit can very efficiently improve the ESD level of I/O pins of a CMOS IC [5]. To verify the ESD performance of SOI NMOS for power-rail ESD protection, three different power-rail ESD clamp circuits are also designed and fabricated in this 0.15-μm partially-depleted SOI salicide CMOS process. The tested power-rail ESD clamp circuits are shown in Fig.10, which include the gate-driven, substrate-triggered, and gate-grounded designs. The NMOS devices in these three different power-rail ESD clamp circuits are all the H-gate device structures. The ESD levels of these three different power-rail ESD clamp circuits are measured and compared in Fig.11, under the variation on the channel width of NMOS devices. In Fig.11, the H-gate NMOS with gate-driven design has a obvious increase on its ESD level, as comparing to the other two designs. The substrate-triggered design did not obviously improve ESD level of the H-gate NMOS, as comparing to the gate-grounded design. This is also a difference to the previous results in the bulk CMOS process [4].

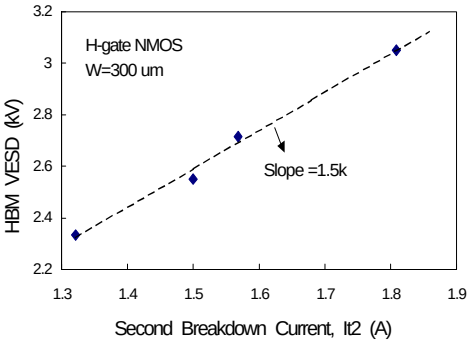


Fig.6 The correlation between the ESD level and It2 value of the H-gate NMOS with different channel length.

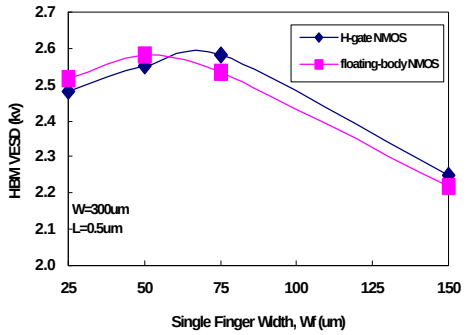
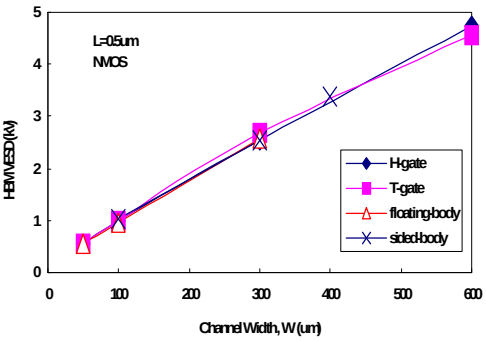
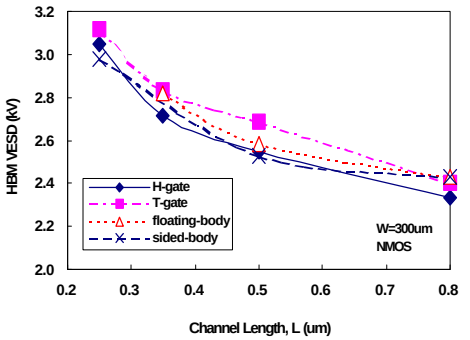


Fig.7 The variation on ESD level of the H-gate and floating-body NMOS' s, which are drawn with a fixed W/L=300μm/0.5μm but with different finger length.

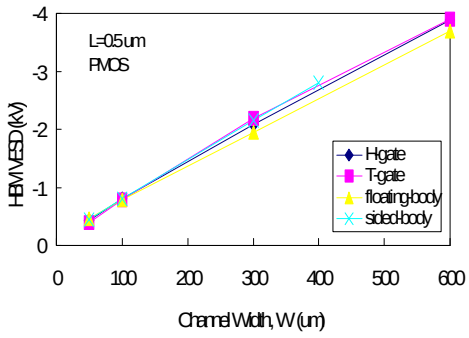


(a)

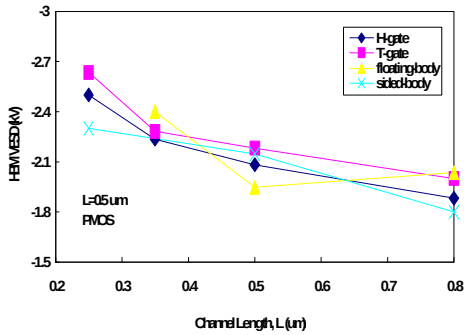


(b)

Fig.8 Dependence and comparison of ESD levels of NMOS devices among the four different device structures on the (a) channel width (L=0.5μm), and (b) channel length (W=300μm).

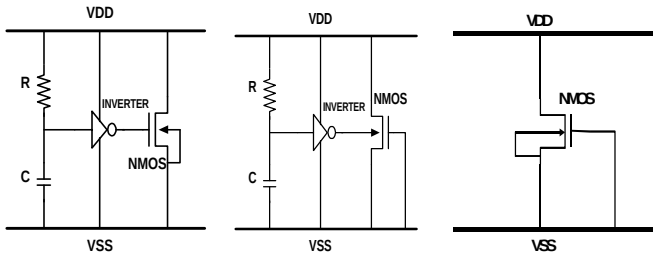


(a)



(b)

Fig.9 Dependence and comparison of ESD levels of PMOS devices among the four different device structures on the (a) channel width (L=0.5μm), and (b) channel length (W=300μm).



(a) (b) (c)

Fig.10 Power-rail ESD clamp circuits designed with (a) the gate-driven technique, (b) the substrate-triggered technique, and (c) only gate-grounded design.

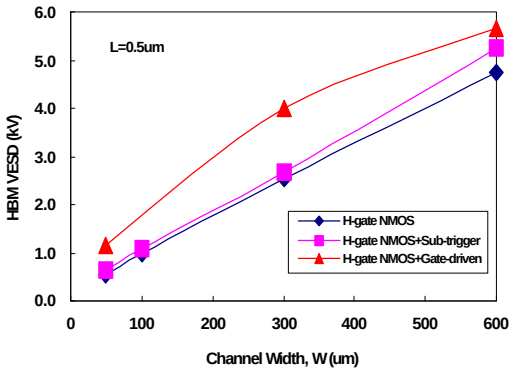
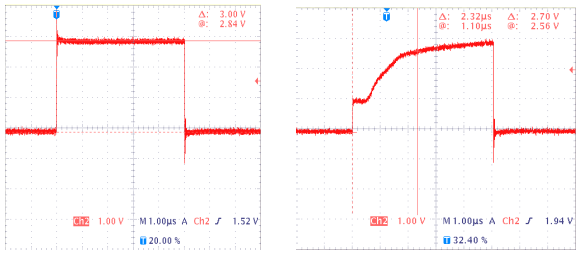


Fig.11 Comparison on the ESD levels among the three different power-rail ESD clamp circuits, shown in Fig.10, under the variation of different channel width.

D. Turn-on Verification

The power-rail ESD clamp circuit can be efficient, only if it can be turned on much faster than the device breakdown in the core circuits of a CMOS IC. To verify the turn-on efficiency of the power-rail ESD clamp circuits, a 0-to-3V voltage pulse is applied to the VDD node and the VSS node is relatively grounded. The H-gate NMOS with a channel length of 0.5μm has a drain breakdown voltage higher than 3V. Such a 0-to-3V voltage pulse applied to the ESD clamp circuit with the gate-grounded design has a voltage waveform shown in Fig.12(a), where the voltage waveform did not degrade. But, when such a 0-to-3V voltage pulse applied to the ESD clamp circuit with gate-driven design, the voltage waveform is degraded and shown in Fig.12(b). This is due to the turn-on of the ESD clamp NMOS across the VDD and VSS power rails to clamp the pulse voltage. The degraded voltage waveform shown in Fig.12(b) has verified the effectiveness of the power-rail ESD clamp circuit with gate-driven design in this SOI CMOS process.



(a) (b)

Fig.12 The degraded voltage waveforms of the applied 0-to-3V voltage pulse to the VDD node of the power-rail ESD clamp circuits with (a) the gate-grounded design, and (b) the gate-driven design, where the VSS is grounded and the ESD clamp NMOS has channel width of 600μm.

CONCLUSION

ESD robustness of the NMOS and PMOS devices with four different device structures and layout parameters in a 0.15-μm partially-depleted SOI salicide CMOS process has been investigated. The ESD level of NMOS/PMOS with a channel width of 300μm can still sustain HBM ESD stress of 2kV. To further improve ESD level, the power-rail ESD clamp circuit designed with the gate-driven technique is recommended to place into the SOI CMOS IC. With gate-driven design, the ESD level of NMOS with a channel width of 300μm can be improved to become 4kV.

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