ESD Protection Strategy for Sub-Quarter-Micron CMOS Technology : Gate-driven Design Versus Substrate-triggered Design

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ABSTRACT

The operation principles of gate-driven design and substrate-triggered design for ESD (ElectroStatic Discharge) protection are first explained by energy-band diagrams in this paper. The on-chip ESD protection devices realized in 0.18-μm and 0.35-μm CMOS processes are used to verify the efficiency of gate-driven or substrate-triggered designs. The substrate-triggered design can effectively and continually improve ESD robustness of protection devices than the gate-driven design. The HBM (Human-Body-Model) ESD level of NMOS with a W/L of 300μm/0.3μm can be improved from the original 0.8kV to become 3.3kV by the substrate-triggered design. But, the gate-driven design cannot continually improve the ESD level of the same device in the sub-quarter-micron CMOS process.

INTRODUCTION

ESD level of commercial IC products is generally requested to be higher than 2kV in the HBM [1] ESD stress. Therefore, on-chip ESD protection circuits had been built on the chip to protect the devices and circuits against ESD damages. To sustain the requested ESD level without causing damage in IC, on-chip ESD protection circuits are often drawn with larger device dimensions. Such ESD protection devices in ESD protection circuits are often realized by finger-type layout to save total layout area [2]. But, during the ESD stress, the multiple fingers of ESD protection NMOS cannot be uniformly turned on. Only several fingers of the NMOS were turned on and therefore damaged by ESD [3]. The EMMI photography of turned-on NMOS (W/L=300μm/0.5μm) with 40mA drain pulse current is shown in Fig. 1. Only some regions of the center fingers in this NMOS are turned on. Due to the short-channel NMOS has the snapback effect on its I-V curve, as shown in Fig. 2. The turned-on center fingers of Fig. 1 will cause the ESD current crowding on those fingers. If the turned-on region cannot be extended to full regions of all fingers before second breakdown occurs in NMOS, the ESD current will be mainly discharged through this turned-on region. This often causes a low ESD level, even if the NMOS has a large device dimension.

To improve the turn-on uniformity among the multiple fingers, the gate-driven design [3]-[5] and substrate-triggered design [6]-[8] had been reported to increase ESD level of the large-device-dimension NMOS. The design diagrams are summarized in Fig. 3(a) and 3(b), respectively. In Fig. 3(a), an ESD detection circuit is connected between the pad and the gate of NMOS. In Fig. 3(b), the ESD detection circuit is also connected between the pad and the bulk of NMOS. In normal operation condition, the V_G in Fig. 3(a) must be kept at zero to turn off the channel of NMOS. The V_B in Fig. 3(b) must be kept at ground to turn off the parasitic lateral BJT of NMOS. There are two current flow paths in protection devices during ESD stress. One is the channel current

of MOSFET, the other is the turn-on current of parasitic lateral BJT. The gate-driven design often enhances the channel current during ESD stress, but there is almost no channel current in substrate-triggered design. The substrate-triggered design only improves the turn-on current of parasitic lateral BJT. Some discussion will be explained in the next section.

Recently, ESD level of the gate-driven NMOS had been found to be decreased dramatically when the gate voltage is somewhat increased [5], [6], [9]. The gate-driven design causes ESD current flowing through the surface channel of NMOS, therefore NMOS becomes more sensitive to be burned out by ESD energy. With gate-driven design, the larger ESD current flowing on the surface channel can easily damage the interface between gate-oxide and substrate. However, the parasitic lateral BJT of MOSFET can sustain higher ESD current than the channel surface of MOSFET. If the lateral BJT can be controlled as the dominant ESD current path, the substrate-triggered design can sustain higher ESD current. In this paper, the operation principles of the gate-driven and substrate-triggered designs for ESD protection are clearly explicated by using energy-band diagrams.
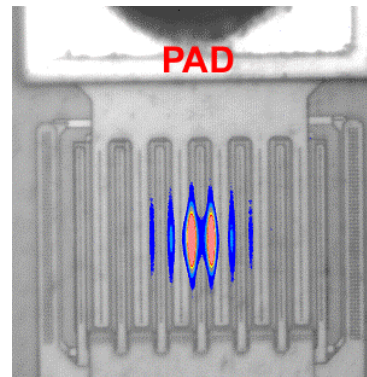

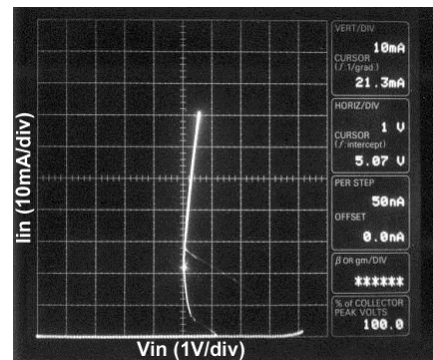Fig. 1. The EMMI photography of turned-on NMOS (W/L = 300μm/0.5μm) with 40mA drain pulse current.

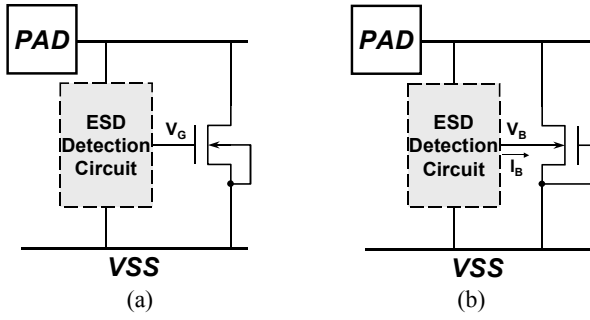Fig. 2. The snapback I-V curve of NMOS device with W/L of 300μm/0.5μm.

Fig. 3. The ESD protection circuit realized by the (a) gate-driven design, and (b) substrate-triggered design.

OPERATION PRINCIPLES

Gate-Driven Effect

To improve ESD robustness of the ESD-protection NMOS devices, the gate-driven design had been reported to more uniformly trigger on the multiple fingers of the large-dimension ESD-protection NMOS. But, the coupled voltage on the gate of NMOS can turn on the channel of the NMOS, therefore the ESD current is discharging through the channel region of the ESD-protection NMOS. Due to the shallower junction depths and the LDD structure at the drain/source regions, the turned-on NMOS is weak to sustain ESD stress. To understand the physic effect on current distribution, the energy-band diagram is a well method to explain the potential distribution along MOSFET. The current distribution can be determined from the energy-band diagram. To disperse the energy heat and lower the temperature in MOSFET during ESD stress, the larger current distribution area with lower current density can sustain higher ESD level.

The energy-band diagrams with different gate-driven voltage are illustrated in Fig. 4. The cross-sectional view of NMOS device is shown in Fig. 4(a). Energy-bands of some positions (A-A', B-B', and C-C' as shown in Fig. 4(a)) in NMOS are analyzed with different gate-biases ($V_{GS}=0$, $V_{GS}>0$, and $V_{GS}>>0$ with the same V_{DS} bias), which are shown in Fig. 4(b), 4(c), and 4(d). In the $V_{GS}=0$ case, the ESD current is discharged by the lateral-BJT. When the V_{GS} is increased, energy bands of the channel surface can be lowered by gate bias (V_{GS}) as shown in Fig. 4(b). If the gate-bias is increased larger enough, channel current will be formed by accumulation charges as shown in the region G of Fig. 4(c) and 4(d). Then, the ESD current from drain of MOSFET has two paths to discharge. If the gate bias is continually increased, the discharge region G and S will be extended and combined together as shown in Fig. 4(d). Then ESD protection devices can sustain higher ESD robustness by gate-driven. But the operation mechanism has to depend on the substrate doping profile of impurities under the gate-oxide in NMOS.

But, the electric field ($\mathcal{E}_{ox}$) in gate-oxide is increased by the accumulation charges and gate bias (V_{GS}) as shown in Fig. 4(d). The high electric field may destroy the gate-oxide and damage the channel surface of MOSFET. On the other hand, the doping profile of impurities under gate-oxide is an important issue to affect the quantities of channel current and lateral BJT current. The doping profiles of impurities can also determinate that the ESD protection devices are suitable for the gate-driven design. For another issue in gate-driven design, coupled-voltage on the gate of ESD protection device must be optimized to avoid damaging the gate-oxide and surface channel of MOSFET.
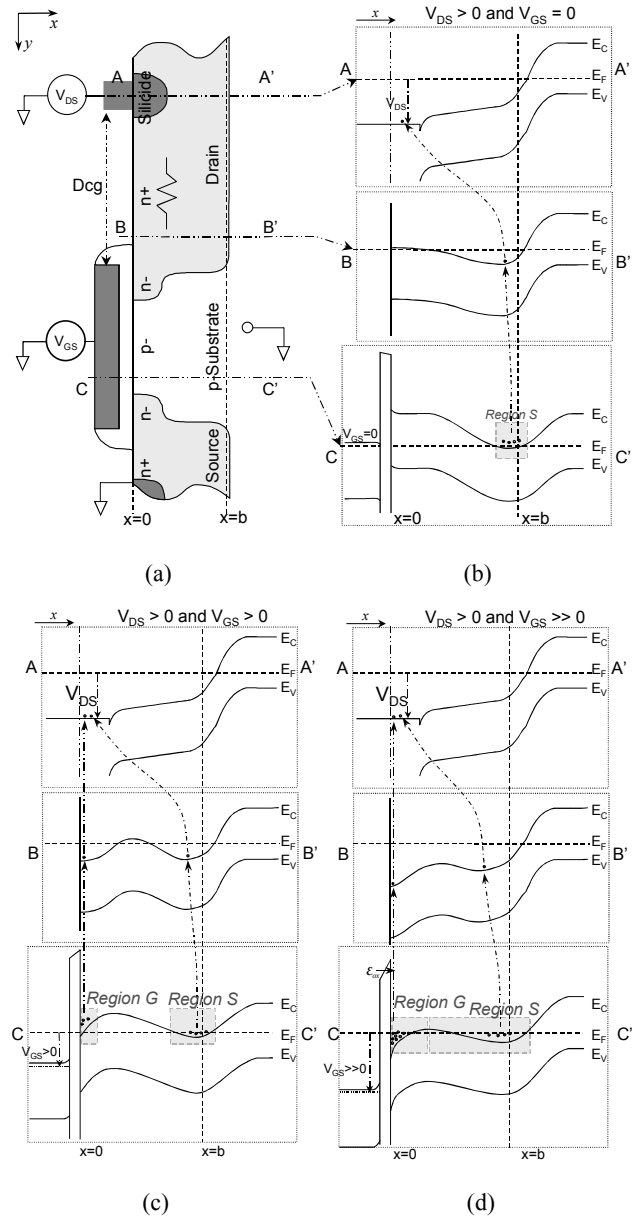

Fig. 4. Illustrate the energy band variations of NMOS device under different gate-driven operations.

Substrate-Triggered Effect

To explain the effect of substrate-triggered design, the energy-band diagrams with different substrate-triggered biases under the same drain bias are shown in Fig. 5. Different from the gate-driven design, the energy-band diagrams of substrate-triggered design can hardly be lowered as shown in Fig. 5(c) and 5(d), because the gate bias of MOSFET is held on ground. In Fig. 5(b), there is no bias on substrate. The current distribution region S of lateral-BJT in Fig. 5(b) is far small than those regions of substrate-triggered devices in Fig. 5(c) and 5(d), because the substrate bias lowers the energy bands in the substrate region and extend the current distribution region S. Device has the more current distribution region; the power dispersion has the more space to sustain the heat dispersion. So, substrate-triggered devices can sustain higher ESD robustness. By the explication, substrate bias does not damage gate-oxide and channel surface of

MOSFET, and the doping profile of impurities under gate-oxide can't clearly affect the effect of substrate-triggered design. Therefore, the ESD protection devices with substrate bias can have a much higher ESD level.
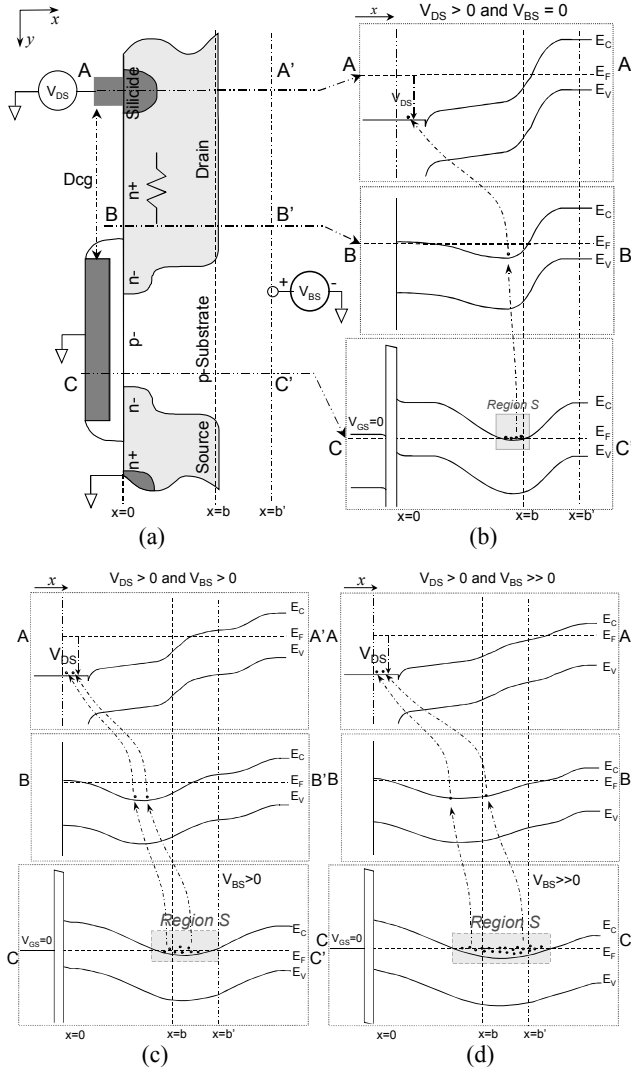

(a)   (b)

(c)   (d)

Fig. 5. Illustrate the energy band variations of NMOS device under different substrate triggered operations.

EXPERIMENTAL VERIFICATION

To investigate this gate-driven effect, different gate biases are applied to the gate of MOSFET and ESD current zaps into the drain of MOSFET. In the 0.35-µm CMOS process, the HBM-ESD measured results on both the NMOS and PMOS devices with different channel width (W) are shown in Fig. 6(a) and 6(b), respectively. The ESD level of the NMOS with W=600µm is initially increased while the gate bias increases from 0V to 4V. But, the ESD level is suddenly decreased while the gate bias is greater than 6V/8.5V for NMOS with 200-µm/600-µm channel width, as that shown in Fig. 6(a). There is a similar gate-driven effect on the PMOS device. In Fig. 6(b), the ESD level (in absolute value) of the PMOS with W=600µm is initially increased while the gate bias changes from 0V to -5V. But, the ESD level is suddenly decreased while the gate bias is lower than -5V.

The similar result in the 0.18-µm CMOS process is shown in

Fig. 7, where the second breakdown current It_2 is measured by 100-ns TLP system. But, there is obvious degradation when $V_G > 0.3V$ in Fig. 7. The value is far smaller than the degraded voltage in the 0.35-µm CMOS process. So, the gate-driven design is very hard to apply on sub-quarter-micron CMOS process technology except to finely tune the doping profile of substrate impurities under the gate.
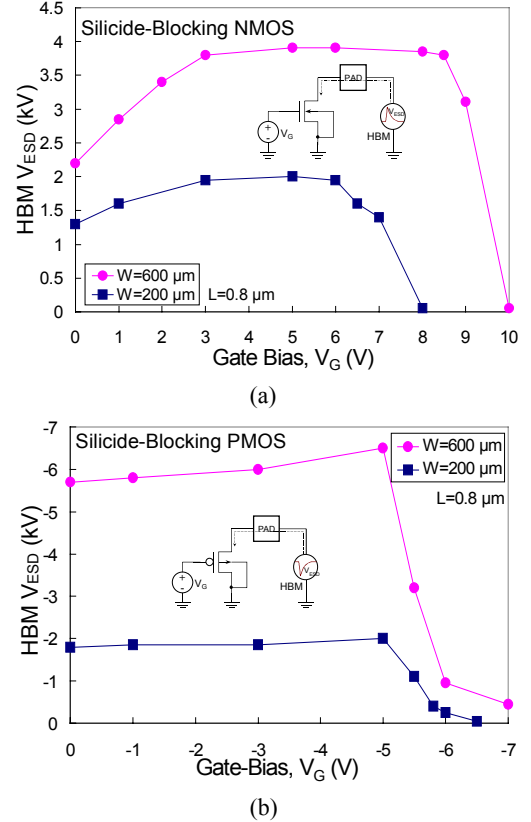

(a)

(b)

Fig. 6. The effect of the gate biases on the ESD robustness of (a) NMOS, and (b) PMOS for 0.35-µm CMOS process.

To avoid the degradation on the ESD level of the gate-driven devices, the substrate-triggered design had been reported to improve ESD level of the ESD-protection devices. To investigate the substrate-triggered effect on ESD robustness of NMOS, different substrate biases are applied to the substrate of NMOS and ESD current zaps into the drain of NMOS. In the 0.35-µm CMOS process, the HBM-ESD measured results are shown in Fig. 8(a) and 8(b) for the NMOS devices with different channel width and length. In Fig. 8(a), the ESD level of the NMOS with a device dimension of W=600µm and L=0.8µm can be significantly increased greater than 8kV while the substrate bias increases from 0V to only 0.8V. In Fig. 8(b), the NMOS device (W=200µm) with a shorter channel length and higher substrate bias can sustain a much higher ESD level. The ESD level of the NMOS with a channel length of 0.5µm under 0-V gate and substrate biases is only 2.8kV, but the ESD level is increased up to 4.4kV while the NMOS has a substrate bias of 2V. As shown in Fig. 8, the ESD level is not suddenly degraded while the substrate bias increases up to 2V. The substrate-triggered design can effectively improve ESD robustness of the ESD-protection devices without the sudden degradation as that shown in the gate-driven design. Therefore, this substrate-triggered design is more suitable to improve ESD robustness of the ESD-protection devices and circuits in the sub-quarter-micron CMOS technologies.
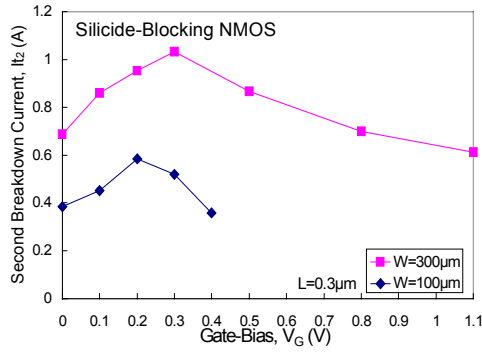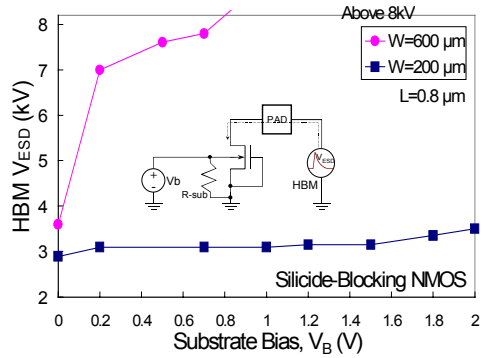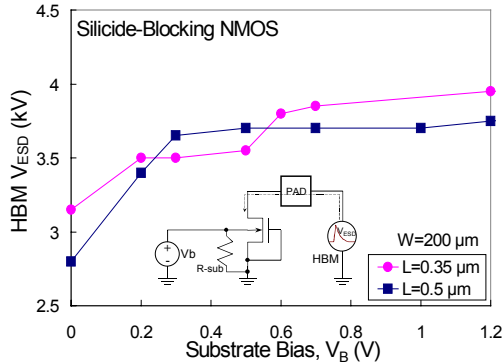
Fig. 7. The dependence of It_2 on the gate bias of the traditional finger-type NMOS for 0.18-µm CMOS process.

(a)

(b)

Fig. 8. The effect of the substrate biases on ESD robustness of NMOS devices with (a) different channel width, and (b) different channel length for 0.35-µm CMOS process.
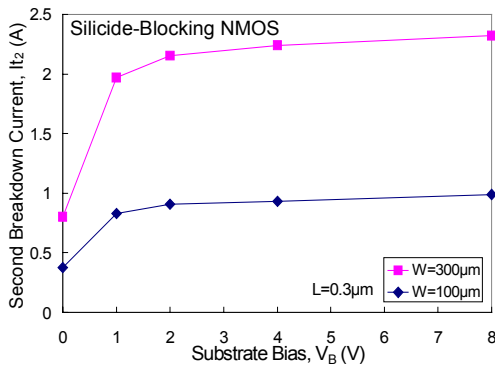

Fig. 9. The dependence of It_2 on the substrate bias of the substrate-triggered NMOS for 0.18-µm CMOS process.

For 0.18-µm CMOS process, the TLP-measured second breakdown current It_2 of NMOS with substrate-triggered design are shown in Fig. 9. The second breakdown current (It_2) is not suddenly degraded while the substrate bias increases up to 8V. With a substrate-triggered design, the NMOS (W/L=300µm /0.3µm) can sustain an ESD level of 3.3kV in the 0.18-µm CMOS process. The NMOS under the same device dimension but with gate-driven design has a maximum ESD level of only 0.8kV in the 0.18-µm CMOS process. This has verified the excellent effectiveness of the substrate-triggered technique to continually improve ESD robustness in sub-quarter-micron CMOS technology.

CONCLUSION

From the explication of energy-band diagram, the ESD current in the gate-driven device easily causes damage on the MOSFET. This effect will cause the degradation of ESD level for gate-driven devices. To design suitable gate-driven circuits, the doping profile of substrate must be fine tuned in MOSFET. However, there is no doping fine-tuned problem for the ESD protection devices with substrate-triggered design. It does not cause degradation on ESD level in the substrate-triggered devices. The substrate-triggered design therefore becomes the most effective solution for on-chip ESD protection in sub-quarter-micron CMOS technologies.

REFERENCES

[1] ESD Test Standard, ESD STM5.1, ESD Association, 1998.
[2] C. Jiang, E. Nowak, and M. Manley, "Process and design for ESD robustness in deep submicron CMOS technology," *Proc. of IEEE Int. Reliability Physics Symp.*, 1996, pp. 233-236.
[3] C. Duvvury, C. Diaz, and T. Haddock, "Achieving uniform nMOS device power distribution for sub-micron ESD reliability," *Tech. Dig. of IEDM*, 1992, pp.131-134.
[4] C. Duvvury and C. Diaz, "Dynamic gate coupling of NMOS for efficient output ESD protection," *Proc. of IEEE Int. Reliability Physics Symp.*, 1992, pp. 141-150.
[5] J. Chen, A. Amerasekera, and C. Duvvury, "Design methodology and optimization of gate-driven NMOS ESD protection circuits in submicron CMOS processes," *IEEE Trans. on Electron Devices*, vol. 45, no. 12, pp. 2448-2456, 1998.
[6] A. Amerasekera, C. Duvvury, V. Reddy, and M. Rodder, "Substrate triggering and salicide effects on ESD performance and protection circuit design in deep submicron CMOS processes," *Tech. Dig. of IEDM*, 1995, pp. 547-550.
[7] M.-D. Ker, T.-Y. Chen, and C.-Y. Wu, "Design of cost-efficient ESD clamp circuits for the power rails of CMOS ASIC's with substrate-triggering technique," *Proc. of IEEE Int. ASIC Conf. and Exhibit*, 1997, pp. 287-290.
[8] M.-D. Ker, T.-Y. Chen, C.-Y. Wu, H. Tang, K.-C. Su, and S.-W. Sun, "Novel input ESD protection circuit with substrate-triggering technique in a 0.25-µm shallow-trench-isolation CMOS technology," *Proc. of IEEE Int. Symp. on Circuits and Systems*, vol. 2, 1998, pp. 212-215.
[9] T.-Y. Chen, M.-D. Ker, and C.-Y. Wu, "Experimental investigation on the HBM ESD characteristics of CMOS devices in a 0.35µm silicided process," *Proc. of Int. Symp. on VLSI Technology, System, and Application*, 1999, pp.35-38.