COMPLEMENTARY SUBSTRATE-TRIGGERED SCR DEVICES FOR ON-CHIP ESD PROTECTION CIRCUITS

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ABSTRACT

The turn-on mechanism of SCR device is essentially a current triggering event. While a current is applied to the base or substrate of a SCR device, it can be quickly triggered on into its latching state. In this paper, the complementary substrate-triggered SCR devices, which are combined with the substrate-triggered technique and SCR devices, are first reported in the literature for using in the on-chip ESD protection circuits. A complementary style on the substrate-triggered SCR devices is designed to discharge both of the positive and negative ESD stresses on the pad. The total holding voltage of the substrate-triggered SCR device can be increased by adding the stacked diode string to avoid the transient-induced latchup issue in the ESD protection circuits. The on-chip ESD protection circuits designed with the proposed complementary substrate-triggered SCR devices for the I/O pad and power pad have been successfully verified in a 0.25-μm STI CMOS process with the HBM (MM) ESD level of >8kV (650V) in a small layout area.

I. INTRODUCTION

With the best ESD robustness in the smallest layout area, as comparing to other ESD protection devices (such as the diode, MOS, BJT, or field oxide device) in CMOS technology, the SCR device had been used in the on-chip ESD protection circuits for a long time [1], [2]. But, the SCR devices often have a higher switching voltage (~20V) in the sub-quarter-micron CMOS technology, which is generally greater than the gate-oxide breakdown voltage of the input stages. To provide more effective on-chip ESD protection, the low-voltage-trigger SCR (LVTSCR) [3] and the complementary-LVTSCR [4] had been invented to reduce the switching voltage of the SCR devices. Moreover, some advanced circuit techniques had been also reported to enhance the ESD level or the turn-on efficiency of ESD protection devices, such as the gate-coupled technique [5], the GGNMOS-triggered SCR [6], and the substrate-triggered technique [7]. However, another issue limiting the use of SCR devices is the latchup concern. Such SCR devices could be accidentally triggered on by noise pulse [8] when IC's are operated in normal circuit operating conditions.

In this paper, combining with the substrate-triggered technique, the novel p-type substrate-triggered SCR (P_STSCR) and the n-type substrate-triggered SCR (N_STSCR) devices for ESD protection are proposed and verified in a 0.25-μm CMOS process. Such novel substrate-triggered SCR devices are designed to be kept off during the normal circuit operating conditions, and to be quickly triggered on during the ESD-zapping conditions. The latchup issue among the SCR devices can be successfully solved by the proposed ESD protection circuits with stacked diode string.

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II. SUBSTRATE-TRIGGERED SCR DEVICES

The proposed device structures of P_STSCR and N_STSCR with stacked diode string are shown in Figs. 1(a) and 1(b), respectively. As comparing to the traditional lateral SCR device structure [1], an extra P+ diffusion is inserted into the substrate of the P_STSCR device structure as the trigger node for P_STSCR. The inserted P+ diffusion is connected out as the p-trigger node of the P_STSCR device. When a trigger current is applied into this trigger node, the P_STSCR will be triggered into its latching state. For the N_STSCR, an extra N+ diffusion is inserted into the N-well of the N_STSCR device structure as the trigger node. The inserted N+ diffusion is connected out as the n-trigger node of the N_STSCR device. When a trigger current is drawn out from thid trigger node, the N_STSCR will be triggered into its latching state. The current paths in the P_STSCR and N_STSCR devices are indicated by the dashed lines shown in Figs. 1(a) and 1(b), respectively.

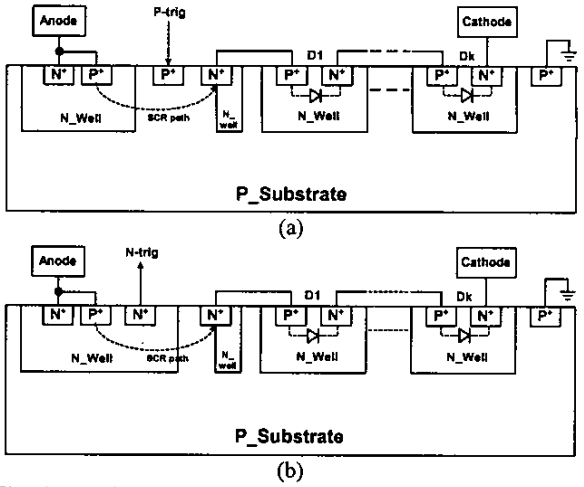


Fig. 1 Device structures of (a) the p-type substrate-triggered SCR (P_STSCR) device with stacked diode string, and (b) the n-type substrate-triggered SCR (N_STSCR) device with stacked diode string.

The number of diodes in the stacked diode string is depended on the power supply voltage of CMOS ICs in applications. To avoid the latchup issue, the total holding voltage will be designed greater than the power supply voltage. The total holding voltage (Vh) of a substrate-triggered SCR device with k-stacked diodes can be written as

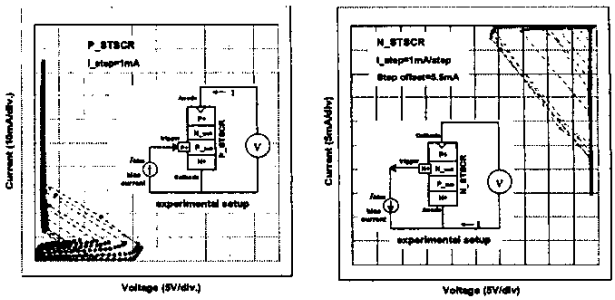
$$Vh = Vh_{\_SCR} + k \times V_D, \quad (1)$$

where $Vh_{\_SCR}$ is the holding voltage (~1.35V) of a P_STSCR (or N_STSCR) device, and V_D is the cut-in voltage (~0.6V) of a diode in forward-biased condition.

The P_STSCR and N_STSCR devices with different numbers of stacked diodes have been drawn in layout and fabricated in a 0.25-μm STI CMOS process. The DC I-V characteristics of stand-alone P_STSCR and N_STSCR devices are measured in Figs. 2(a) and 2(b), respectively. The experimental setups to measure the DC I-V characteristics of the P_STSCR and N_STSCR devices are also inserted into Figs. 2(a) and 2(b), respectively.

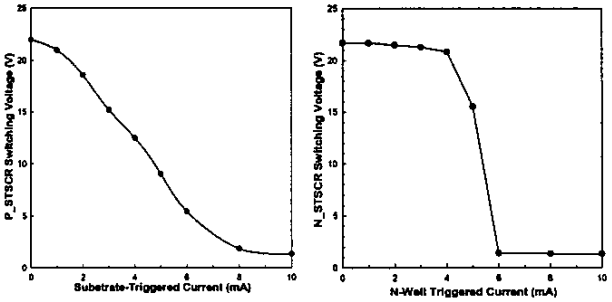
The dependences of the switching voltage of the P_STSCR and N_STSCR devices on the substrate/ well-triggered current are shown in Figs. 3(a) and 3(b), respectively. When the P_STSCR device has no substrate-triggered current (Ibias=0), the P_STSCR is turned on by its original N-well/P-substrate junction breakdown. In Fig. 2(a), the switching voltage of the P_STSCR device is as high as 22V, when the substrate-triggered current is zero. But, the switching voltage of the P_STSCR device is reduced to only 9V, when the substrate-triggered current is 5mA. Furthermore, the switching voltage of the P_STSCR device can be reduced to only 1.85V, when the substrate-triggered current is increased up to 8mA. Without through the avalanche breakdown mechanism, the P_STSCR can be triggered on by applying the trigger current into its trigger node. In the N_STSCR device, it also has the similar characteristics as that of the P_STSCR device.

With a much lower switching voltage, the turn-on speed of the P_STSCR / N_STSCR device can be further improved to quickly discharge the ESD current. This is a very excellent feature of this proposed ESD protection device for using in the on-chip ESD protection circuits in sub-quarter-micron CMOS processes. Fig. 4 shows the dependence of the total holding voltage of the ESD protection device realized by the P_STSCR with stacked diode string on the number of diodes under different temperatures. With increase of the number of stacked diodes, the holding voltage of ESD protection device is raised. However, the total holding voltage slightly reduces when the operating temperature is increased, because the current gain (β) of the parasitic bipolar transistor in the SCR device is increased with the increase of operating temperature. For safe applications in a 2.5-V CMOS IC, two diodes must be stacked with the P_STSCR or N_STSCR devices in the ESD protection circuits to avoid the latchup issue in normal circuit operating conditions.



(a) (b)

Fig. 2 The experimental setups and the measured DC I-V curves of (a) the P_STSCR device, and (b) the N_STSCR device, fabricated in a 0.25-μm shallow-trench-isolation (STI) CMOS process.



(a) (b)

Fig. 3 Dependences of the switching voltage of (a) the P_STSCR device on the substrate-triggered current, and (b) the N_STSCR device on the well-triggered current.

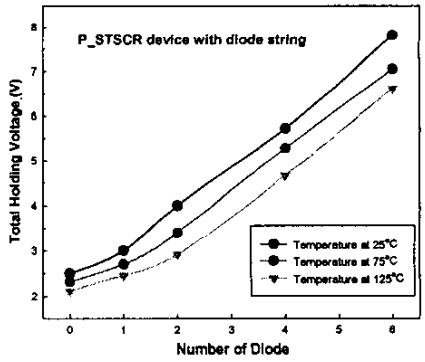


Fig. 4 Dependence of the total holding voltage of the P_STSCR with stacked diode string on the number of stacked diodes under different temperatures.

III. ON-CHIP ESD PROTECTION DESIGN

A. ESD protection designs for I/O pad

The ESD protection circuits for I/O pad, realized with the complementary substrate-triggered SCR devices, are shown in Figs. 5(a) and 5(b). In Fig. 5(a), the p-trigger (n-trigger) node of the P_STSCR (N_STSCR) device is

connected to the output of the inv_1 (inv_2). The input of the inv_1 (inv_2) is connected to VDD (VSS) through the resistor R. The resistor R is better realized by using the N+ diffusion resistance for the concern of antenna effect [9]. A capacitor C is placed between the input of the inv_1 (inv_2) and VSS (VDD). This capacitor can be formed by the parasitic capacitance at the input node of the inverter. In the normal circuit operating conditions with VDD and VSS power supplies, the input of inv_1 is biased at VDD. Therefore, the output of the inv_1 is biased at VSS due to the turn on of NMOS in the inv_1. The p-trigger node of the P_STSCR device is kept at VSS by the output of the inv_1, so the P_STSCR device is guaranteed to be kept off in the normal circuit operating conditions. For inv_2 in the normal operating conditions, its gate is biased at VSS. Thus, the output of the inv_2 is kept at VDD due to the turn on of the PMOS in the inv_2. The n-trigger node of the N_STSCR device is biased at VDD by the output of the inv_2, so the N_STSCR is also guaranteed to be kept off in the normal circuit operating conditions.

Under the positive-to-VSS ESD-zapping condition, the input of the inv_1 is initially floating with a zero voltage level, thereby the PMOS of the inv_1 will be turned on due to the positive ESD voltage on the pad. So, the output of the inv_1 is charged up by the ESD energy to generate the trigger current into the p-trigger node of the P_STSCR device.

Therefore, the P_STSCR device is triggered on by the triggered current generated from the output of the inv_1, and the ESD current is discharged from pad to VSS through the P_STSCR device. The RC time constant is designed to keep the input of the inv_1 at a relatively low voltage level during ESD stress condition. Under negative-to-VDD ESD-zapping condition, the input of the inv_2 is initially floating with a zero voltage level, and the NMOS of the inv_2 will be turned on due to the negative ESD voltage at the pad. So, the output of the inv_2 is pulled down by the negative ESD voltage to draw the trigger current out from the n-trigger node of the N_STSCR device. Therefore, the N_STSCR device is triggered on by the triggered current generated from the output of the inv_2, and the ESD current is discharged from pad to the grounded VDD pin through the N_STSCR device.

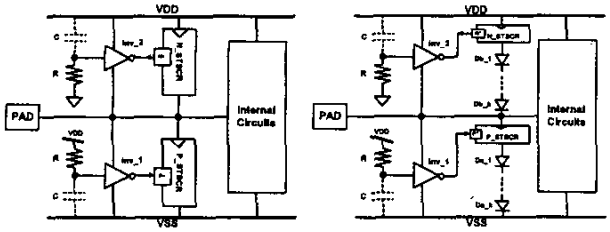


Fig. 5 (a) The ESD protection circuit designed with the substrate-triggered SCR devices for the I/O pad. (b) The modified design of (a) to avoid latchup issue.

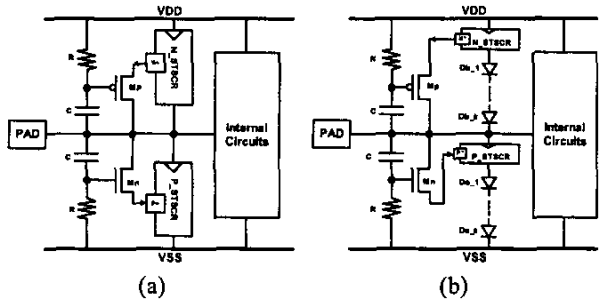


Fig. 6 (a) Another ESD protection circuit designed with the substrate-triggered SCR devices for the I/O pad. (b) The modified design of (a) to avoid latchup issue.

Fig. 5(b) is a modified design of Fig. 5(a) to make the ESD protection circuit latch-up free under normal circuit operating conditions. The total holding voltage of the ESD protection device must be designed greater than the power supply voltage. By changing the number of stacked diodes, the total holding voltage can be adjusted to meet different circuit applications.

Fig. 6(a) shows another ESD protection circuit designed with the substrate-triggered SCR devices for the I/O pad. When a positive-to-VSS ESD zapping on the pad, the positive transient voltage on the pad is coupled through the capacitor C to the gate of Mn. The Mn with a positive coupled gate bias can be turned on to conduct some ESD current from the pad into the p-trigger node of the P_STSCR device. Therefore, the P_STSCR is triggered on to discharge the ESD current from the pad to VSS. When a negative-to-VDD ESD zapping on the pad, the negative transient voltage on the pad is coupled through the capacitor C to the gate of Mp. The Mp with a negative coupled gate bias can be turned on to draw some ESD current out from the n-trigger node of the N_STSCR device. Therefore, the N_STSCR is triggered on to discharge the ESD current from VDD to the pad. The RC value in Fig. 6(a) must be tuned at the same value, where the coupled voltage under normal circuit operating conditions must be smaller than the threshold voltage of Mn/Mp, but greater than the threshold voltage of Mn/Mp under ESD zapping conditions. Fig. 6(b) is the modified design of Fig. 6(a) with the stacked diodes to overcome the latchup issue.

B. ESD protection design for the power pad

The P_STSCR / N_STSCR device can also be applied to design the power-rail ESD clamp circuits. The VDD-to-VSS ESD clamp circuit realized with the P_STSCR / N_STSCR device and the stacked diode string are shown in Figs. 7(a) and 7(b), respectively. The function of the ESD-detection circuit, which is formed with resistor, capacitor, and inverter, is similar to the ESD-detection circuit used in the input pad, but the RC is designed with a time constant of about ~1μs to distinguish

the VDD power-on event (with a rise time of ~ms) or ESD-stress events (with a rise time of ~ns). During normal VDD power-on transition (from low to high), the input of the inverter in Fig. 7(a) can follow up in time with the power-on VDD signal, so the output of the inverter is kept at zero. Hence, the P_STSCR device with diode string are kept off and don't interfere the functions of internal circuits.

When a positive ESD voltage is applied to VDD pin with VSS pin relatively grounded, the RC delay will keep the input of the inverter at a low voltage level for a relatively long time, therefore the output of the inverter will be pulled high to trigger the P_STSCR device. While the P_STSCR device is triggered on, the ESD current is discharged from VDD to VSS through the P_STSCR device and the stacked diode string. With suitable ESD-detection circuit, the P_STSCR device can be quickly triggered on to discharge the ESD current.

In Fig. 7(b), during normal VDD power-on transition, the input of the inv_1 will be biased at VDD, so the output of the inv_1 (the input of the inv_2) will be biased at zero, therefore the output of the inv_2 will be kept at VDD. Hence, the N_STSCR device with diode string are kept off and don't interfere the functions of internal circuits. However, when a positive ESD voltage is applied to the VDD pin, the RC delay will keep the input of the inv_1 at a low voltage level for a relatively long time, therefore the output of the inv_1 (the input of the inv_2) will become high, then the output of the inv_2 will be kept at low voltage level to trigger the N_STSCR device. While the N_STSCR device is triggered on, the ESD current is discharged from VDD to VSS through the N_STSCR device and the stacked diode string.

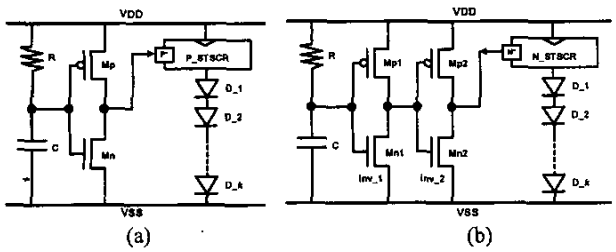


Fig. 7 The VDD-to-VSS ESD clamp circuit realized by (a) the P_STSCR device with stacked diode string, and (b) the N_STSCR device with stacked diode string.

IV. EXPERIMENTAL RESULTS

A. ESD robustness

The proposed ESD protection devices and circuits for the I/O and the power pads have been fabricated in a 0.25-μm CMOS process. The layout top views of the P_STSCR device with two stacked diodes and the N_STSCR device with three stacked diodes are shown in Figs. 8(a) and 8(b), respectively. The device dimensions of the P_STSCR and N_STSCR are drawn as 20μm×21μm, and each diode has a 30μm×3μm anode layout area. The human-body-model (HBM) and machine-model (MM) ESD stresses are used to verify the ESD level of the proposed ESD protection circuits designed with the substrate-triggered SCR devices and different number of the stacked diodes. The ESD test results are compared in Fig. 9.

The ESD-generated power across the ESD protection devices is Power ≅ I_{ESD}×Vhold. Thus, the HBM and MM is decreased when the number of stacked diodes is increased. For power supply voltage of 2.5V, the ESD protection circuit can be free to latchup issue even if the operating temperature is at 125°C, when the number of stacked diodes is two. In this condition, the HBM (MM) is still as high as >8kV (650V), it is still high enough for ESD protection. The ESD levels of substrate-triggered SCR devices are the same as that of the traditional SCR device under the same layout area because of the same discharging path and area. The aim of this literature is to reduce the switching voltage, to avoid the transient-induced latchup issue, and to enhance the turn-on speed of the SCR device. In comparison, for gate-grounded NMOS device in the same 0.25-μm CMOS process, it consumes a large layout area of 25.8μm×60μm to sustain the ESD level of only 3.5kV.

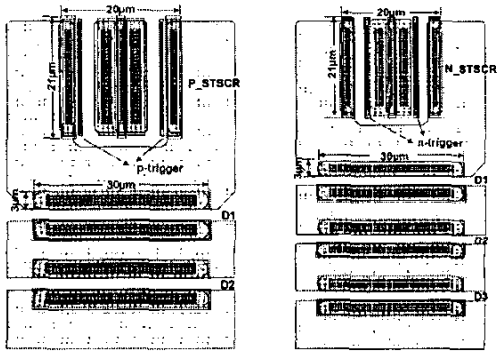


Fig. 8 The layout top views of (a) the P_STSCR with two stacked diodes, and (b) the N_STSCR device with three stacked diodes.

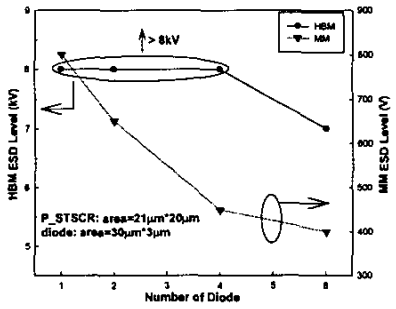


Fig. 9 Dependence of HBM and MM ESD levels on the number of stacked diodes for the ESD protection circuit realized with the P_STSCR device and stacked diode string.

B. Turn on verification

In order to verify the functions of the ESD protection circuits realized with the R, C, inverter, and P_STSCR with stacked diode string, a voltage pulse with a pulse width of 400ns and a rise time of 10ns to simulate the ESD triggering is applied to the VDD of Fig. 7(a), which the VSS is connected to ground. In Fig. 10, a 0-to-5V voltage pulse applied on the VDD is clamped to 1.6V (3.2V) by the ESD protection circuit with P_STSCR and zero (two) stacked diodes. By increasing the number of the stacked diodes, the clamped voltage on VDD is increased.

By using this method, the turn-on efficiency of the

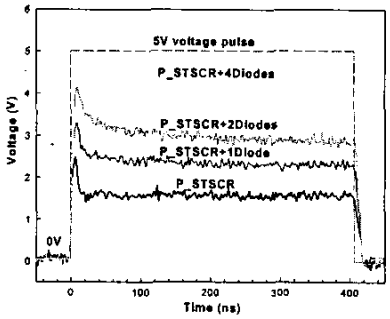


Fig. 10 The measured voltage waveforms to verify the turn-on efficiency of the power-rail ESD clamp circuit in Fig.7(a) with different number of tacked diodes. A 0-to-5V voltage pulse is applied to the VDD node with the VSS grounded.

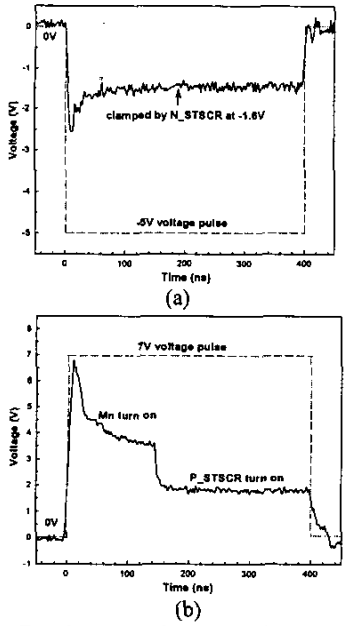


Fig. 11 (a) The clamped voltage waveform on the I/O pad of ESD protection circuit in Fig. 5(a) with a negative 0-to-5V voltage pulse to simulate the negative-to-VDD ESD-stress condition. (b) The clamped voltage waveform on the I/O pad of ESD protection circuit in Fig. 6(a) with a positive 0-to-7V voltage pulse to simulate the positive-to-VSS ESD-stress condition.

ESD protection circuit for I/O pad can be also verified. The clamped voltage waveform on the I/O pad of ESD protection circuit in Fig. 5(a) with a negative 0-to-5V voltage pulse to simulate the negative-to-VDD ESD-stress condition is measured in Fig. 11(a). The -5V voltage pulse is clamped to about -1.6V by the N_STSCR in the ESD protection circuit of Fig. 5(a). With a positive 0-to-7V voltage pulse to simulate the positive-to-VSS ESD-stress condition, the clamped voltage waveform on the I/O pad of ESD protection circuit in Fig. 6(a) is measured in Fig. 11(b). In Fig. 11(b), the NMOS, Mn in the ESD protection circuit of Fig. 6(a), will be first turned to conduct some ESD current to trigger on the P_STSCR device, and then the P_STSCR clamps the voltage to 1.6V. This has verified the effectiveness of the proposed ESD protection circuits designed with the substrate-triggered technique and the SCR devices. To achieve latchup free, some diodes must be stacked with the substrate-triggered SCR devices in the ESD protection circuits.

V. CONCLUSION

The ESD protection circuits, designed with the proposed complementary substrate-triggered SCR devices with stacked diode string and ESD-detection circuit, have the advantages of adjustable switching voltage and tunable holding voltage, faster turn-on speed, smaller occupied layout area, and much higher ESD robustness. Therefore, they are very useful in CMOS IC products fabricated in the sub-quarter-micron CMOS processes.

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