ESD PROTECTION CIRCUITS WITH NOVEL MOS-BOUNDED DIODE STRUCTURES

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ABSTRACT

On-chip ESD protection circuits realized with novel diode structures without the field-oxide boundary across the p/n junction are proposed. A PMOS (NMOS) is especially inserted into the diode structure to form the PMOS-bounded (NMOS-bounded) diode, which is used to block the field oxide isolation across the p/n junction in the diode structure. Without the field oxide boundary across the p/n junction of diode structure, the proposed PMOS-bounded and NMOS-bounded diodes can sustain much higher ESD stress, especially under the reverse-biased condition. Such PMOS-bounded and NMOS-bounded diodes are fully process-compatible to general CMOS processes without additional process modification or mask layers. The ESD protection circuits designed by such new diodes with different junction perimeters have been successfully verified in a 0.35-μm CMOS process.

1. INTRODUCTION

With the shallower junction, much thinner gate oxide, salicided (self-aligned silicided) diffusion, Cu inter-connection, and LDD (Lightly-Doped Drain) structure used on the MOSFET devices, electrostatic discharge (ESD) issue has become a main reliability concern of CMOS integrated circuits in sub-quarter-micron CMOS technology [1]-[3]. To sustain a reasonable ESD stress (typically, ±2kV in the human-body-model ESD event [4]) for safe mass production, on-chip ESD protection circuits have to be added into the IC products. The typical ESD protection circuit with double diodes for a pad is shown in Fig. 1 [5], where the ESD clamp circuit between the VDD and VSS power rails are often added into the chip to avoid the ESD damages located in the internal circuits [6].

When the diodes are stressed by the ESD pulse under the reverse-biased stress conditions, which are the positive-to-VSS (PS-mode) ESD stress for N-type diode and the negative-to-VDD (ND-mode) ESD stress for P-type diode, the diffusion boundary to the field-oxide isolation is easily damaged by ESD to cause a very low ESD robustness [7]. The weakest point at the boundary between the field-oxide shallow-trench isolation (STI) and the diffusion edge of the diode structure is illustrated in Fig. 2, where the field-oxide region near to the P+ diffusion has a pull-down structure. When the p/n junction is reverse biased during ESD stress, the breakdown point is located at the boundary between the P+ diffusion and field-oxide region. Due to the limit area of the boundary for heat dissipation, this pull-down structure on the field-oxide boundary causes the P+ diffusion having a lower ESD robustness on its diffusion edge. If the CMOS process has the silicided diffusion, the silicide layer covered on the P+ diffusion causes a bend-down corner at the boundary between the P+ diffusion and field-oxide region. This bend-down corner further causes the diode being more easily damaged by ESD. Thus, the ESD protection circuits formed by double diodes often have lower ESD robustness in the reverse-biased ESD-stress conditions (PS-mode and ND-mode ESD stresses), even if the diodes have been drawn with larger silicon area. In process technology, the silicide-blocking mask is therefore used to remove the silicided layer covered on the P+ diffusion in Fig. 2 for improving ESD robustness. However, the extra cost and throughput time delay on wafer fabrication with the additional mask layer and process steps will be increased.

In this paper, the novel diode structures, called as NMOS-bounded diode and PMOS-bounded diode, are proposed to significantly improve ESD robustness of CMOS IC's in deep-submicron CMOS processes. With the new proposed diode structures, the on-chip ESD protection circuits for input, output, and power pads have been designed and practically verified in a 0.35-μm polycided CMOS process.

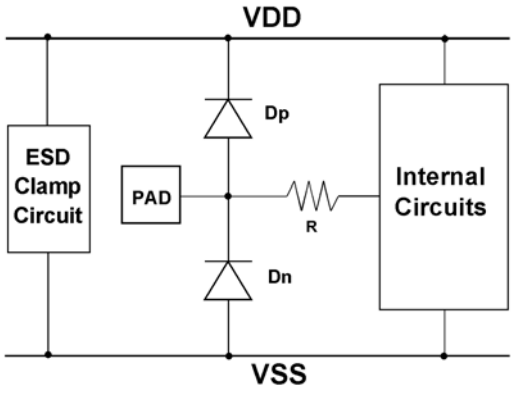


Fig. 1 The typical ESD protection circuit with double diodes for an input pad and the power-rail ESD clamp circuit.

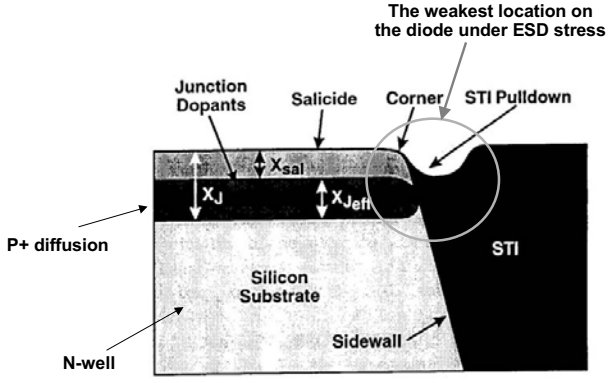
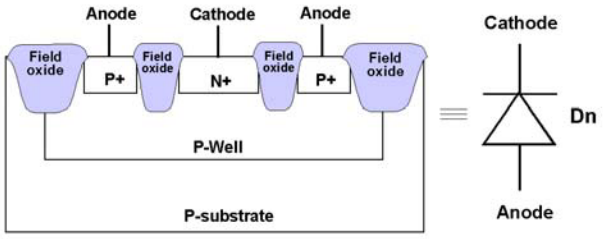


Fig. 2 The pull-down weakest point at the boundary between the field-oxide shallow-trench isolation (STI) and the diffusion edge of the diode structure.

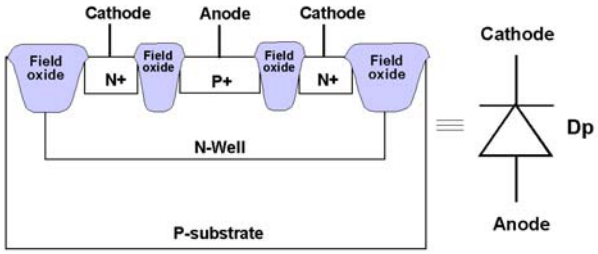
2. THE DIODE STRUCTURES

2.1. Normal N-type and P-type diodes

The top view and cross-sectional view of the normal N-type diode (Dn) and P-type (Dp) realized in the 0.35-μm polycided CMOS process are shown in Figs. 3(a) and 3(b), respectively. For the normal N-type diode, N+ diffusion (as the cathode) is placed in a P-well in P-substrate to form the p/n junction of the diode. The anode of such an N-type diode is connected out by the P+ diffusion in the P-well (or p-substrate). For the normal P-type diode, P+ diffusion (as the anode) is placed in an N-well to form the p/n junction of the diode. The cathode of such a P-type diode is connected out by the N+ diffusion in the N-well. Such diodes had been fabricated in the testchip to verify its ESD robustness.



(a)



(b)

Fig. 3 The device cross-sectional views of the (a) normal N-type diode, and (b) normal P-type diode, in CMOS process.

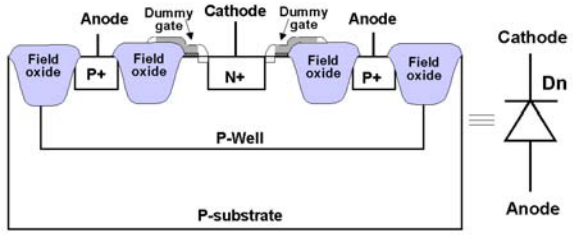
2.2. Poly-Bounded N-type and P-type diodes

To overcome the weakest ESD-damaged lactation at the p/n junction diffusion to the field-oxide boundary, a modified diode structure with dummy gate [7], called as the poly-bounded N-type (P-type) diode, is shown in Figs. 4(a) and 4(b).

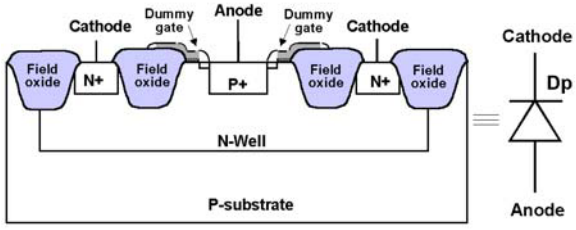
As comparing to Fig. 3, the field-oxide isolation regions between the P+ and N+ diffusions are removed away from the N+ (P+) diffusion of the normal N-type (P-type) diode and replaced by the dummy poly gates. The dummy poly gates are located half on the P-Well (N-Well) region and half on the field-oxide region. Therefore, there is no field-oxide boundary to the N+ (P+) diffusion edge of the poly-bounded N-type (P-type) diode. Without the field-oxide boundary at the p/n junction of the diodes, the pull-down and bend-down corner in Fig. 2 to cause low ESD robustness can be overcome. Such diodes had been also fabricated in the testchip to verify its ESD robustness.

2.3. NMOS-Bounded and PMOS-Bounded diodes

The layout top views and the device cross-sectional views of the proposed NMOS-bounded diode and PMOS-bounded diode are shown in Figs. 5(a) and 5(b), respectively. The N(P)MOS-bounded diode has a N(P)MOS structure inserted in the diode structure.

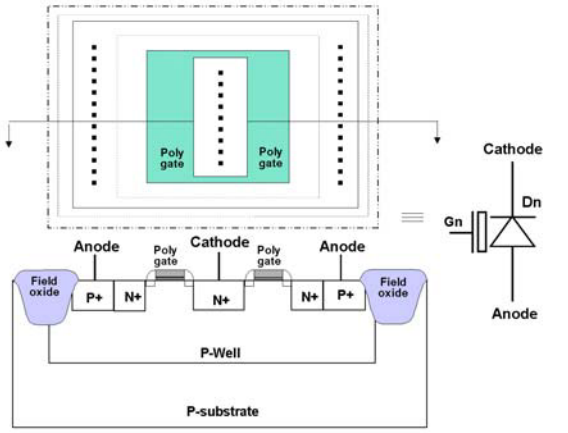


(a)

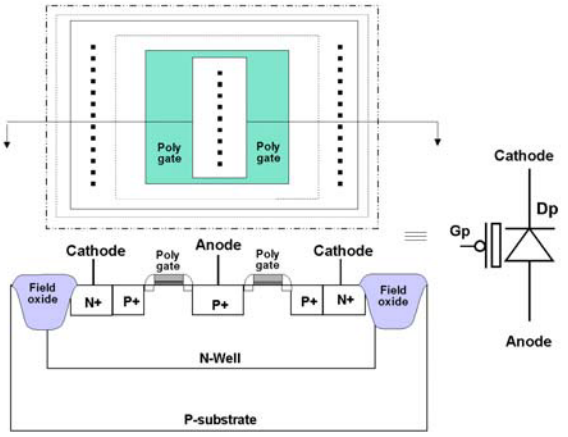


(b)

Fig. 4 The device cross-sectional views of the (a) poly-bounded N-type diode, and (b) poly-bounded P-type diode, in CMOS process.



(a)



(b)

Fig. 5 The layout top views and the device cross-sectional views of the (a) NMOS-bounded diode, and (b) PMOS-bounded diode, in CMOS process.

The NMOS-bounded diode has a diode cathode of N+ diffusion, which does not touch the P+ diffusion in the diode structure. The diode anode of P+ diffusion directly touches another N+ diffusion in the NMOS-bounded diode, where this N+ diffusion is floating. The anode of the PMOS-bounded diode is the P+ diffusion in the center, which does not touch the N+ diffusion. The cathode of diode is the N+ diffusion, which directly touches another P+ diffusion in the structure, where this P+ diffusion is floating. In this N(P)MOS-bounded diode, the poly gate is fully covered by the N+ (P+) implantation, therefore the gate can be successfully formed on the NMOS (PMOS) channel. If there is correct gate bias on the NMOS (PMOS) gate, the diode turn-on speed can be enhanced to bypass the ESD current. Therefore, it can provide more effective protection to the internal circuits. The poly gate in the layout top view shown in Fig. 5 has a close-loop ring to block the field-oxide boundary from the cathode N+ diffusion (anode P+ diffusion) of the N(P)MOS-bounded diode structure. The proposed N(P)MOS-bounded diode is fully compatible to the general CMOS processes without any additional process step or extra mask layer. Such novel diodes had been also fabricated in the testchip to verify its ESD robustness, and to compare with the normal diode and poly-bounded diode in a 0.35-μm CMOS process.

3. ESD PRPOTECTION CIRCUITS WITH THE MOS-BOUNDED DIODES

By using the proposed NMOS-bounded or PMOS-bounded diodes, novel ESD protection circuits can be designed with higher ESD robustness and better protection capability to protect the internal circuits.

3.1. ESD Protection Circuits for I/O Pad

The ESD protection circuits with the NMOS-bounded and PMOS-bounded diodes for the input or output pads are shown in Figs. 6(a) and 6(b). In Fig. 6(a), the PMOS and NMOS in the diode structures are kept off when the IC is in the normal operation condition with the VDD and VSS biases. In Fig. 6(b), the gate-couple technique is applied to control the gate of the NMOS-bounded and PMOS-bounded diodes to speed up the turn-on (breakdown under reverse-biased) speed of the MOS-bounded diodes under the PS-mode and ND-mode ESD stress. Therefore, it can provide better and effective protection function to the internal circuits.

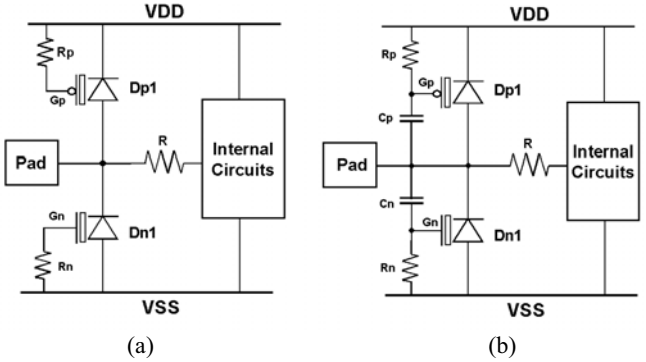


Fig. 6 The ESD protection circuits with the NMOS-bounded and PMOS-bounded diodes for the input or output pads, where (a) poly gate of the N(P)MOS-bounded diode is connected to VSS (VDD) through a resistor, and (b) gate-couple technique is applied.

3.2. Power-Rail ESD Clamp Circuits

The power-rail (VDD-to-VSS) ESD clamp circuits realized with the NMOS-bounded diode or PMOS-bounded diode under reverse-biased condition in the VDD-to-VSS ESD stress are shown in Fig. 7(a) ~ 7(d). In Fig. 7(a) ~ 7(b), the gate of NMOS-bounded or PMOS-bounded diode is controlled by the RC-based ESD detection circuit, where the RC has a time constant of ~ 1μs. In Fig.7(c) ~ 7(d), the NMOS-bounded or PMOS-bounded diode is controlled by the gate-couple design.

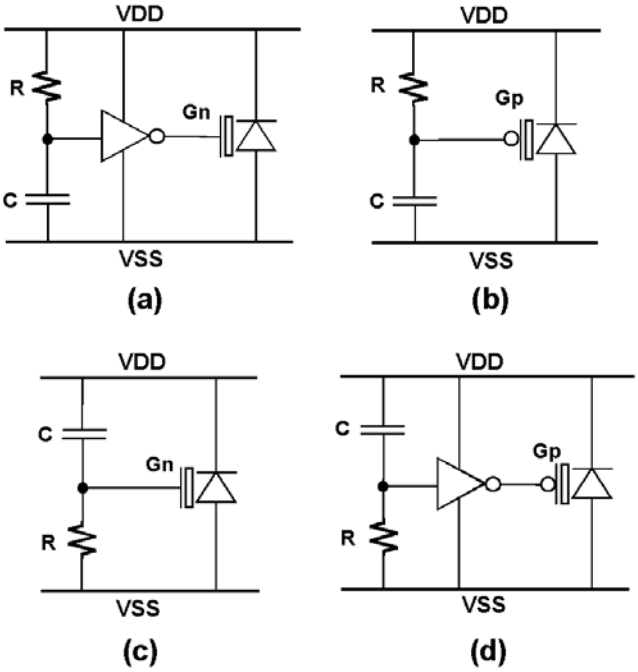


Fig. 7 The ESD protection circuits with the NMOS-bounded and PMOS-bounded diodes under reverse-biased condition for power-rail protection, where (a) with RC-based ESD detection circuit to control NMOS-bounded diode, (b) with RC-based ESD detection circuit to control PMOS-bounded diode, (c) with gate-couple technique to control NMOS-bounded diode, and (d) with gate-couple technique to control PMOS-bounded diode.

3.3. Whole-Chip ESD Protection Networks

For a complex VLSI, the power lines for different circuit groups are often separated to block the noise between different circuit groups, and to supply the enough power for circuit operation. But, an IC with the separated power lines often has some unexpected ESD damages located on the interface circuits between the circuit groups. To avoid the ESD damage on the interface or internal circuits, the whole-chip ESD protection network formed by the ESD-connection cell is added between the separated power lines. The NMOS-bounded and PMOS-bounded diodes in stacked configuration can be placed between the separated power rails to provide the ESD current discharging paths. The ESD protection networks realized with NMOS-bounded and PMOS-bounded diodes and ESD buses protection scheme between the separated power rails for the CMOS IC with many separated power lines are shown in Figs. 8(a) ~ 8(d). By using these ESD protection networks, the internal circuits of CMOS IC can be fully protected against ESD damage.

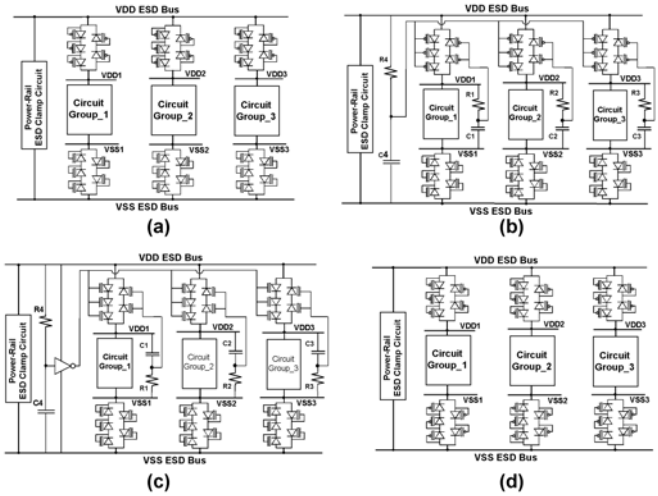


Fig. 8 Examples of separated power lines ESD protection design with NMOS- bounded and PMOS-bounded diodes and ESD buses protection scheme.

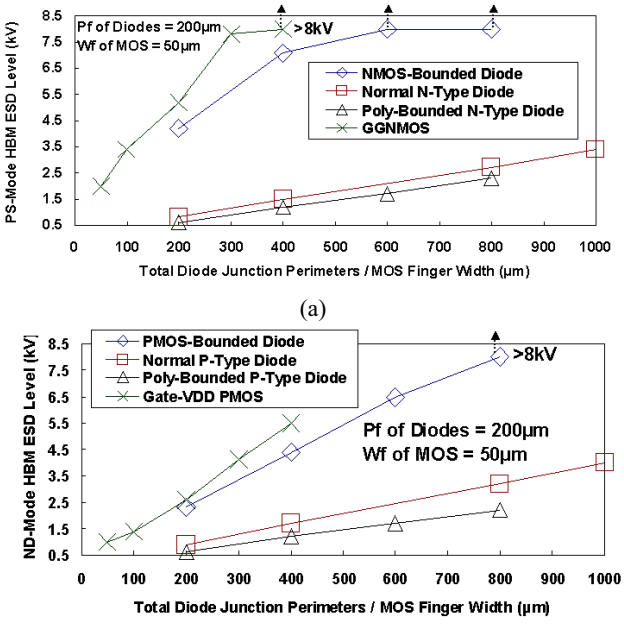


Fig. 9 Dependence of HBM ESD robustness on the total junction perimeters of different diodes under (a) PS-mode, and (b) ND-mode, ESD stress.

4. EXPERIMENTAL RESULTS

The ESD protection circuits with the proposed new diodes, the traditional normal diodes, and the poly-bounded diodes had been fabricated in a 0.35-μm polycided CMOS process. The human-body-model (HBM) ESD tester is used to verify their ESD robustness. The failure criterion is defined at the leakage current greater than 1μA at 3.3-V revised bias.

Figs. 9(a) and 9(b) show the HBM ESD level of the ESD protection circuits realized with different total diode junction perimeters or total MOSFET's finger width under PS-mode and ND-mode ESD stress conditions.

From the experimental results, the NMOS-bounded diode and PMOS-bounded diode have much higher ESD level than the normal diodes and poly-bounded diodes. The gate-grounded NMOS and gate-VDD PMOS are also tested and compared in Fig. 9. Although the ESD level of the gate-grounded NMOS and gate-VDD PMOS seem to be higher, the non-uniform turned-on issue often happens to the gate-grounded NMOS and gate-VDD PMOS to degrade its ESD performance in the real chip applications due to the snapback effect of the lateral BJT in the MOS structures. Therefore, the proposed NMOS-bounded and PMOS-bounded diodes are more suitable than the normal diodes, poly-bounded diodes, and MOSFET's for ESD protection design in deep-submicron CMOS processes.

5. CONCUSION

The proposed NMOS-bounded and PMOS-bounded diodes are more suitable for on-chip ESD protection design than the normal N-type (P-type) and poly-bounded N-type (P-type) diodes in deep-submicron CMOS processes. As applying the NMOS-bounded and PMOS-bounded diodes in the ESD protection circuits, the gates of the N(P)MOS-bounded diodes can be further controlled by ESD detection circuit, for example, RC-based or gate-couple circuits. Therefore, the diode turn-on speed can be further enhanced to effectively discharge the ESD current.

6. REFERENCES

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