ESD PROTECTION DESIGN TO OVERCOME INTERNAL DAMAGES ON INTERFACE CIRCUITS OF CMOS IC WITH MULTIPLE SEPARATED POWER PINS

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ABSTRACT

This paper reports a real case for ESD level improvement on a CMOS IC product with multiple separated power pins. After ESD stress, the internal damage has been found and located at the interface circuit connecting different circuit blocks with different power supplies. Some ESD designs are implemented to rescue this IC product to meet the required ESD specification. By adding only an extra ESD clamp NMOS with a channel width of 10 μm between the interface node and ground line, the HBM ESD level of this IC product can be improved from the original 0.5 kV to 3 kV. By connecting the separated VSS power lines through the ESD conduction circuit to a common VSS ESD bus realized by the seal ring, the HBM ESD level of the second version IC product with 12 separated power supplies pairs can be significantly improved from the original 1 kV up to > 5 kV, without noise coupling issue.

I. INTRODUCTION

ESD (Electrostatic Discharge) phenomenon continues to be a serious reliability issue in CMOS IC's, because of technology scaling and high integration of circuit blocks [1]. To improve ESD robustness, some circuit techniques such as gate-coupled design or substrate-triggered design [2]-[6] had been used in the input/output ESD protection circuits of CMOS IC's. However, when performing the power pin to power pin ESD stress according to ESD standards [7]-[8], even with the ESD protection circuits on the input/output pins and between VDD and VSS power rails, some unexpected ESD damages may still happen across the internal circuits of CMOS IC's [9]-[13].

In this paper, a real case of internal ESD damage on interface circuit of a CMOS IC product in a 0.35-μm CMOS process with multiple separated power pins is reported. This IC as a multiple clock generator has more than ten separated power supplies, which are fully isolated from each other because of noise coupling issue. The solutions used to improve its ESD level are experimentally verified in this work.

II. ESD FAILURE IN CMOS IC WITH MULTIPLE SEPARATED POWER PINS

A clock generator IC has been fabricated in a 0.35-μm CMOS process and used to supply multiple clock signals to synchronize chip sets working in a system. To prevent the noise coupling issue, the power rails of circuit blocks in this IC are all isolated from each other, as shown in Fig. 1. To protect IC from ESD damage, the ESD protection circuits are traditionally placed between I/O pads and VDD lines, I/O pads and VSS lines, and VDD and VSS power rails. Referring to Fig. 2, the ESD protection devices Mn1, Mp1, Mn2, and Mp2 are placed on the I/O pads to their corresponding power rails. In general digital I/O cell layout, the total channel widths of NMOS and PMOS are often drawn with larger device dimensions.

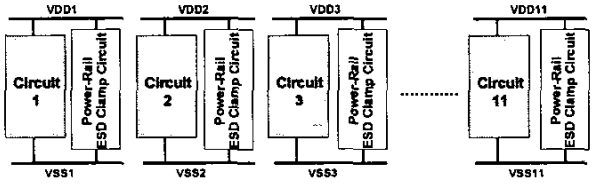

Fig.1 The schematic diagram of the CMOS IC with multiple separated power pairs.

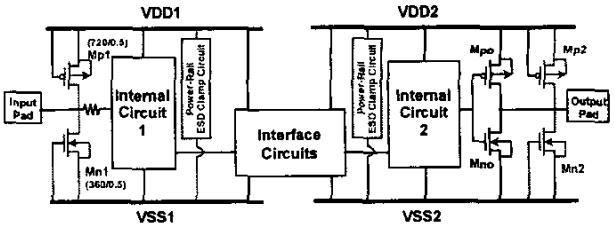

Fig.2 The ESD protection scheme in the CMOS IC with multiple separated power pins.

When the I/O cell is used as an input pad, the NMOS (PMOS) devices are turned off by connecting all the poly gate fingers to VSS (VDD) as ESD protection devices. When the I/O cell is used as an output pad, some poly gate fingers of the MOS are tied to pre-buffer circuit to be output driver. The number of poly gate fingers tied to pre-buffer circuit depends on the demand of output driving capability, and the other poly gate fingers are turned off by tied to VSS or VDD as ESD protection devices. In this IC product, the NMOS and PMOS in the I/O cell have same channel length of 0.5 μm. The total channel width of NMOS is 360 μm, and that of PMOS is 720 μm. Therefore, the ESD protection devices used in the input pad of this IC

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product have NMOS of 360/0.5 and PMOS of 720/0.5 (μm/μm). On the other hand, the size of output ESD protection devices, Mn2 and Mp2, depends on the output driving capability demand.

The cell layouts of power pads (include VDD pad and VSS pad) are the same as the I/O cell. In the power cell layout, the gate of NMOS is tied to ground and the gate of PMOS is tied to VDD, thus the NMOS and PMOS are both used as the power-rail ESD clamp circuits, as those shown in Fig. 3.

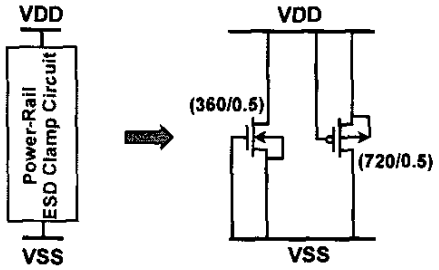
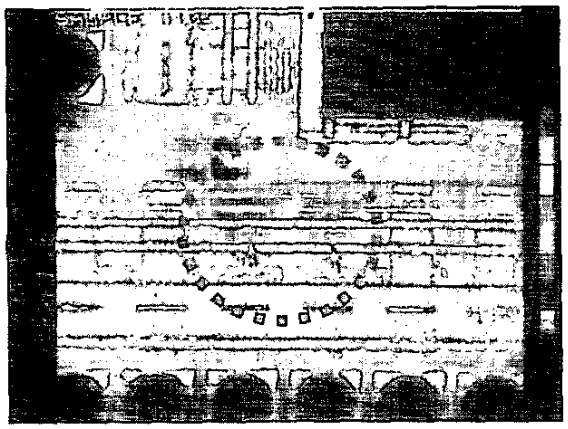
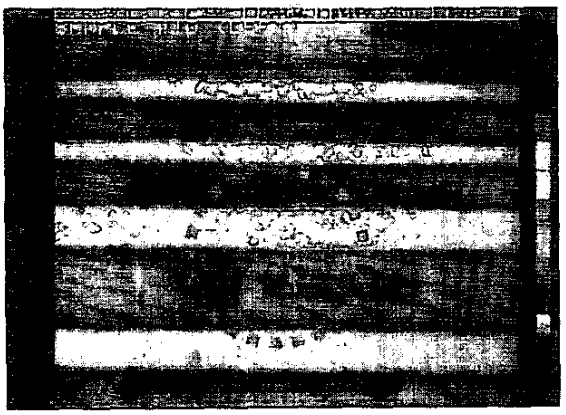


Fig.3 The power rail ESD clamp circuit for all VDD and VSS pads of the CMOS IC with multiple separated power pins.



(a)



(b)

Fig.4 (a) The internal damages caused by ESD stress across the separated power pins. (b) The zoomed-in picture on the left hot spot in (a).

With such big-size ESD protection devices in the I/O pads and power rails, the HBM ESD level of I/O pins can pass 5 kV. However, when performing the ESD test between the separated power pins, this IC product can pass only 0.5-kV but fail at 1-kV HBM ESD stress. The failure spots are found by EMMI (Photo-Emission Microscope) and pictured in Fig. 4.

By tracing the original chip layout and comparing to the circuit schematic, the hot spots are found on the PMOS of the input stage across interface between two circuit blocks with different VDD power supplies. Fig. 5 illustrates the equivalent circuit diagram across the interface circuit of the CMOS IC with separated power supplies, where the dashed lines with the arrows indicate the possible ESD current paths when an ESD stress is applied on VDD2 pin and the VSS1 pin relatively grounded. The ESD stress damages the gate oxide of PMOS Mp2 in Fig. 5, and induces a leakage current path between the power rails when VDD and VSS power supplies are applied on the circuits.

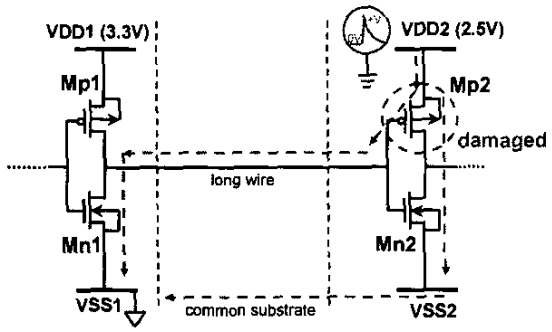


Fig.5 The equivalent circuit diagram to show ESD current paths in the CMOS IC with separated power supplies, when ESD stress is applying on VDD2 with VSS1 relatively grounded. The dashed lines with the arrows indicate the possible ESD current paths.

III. METHODS TO IMPROVE ESD ROBUSTNESS

To solve the internal damage problems caused by ESD stresses across different power pins, there were four approaches used and verified in this work to enhance the ESD immunity of this IC product.

A. NMOS clamps between interface and VSS metal line

For the cost consideration, the usage of photo mask changing on only metal layers is the first choice for this IC product. In the original layout, some dummy NMOS devices were placed in the chip, which can be connected to the interface circuit by changing metal mask layout. Besides, a 1-μm wide metal line used to connect the VSS1 and VSS2 is also achieved by changing the same metal mask layout. Fig. 6 shows the schematic diagram of the equivalent circuit after changing one metal mask. In Fig. 6, the first gate-grounded NMOS Mn1 is connected between VDD2 (2.5V) and the input node Y of inverter i2. The second gate-grounded NMOS Mn2 is connected between

VSS2 (0V) and the input node Y of inverter i2. Mn1 and Mn2 have the same channel width and channel length, which are 10 μm and 0.5 μm, respectively. The 1-μm wide metal line, Met1, is used to connect VSS2 (0V) and VSS1 (0V). Only one mask changing is used to achieve above layout modifications in this IC product for improving ESD robustness.

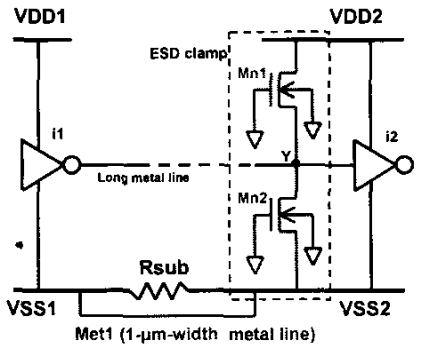


Fig.6 ESD clamp devices directly added to the interface circuit to solve the internal damage by changing one metal mask in the IC layout.

After the re-fabrication of this IC product, the ESD test is performed again, and the measurement results are listed in Table I. Focus Ion Beam (FIB) is also used to cut the metal connection to further investigate the performance of the extra ESD protection scheme shown in Fig. 6. After cutting the metal connection of Mn1 and Mn2 by FIB, the adding of only 1-μm wide metal line Met1 can improve the HBM ESD level to 2 kV. The most robust solution is combining Mn2 and Met1 that can improve the sustained HBM ESD level to 5.5 kV. However, the noise coupling issue between the VSS1 and VSS2 power rails makes this solution not acceptable for this IC application. The modification design with both Mn1+Mn2 and Met1 in Table I has an ESD level of only 3.5kV, because the Mn1 used in Fig. 6 is originally not drawn for ESD protection purpose. Only several contacts are used to contact the drain/source diffusion, which also have a minimum spacing between the drain/source contacts and the poly gate of Mn1. This causes a lower ESD level in this case, than that with the Mn2 and Met1. Comparing the measurement results and considering the practical application and noise issue, the advisable solution is only adding NMOS device Mn2 on the interface circuits between the input node Y and VSS2. Finally, the HBM ESD level of this IC product with multiple separated power supplies can be rescued to 3 kV.

Table I

ESD test results of the IC product with multiple separated power pins by using different solutions to improve ESD level.

Before Modification	Mn2	Met1	Mn1+Mn2	Mn2+Met1	Mn1+Mn2 +Met1
0.5kV	3kV	2kV	1kV	5.5kV	3.5kV

B. VSS ESD bus

ESD bus provides a common ESD current discharging path along the CMOS IC with separated power lines [14]. The ESD bus design was incorporated in the new version of another IC product with multiple separated power pins. This new IC product includes 12 separated power pairs to supply 12 internal circuit blocks connected by individual interface circuits, as those shown in Fig. 7. Each circuit block comprises the ESD protection scheme as those shown in Figs. 2 and 3. In this second IC product, the VSS2 power line of a PLL (Phase-Locked Loops) circuit does not connect to the common VSS ESD bus through the ESD conduction circuit because of limited layout area and noise coupling issue. The ESD conduction circuit comprises of two series diodes in a bi-directional connection [15], as shown in Fig. 8. The two series diodes can provide isolation of about 1-V noise between the VSS power lines and the common VSS ESD bus.

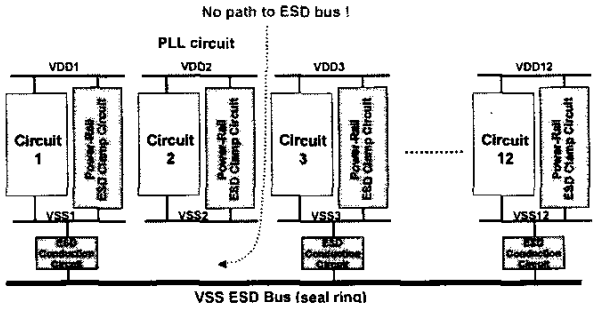


Fig.7 The second IC product includes 12 separated power pairs to supply 12 internal circuit blocks. The common VSS ESD bus is used to connect VSS power line of each circuit block through ESD conduction circuit except the PLL circuit block.

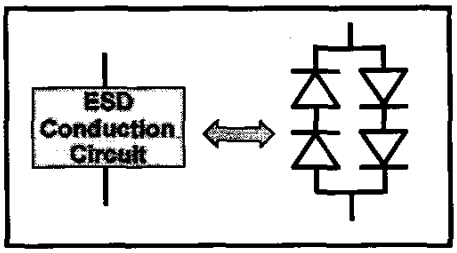


Fig.8 ESD conduction circuit comprises two series diodes with bi-directional connection [15].

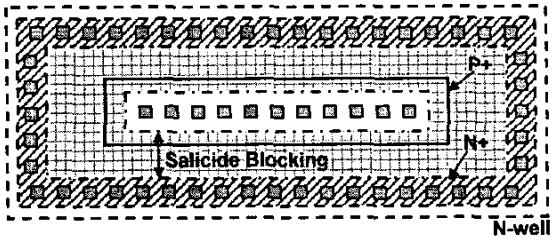


Fig.9 The device layout schematic of the diode used in ESD conduction circuit.

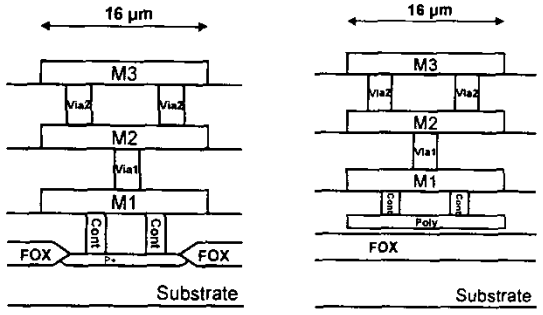


Fig.10 The cross-sectional views of (a) the seal ring suggested in the design rule, and (b) the modified seal ring used as the common VSS ESD bus in this new design.

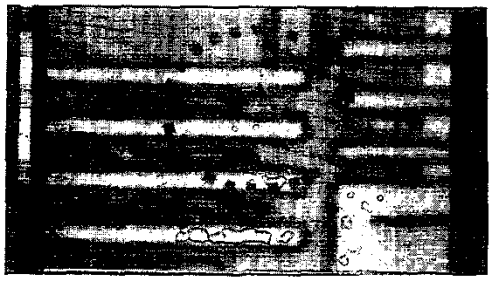


Fig.11 Internal damage caused by ESD stress on the second IC product, which is still located at the interface circuit between the PLL circuit block and the other circuit blocks with separated power supplies.

Between every two VSS power lines, there are equivalent four series diodes to provide a 2-V noise margin. Fig. 9 illustrates the device layout of the diode used in the ESD conduction circuit, which is realized by the P+ diffusion in an N-well. The salicide-blocking mask is used to block the silicide on the diode diffusion across the junction region.

The common VSS ESD bus, shown in Fig. 7, is constructed by the seal ring structure. Originally, the seal ring is used to prevent the mechanical stress on the die when wafer being sawed. Figs. 10(a) and 10(b) show the cross-sectional views of the design rule suggested seal ring and the modified seal ring used for the common VSS ESD bus in this second IC product, respectively. In Fig. 10(b), the metal contacts of the seal ring directly connect to the polysilicon layer instead of to the P+ diffusion in the substrate. Therefore, the noise in the substrate does not couple into the common VSS ESD bus, and not couple into the VSS power lines of the circuit blocks.

Accordingly, each pin of this second IC product can sustain a higher HBM ESD level to pass 5 kV, except the pins for the PLL circuit block, which can sustain the HBM ESD level of only 1 kV. Because the VSS2 of the PLL circuit block is not connected to the common VSS ESD bus through the ESD conduction circuit, the ESD stress across the different power pins easily causes the stress on the interface circuit between the PLL circuit block and the other circuit blocks. Again, the internal damage is still found in interface circuit between the PLL circuit block and the other circuit blocks with separated power supplies, and the EMMI failure picture is shown in Fig. 11.

C. High impendence interface circuits

Fig. 12 shows the equivalent circuit of interface circuit of the second IC product. The PLL circuit receives the output signal from a pre-buffer through a long metal wire, which is longer than 25 μm. The input circuit of the PLL circuit has an inverter inv1 and a transmission gate TG1. From the failure spot shown in Fig. 11, the damage location is found at the output PMOS (Mp). The equivalent circuit to show ESD current path is illustrated in Fig. 13. When the PLL circuit input circuit is modified without the transmission gate, as that shown in Fig. 14, the ESD level of this IC product can be increased from 1 kV to 2 kV. From the experimental data, the transmission gate of the interface circuit is sensitive to ESD events.

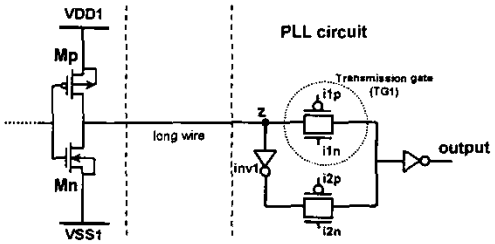


Fig.12 The interface circuit between the PLL circuit block and another circuit block of the second IC product.

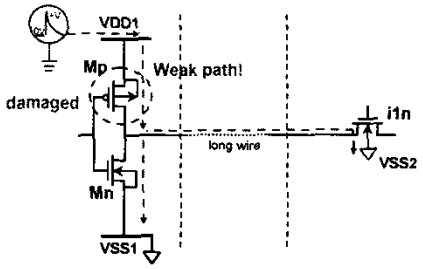


Fig.13 The equivalent circuit diagram to show the ESD current path flowing through the interface circuit, when an ESD event is happed on VDD1 with the VSS1 and VSS2 relatively grounded.

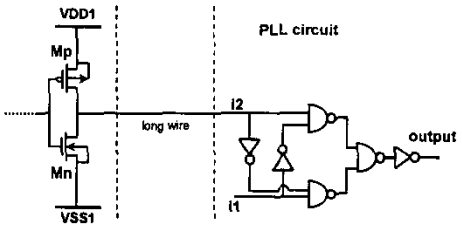


Fig.14 The modified input circuit of the PLL circuit block without using the transmission gate TG1 of Fig.12.

D. Final solution

The final version of whole-chip ESD protection design for this second IC product with 12 separated power pairs is shown in Fig. 15. The ESD conduction circuit is added to connect the VSS2 of PLL circuit block to the common VSS ESD bus line. For the consideration of noise coupling issue, only two series diodes in one direction are added in the ESD conduction circuit, where the anode of the series diodes is connected to the common VSS ESD bus line and the cathode of the series diodes is coupled to VSS2 of PLL circuit block. Thus, the noise generated by PLL circuit block would not couple to other circuits through the common VSS ESD bus line. Besides, the input buffer of PLL circuit block in the interface circuit is realized by the modified circuit, as that shown in Fig. 14 without the transmission gate TG1. The HBM ESD level of the final version of this second IC product with 12 separated power pairs and the whole-chip ESD protection design shown in Fig. 15 is improved from the original 1 kV to become > 5 kV, including the ESD stresses across the different power pins.

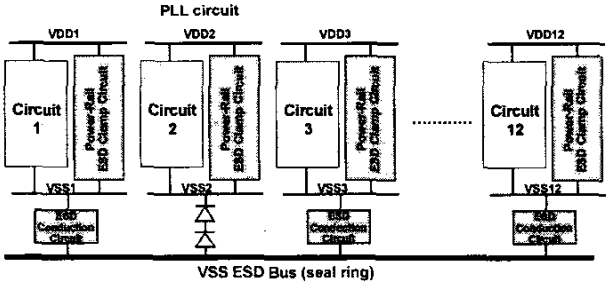


Fig.15 The final version of ESD protection scheme of the second IC product with 12 separated power pairs.

IV. CONCLUSION

A real case for ESD improvement on IC product with a lot of multiple separated power pairs has been studied in more details. The I/O pins can pass the 5-kV HBM ESD stress, but some internal damages had been found and located at the interface circuit between the circuit blocks with different power supplies. A final solution with the common ESD bus line, realized by the modified seal ring, is added to surround the whole chip with ESD conduction circuit connecting to every separated VSS power line. The two series diodes in bi-direction connection are used in the ESD conduction circuit to provide the ESD current discharging path between the separated VSS power lines and also to provide high enough noise margin between the separated VSS power lines. The overall HBM ESD level of this IC product with 12 separated power pairs has been successfully improved from the original 1 kV to become greater than 5 kV. This case provides an important witness on the effectiveness of ESD bus for effective whole-chip ESD protection design, which will become more useful in the sub-quarter-micron CMOS technologies with the much thinner gate oxide and the more separated mixed-voltage power supplies.

REFERENCES

[1] C. Jiang, E. Nowak, and M. Manley, "Process and design for ESD robustness in deep submicron CMOS technology," in *Proc. of IEEE Int. Reliability Physics Symp.*, 1996, pp. 233-236.

[2] M.-D. Ker, C.-Y. Wu, T. Cheng, and H.-H. Chang, "Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC," *IEEE Trans. on VLSI Systems*, vol.4, no.3, pp.307-321, Sept. 1996.

[3] J. Chen, A. Amerasekera, and C. Duvvury, "Design methodology and optimization of gate-driven NMOS ESD protection circuits in submicron CMOS processes," *IEEE Trans. on Electron Devices*, vol. 45, no. 12, pp. 2448-2456, 1998.

[4] M.-D. Ker, T.-Y. Chen, C.-Y. Wu, H. Tang, K.-C. Su, and S.-W. Sun, "Novel input ESD protection circuit with substrate-triggering technique in a 0.25-μm shallow-trench-isolation CMOS technology," in *Proc. of IEEE Int. Symp. on Circuits and Systems*, vol. 2, 1998, pp. 212-215.

[5] C. Duvvury, S. Ramaswamy, A. Amerasekera, and R. Cline, "Substrate pump NMOS for ESD protection applications," in *Proc. of EOS/ESD Symp.*, 2000, pp. 7-17.

[6] M.-D. Ker, T.-Y. Chen, and C.-Y. Wu, "ESD protection design in a 0.18-μm salicide CMOS technology by using substrate-triggered technique," in *Proc. of IEEE Int. Symp. on Circuits and Systems*, vol. 4, 2001, pp. 754-757.

[7] JEDEC Standard, No. 22-A114-B, June 2000.

[8] ESD Association Standard Test Method for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM), Component Level, ESD-STM-5.1, ESD Association, NY. USA, 1998.

[9] C. Duvvury, R. N. Rountree, and O. Adams, "Internal chip ESD phenomena beyond the protection circuit," *IEEE Trans. on Electron Devices*, vol. 35, pp. 2133-2139, Dec., 1988.

[10] C. C. Johnson, T. J. Maloney, and S. Qawami, "Two unusual HBM ESD failure mechanisms on a mature CMOS process," in *Proc. of EOS/ESD Symp.*, 1993, pp. 225-231.

[11] M.-D. Ker and T.-L. Yu, "ESD protection to overcome internal gate-oxide damage on digital-analog interface of mixed-mode CMOS IC's," *Microelectronics and Reliability*, vol. 36, 1996, pp.1727-1730.

[12] M. Chaine, S. Smith, and A. Bui, "Unique ESD failure mechanisms during negative to Vcc HBM tests," in *Proc. of EOS/ESD Symp.*, 1997, pp. 346-355.

[13] V. Puvvada and C. Duvvury, "A simulation study of HBM failure in an internal clock buffer and the design ussues for efficient power pin protection strategy," in *Proc. of EOS/ESD Symp.*, 1998, pp. 104-110.

[14] M.-D. Ker, H.-H. Chang, and T.-Y. Chen, "ESD buses for whole-chip ESD protection," in *Proc. of IEEE Int. Symp. on Circuits and Systems*, 1999, pp. 545-548.

[15] M.-D. Ker, "ESD protection circuit for mixed mode integrated circuits with separated power pins," US patent #6,075,686, Jun. 2000.