ESD Robustness of Low Temperature Poly-Si TFT's

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Abstract -- The optimum geometry design of Low Temperature Poly-Si (LTPS) TFT's for the best electrostatic discharge (ESD) robustness is investigated in this paper. By using the Transmission Line Pulsing (TLP) system, the secondary breakdown current (It2) of the top-gate LTPS TFT under different device dimensions was measured. It has been found that the It2 increases as channel length is shrunk, and the It2 per micron-meter channel width tremendously increases as the channel width decreases. Furthermore, it has been also found that the overlap region between drain and gate degrades the ESD robustness of the LTPS TFT's. The secondary breakdown current (It2) of LTPS TFT devices under substrate or gate bias is also investigated in this work.

1. Introduction

Recently, Low Temperature Poly-Si (LTPS) Thin-Film-Transistor (TFT) technology has been applied in integrated peripheral driver circuits of Active Matrix Liquid Crystal Display (AMLCD) for cost reduction and power consumption issue. System on Panel (SOP), combined memory and controller with driver circuits on a glass substrate, will be the most suitable application for LTPS TFT's in the near future [1]. When the time of SOP is approaching, the ESD reliability issue of TFT-LCD system is not only an oncoming problem but also an extremely worth-concern problem. In the silicon base CMOS technologies, several advanced whole-chip ESD protection schemes have been proposed [2]-[4]. However, still now, neither research report nor related information about the ESD reliability issue of LTPS circuits has been mentioned. In order to overcome this troublesome problem, the ESD characteristics of LTPS devices should be investigated first. According to the investigated results, the optimum geometry design of LTPS devices for LTPS circuits can be found.

In this paper, the ESD robustness of LTPS devices with different geometry parameters have been characterized by measuring their It2, which represents the ESD robustness of a device. In addition to optimum geometry design of LTPS TFT device, the gate-driven and substrate-triggered effects on the LTPS TFT device is also monitored in this paper for effective ESD protection design.

2. Device Structure and Fabrication

Fig. 1 shows the schematic structure of the investigated top-gate LTPS TFT device that was fabricated on the glass with deposition of 300nm TEOS oxide by PECVD. A 50nm thick PECVD α-Si film was then deposited. After definition of the n-type source/drain region, α-Si film was crystallized by excimer-laser. Then the polysilicon island was defined by dry etching process. A 100nm TEOS oxide was deposited on the island as gate insulator and followed by gate metal deposition and patterning. A 400nm TEOS oxide was deposited as inter-layer, and the contact holes were patterned. A Cr/Al double-layer film was deposited and patterned as source/drain metal. Finally, the LTPS TFT's were passivated by hydrogenation techniques to reduce interface traps. The detail process flow

for fabrication such TFT device has been reported in [5].

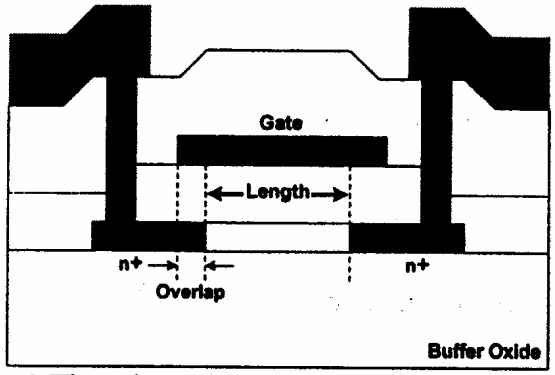


Fig. 1 The schematic structure of the investigated top-gate LTPS TFT device.

3. Measurement Results

The It2 of the top-gate LTPS TFT's were measured by using Transmission Line Pulsing (TLP) system [6]-[7] with a pulse width of 100ns. The human-body-model [8] ESD robustness of CMOS IC's has been often estimated by $V_{ESD} \approx It2 \times 1.5k\Omega$ [9]. So, the device with a larger It2 can sustain a higher ESD stress. There were two failure criteria for the TLP measurement on such LTPS TFT's: (1) the leakage current of the LTPS TFT biased at Vds=5V and Vgs=0V increases three order after TLP stress, and (2) the TLP I-V curve shows obviously a negative resistance region (due to secondary breakdown). Once one of these two failure criteria happens, the top-gate LTPS TFT will be judged as failure.

The measured TLP I-V curves of the top-gate LTPS TFT's with different channel lengths are shown in Fig. 2. As shown in Fig. 2, the top-gate LTPS TFT (W=50μm) with a channel length (L) of 6μm has a It2 of 137mA. When its channel length is increased to 20μm, the TLP-measured It2 is degraded to only 75mA. The top-gate LTPS TFT with shorter channel length will have higher ESD robustness. Fig. 3 shows the measured TLP I-V curves of the top-gate LTPS TFT's with or without overlap region between drain and gate. The turn-on resistance of the overlap device (overlap=1.0μm) is similar to that of non-overlap device (overlap=0μm) under the same W/L. The top-gate LTPS TFT with a device dimension of W/L=50μm/6μm has a It2 of 137mA if the overlap spacing is 0μm. But, its It2 degrades to 113mA, when the TFT device has a drain-gate overlap region of 1.0μm.

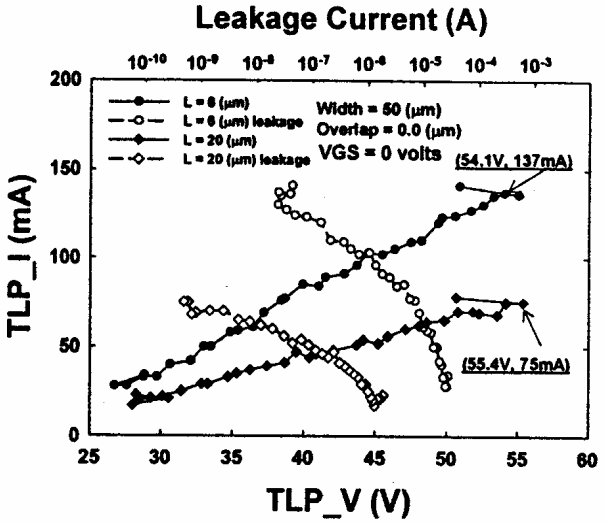


Fig. 2 The measured TLP I-V curves of the LTPS TFT's with different channel lengths.

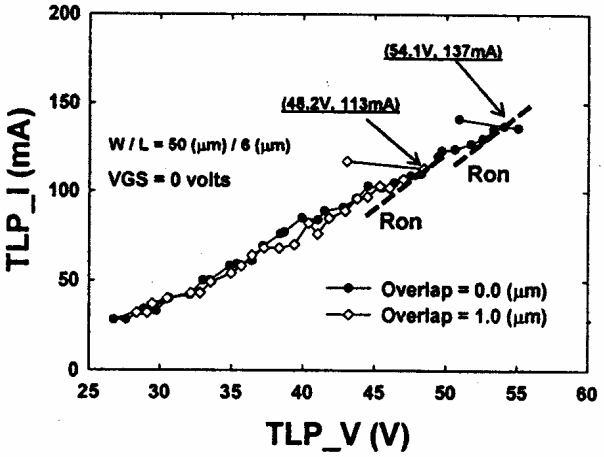


Fig. 3 the measured TLP I-V curves of the top-gate LTPS TFT's with or without overlap region between drain and gate.

Fig. 4 compares the relations between It2 value and channel length of the LTPS TFT's with or without overlap region between drain and gate. It is found that the It2 value increases abruptly in short channel region (for L<10μm) and keeps nearly constant in long channel region (for L>10μm). This is due to the lateral BJT effect (kink effect) is more obvious in the short channel top-gate LTPS TFT. Fig. 4 also shows the relations between turn-on resistance and channel length of the LTPS TFT's with or without overlap region between drain and gate. The turn-on resistance of short channel top-gate LTPS TFT is smaller than that of long channel

one. This is due to the low base resistance of lateral BJT. Moreover, the overlap devices show a weaker ESD robustness than non-overlap devices due to the high electric field at drain side.

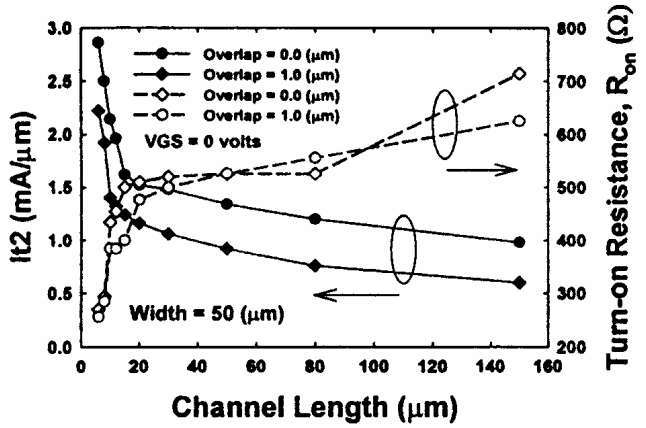


Fig. 4 The relations between It2 value and channel length of the LTPS TFT's with or without overlap region between drain and gate.

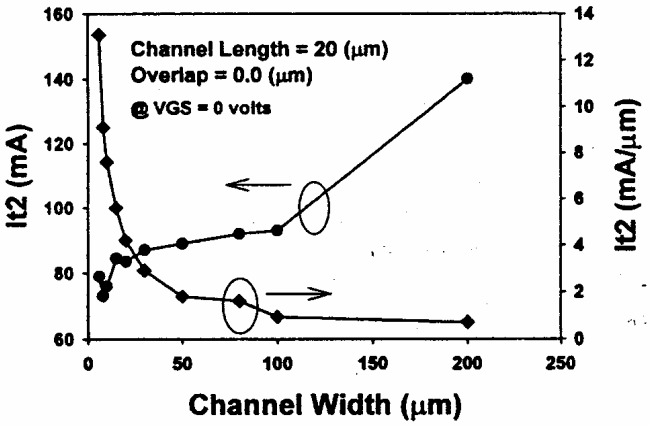
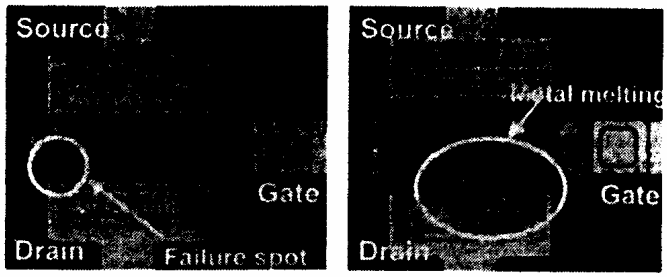


Fig. 5 The relations between It2 and channel width of the LTPS TFT's.

The relations between It2 and channel width of the LTPS TFT's are shown in Fig. 5. Although the It2 (mA) value of the top-gate LTPS TFT increases with channel width, the It2 per micron-meter channel width (mA/μm) of LTPS TFT abruptly increases in narrow width region. The LTPS TFT drawn in the single-finger style has seriously non-uniformly turn-on effect. To effectively increase ESD robustness of LTPS TFT device, the multiple-finger layout style of CMOS output transistors is recommended to realize such LTPS TFT device of a large device dimension. The pictures of failure spots on the LTPS TFT devices after TLP stress are shown in Fig. 6. There is 95% of the top-gate LTPS TFT's after TLP stress to fail at near the corner after TLP stress, as that shown in Fig. 6(a). The other 5% of the top-gate LTPS TFT's after TLP stress failed with metal melting at the drain side, as that shown in Fig. 6(b).



(a) (b)

Fig. 6 The pictures of failure spots after TLP stress. (a) 95% of the devices fail at near the corner. (b) 5% of the devices fail with metal melting at the drain side.

4. Gate-Driven and Substrate-Triggered Effect on LTPS TFT's

In CMOS IC's, the substrate-triggered or gate-driven techniques had been used to improve ESD robustness [10]. To further analysis the ESD robustness of the LTPS TFT devices under gate-driven and substrate-triggered design, the LTPS TFT device with different gate or substrate biases is also measured by TLP system to investigate its It2. The TLP-measured I-V curves of the LTPS TFT devices under different gate (substrate) biases are shown in Fig. 7 (Fig. 9). The TFT device used in gate-bias (substrate-bias) measurement has a device dimension of W/L= 75μm/20μm (90μm/25μm) and a drain-gate overlap of 1.0μm. The dependence of It2 of TFT device on the different gate (substrate) bias voltage is summarized in Fig. 8 (Fig. 10).

In Fig. 7 and Fig. 8, TFT device with increase of gate bias, the It2 increases initially due to the formation of extra current path (surface channel), but it falls in high gate bias due to hot-carriers injection and current over-crowding in surface channel. The turn-on resistance of LTPS TFT also identifies the turn-on mechanism under different gate biases. When ESD current increases to the damage level under a larger gate bias (Vgs>7V), not only the channel region but also the gate electrode were burned out, as the inserted picture shown in Fig. 7.

In Fig. 9 and Fig. 10, the It2 of LTPS TFT increases slightly when the substrate bias has a low voltage level (<5V). When substrate bias is above 5V, the It2 value of LTPS will degrade and the turn-on resistance increase. This result is quite different to that of bulk CMOS device [10]. The mechanism of this abnormal phenomenon will be further studied. From the inserted failure picture in Fig. 9, it shows that the damage point under high substrate bias is located only around the channel region but not on the gate electrode.

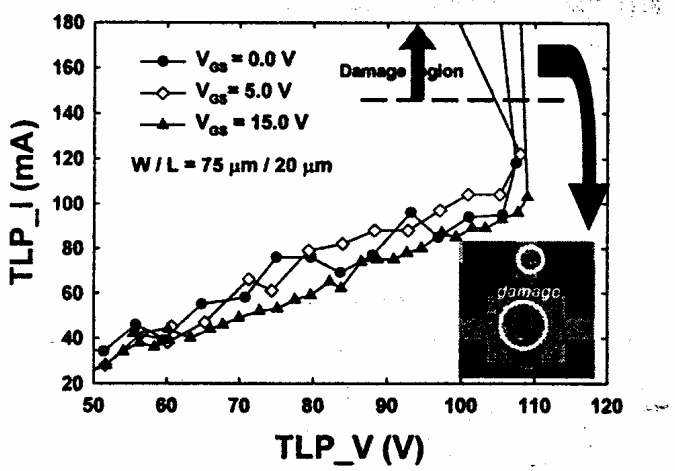


Fig. 7 The TLP-measured I-V curves of the top-gate LTPS TFT's under different gate biases.

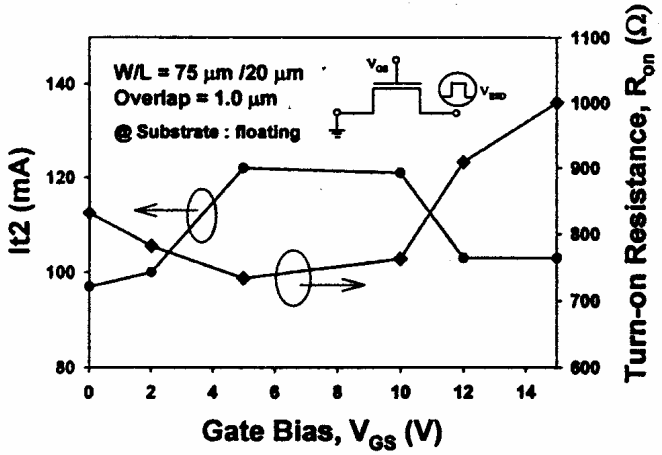


Fig. 8 The dependence of It2 and turn-on resistance of the TFT device on the different gate biases.

5. Conclusion

ESD robustness of the top-gate LTPS TFT's with different geometry parameters has been investigated in details. The experimental results show that the non-overlap LTPS TFT with a shorter channel length has better ESD robustness. Moreover, the finger length of LTPS TFT should be drawn shorter to prevent the non-uniform turn-on effect.

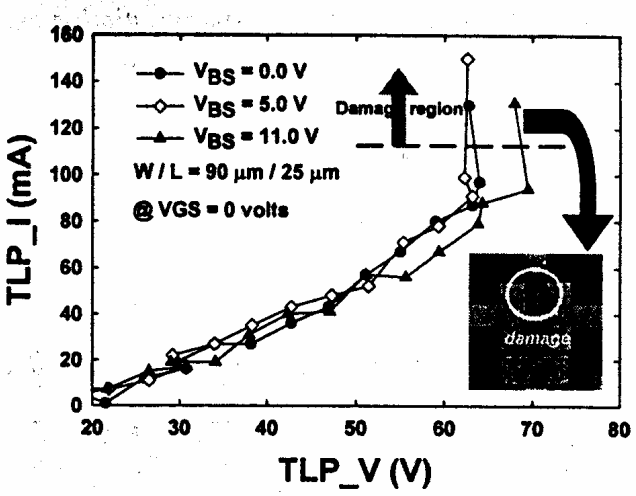


Fig. 9 The TLP-measured I-V curves of the top-gate LTPS TFT's under different substrate biases.

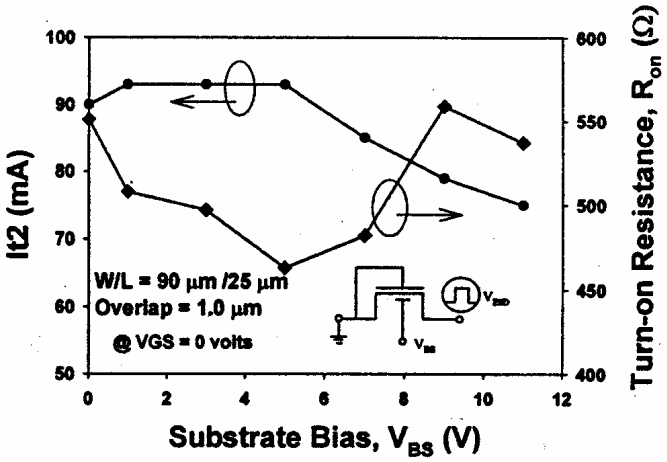


Fig. 10 The dependence of It2 and turn-on resistance of the TFT device on the different substrate biases.

6. References

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