Novel ESD Implantation for Sub-Quarter-Micron CMOS Technology with Enhanced Machine-Model ESD Robustness

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Abstract -- A novel ESD implantation method is proposed to significantly improve machine-model (MM) electrostatic discharge (ESD) robustness of CMOS integrated circuits in sub-quarter-micron CMOS processes. By using this method, the ESD current is discharged far away from the surface channel of NMOS, therefore the NMOS can sustain a much higher ESD level, especially under the machine-model ESD stress. The MM ESD robustness of the gate-grounded NMOS (ggNMOS) with a device dimension of W/L= 300μm/0.5μm has been successfully improved from the original 450V to become 675V in a 0.25-μm CMOS process.

1. Introduction

Component-level ESD stresses on IC products had been classified as three models [1]: the human-body model (HBM) [2]-[4], the machine model (MM) [5]-[6], and the charged device model (CDM) [7]-[8]. The ESD voltage ratio between the HBM and MM ESD robustness of CMOS IC products were around ~10 in the submicron (1.0 ~ 0.5μm) CMOS processes [9]-[10]. Typically, a CMOS IC product, which has a HBM ESD robustness of 2kV, can sustain a MM ESD stress of 200V. However, this ratio has approached to about 15 ~ 20 in the sub-quarter-micron CMOS processes. The CMOS IC fabricated by the sub-quarter-micron CMOS processes can be still designed to have a high HBM robustness, but it becomes more challenging to have a high enough MM ESD level.

In the past, most of ESD design efforts were focused to improve HBM ESD robustness of IC products. With a high HBM ESD robustness, the IC products also had a high enough MM ESD level. However, the MM ESD robustness of IC products has been found to degrade much worse than its HBM ESD robustness in the sub-quarter-micron CMOS processes. How to effectively improve MM ESD robustness of IC products has become a challenge in the sub-quarter-micron CMOS processes. But, from the past literature, it is seldom to see the design or method for improving MM ESD robustness.

In this paper, a novel ESD implantation method is therefore proposed to improve HBM and MM ESD levels of CMOS ICs. Especially, this method can significantly increase ESD level of NMOS under the MM ESD zapping. The experimental result in this paper is the first report in the literature to significantly increase MM ESD robustness in CMOS technology by a general process-compatible ESD implantation method.

2. HBM and MM ESD Current Waveforms

The real ESD current discharging waveforms of HBM and MM ESD stresses through the gate-grounded NMOS (ggNMOS) are measured and compared to find the difference. The experimental setup to measure the current waveforms during ESD test is illustrated in Fig. 1, where the digital oscilloscope with current probe is used to measure the ESD transient currents in time domain. The actual ESD current waveforms flowing through the ggNMOS with a device dimension of W/L=300μm/0.5μm under 4-kV HBM and 400-V MM ESD stresses are measured and shown in Fig. 2 and Fig. 3, respectively.

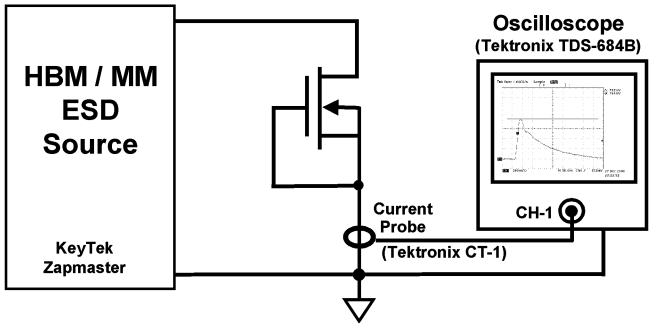

Fig. 1 The experimental setup to measure the ESD transient current waveforms during ESD test.

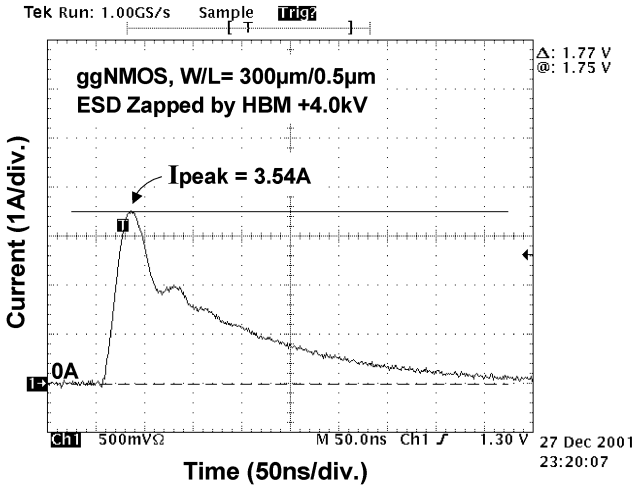

Fig. 2 The measured ESD current discharging waveform through the ggNMOS, which is zapped by 4-kV HBM ESD voltage.

The current peak of 4-kV HBM ESD stress in Fig. 2 is 3.54A, whereas that of 400-V MM ESD stress in Fig. 3 is as high as 4.94A. As comparing these two ESD current waveforms, the MM ESD stress has a much higher ESD current peak within a shorter current pulse width. This implies that the MM ESD events generate more heat in a shorter time period to burn out the device, and therefore cause a much lower ESD robustness. MM ESD protection has become more difficult than HBM in sub-quarter-micron CMOS processes.

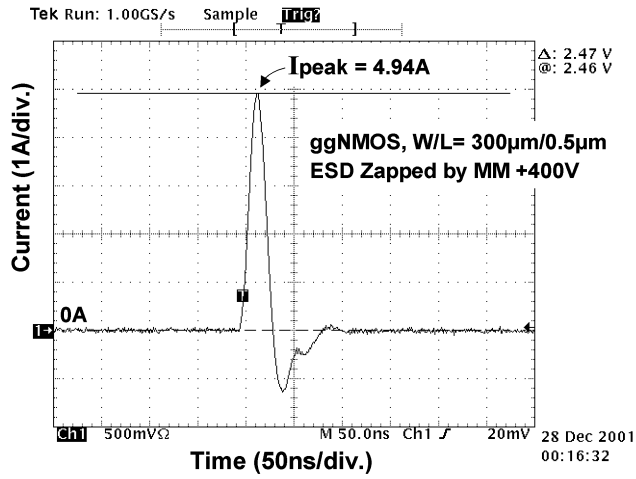

Fig. 3 The measured ESD current discharging waveform through the ggNMOS, which is zapped by 400-V MM ESD voltage.

3. ESD Implantation Methods

In submicron CMOS technology, the NMOS fabricated with LDD structure to overcome the hot-carrier issue, as shown in Fig. 4, often leads to a lower ESD robustness. To improve ESD robustness, some CMOS processes provide one extra ESD-implantation mask to modify the NMOS devices of I/O circuits without the LDD peak structure [11]. One of the traditional ESD implantation methods, with n-type impurity for improving ESD robustness of NMOS, is shown in Fig. 5. The N_ESD impurity in sub-quarter-micron CMOS process often has a lower concentration than that of N+ drain/source diffusion to overcome the hot-carrier issue. A comparison on the effectiveness of improveing ESD robustness among the traditional ESD implantation methods had been experimentally investigated in [11].

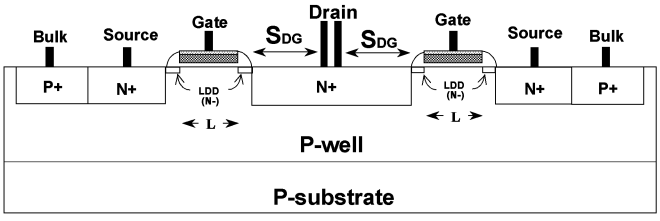

Fig. 4 The normal NMOS device with lightly-doped-drain (LDD) structure to overcome the hot-carrier issue.

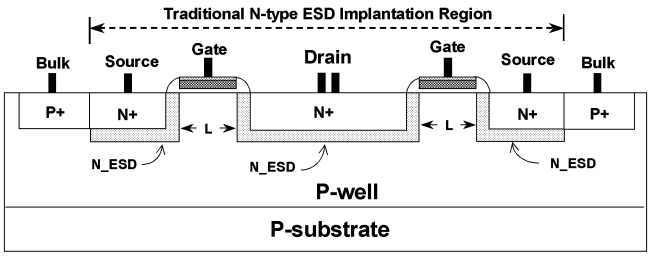

Fig. 5 The traditional ESD implantation method with n-type impurity for improving ESD robustness of NMOS.

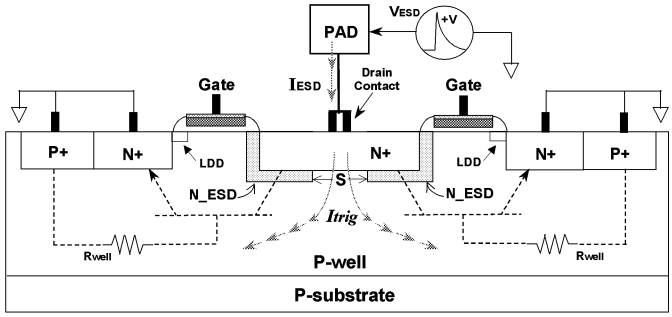

Fig. 6 The new proposed ESD implantation method to significantly improve machine-model ESD robustness of NMOS. The spacing "S" is the important layout parameter to be investigated.

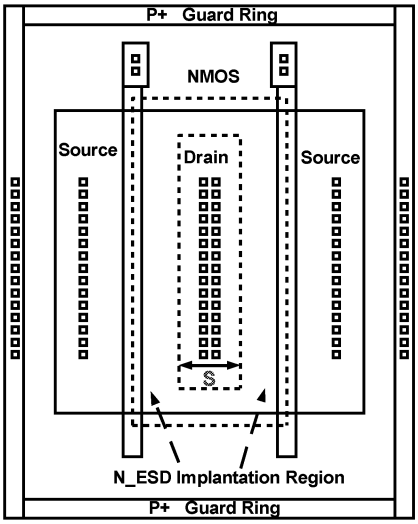

Fig. 7 The corresponding layout top view of the NMOS with the new proposed ESD implantation method. The layout parameter "S" is also indicated in this figure.

To significantly improve MM ESD robustness of NMOS in I/O circuits, the novel ESD implantation method is proposed in Fig. 6, where the spacing "S" is the important layout parameter to be investigated. In Fig. 6, the ESD implantation region covers the whole drain region of NMOS device, but except the region around the drain contact. The corresponding layout top view of the NMOS with the proposed ESD implantation method is drawn in Fig. 7, where the layout parameter "S" is also indicated. This ESD

implantation region has a doping concentration (N_ESD) lighter than that of the original (N+) drain diffusion. Therefore, the junction covered by the proposed ESD implantation method has an increased junction breakdown voltage. But, the region without covering by this ESD implantation has the original junction breakdown voltage.

When a positive ESD voltage is applied to the pad with the VSS relatively grounded. The drain of NMOS is stressed by the ESD voltage and therefore breaks down to clamp the overstress voltage on the pad. The region, which is not covered by the N_ESD implantation, has a lower junction breakdown voltage, therefore the ESD current is first discharged through this region to generate the substrate current (*Itrig*, indicated in Fig. 6) to quickly trigger on the lateral n-p-n BJT in the NMOS device. The ESD current is finally discharged through the parasitic lateral n-p-n BJT in the NMOS, where such ESD current path is far away from the weakest surface channel of the NMOS. So, the MM ESD level of the NMOS can be effectively improved.

4. Experimental Results

To investigate the effectiveness of the new proposed ESD implantation method, some test chips drawn with different layout spacing "S" had been fabricated in a 0.25-μm CMOS process with shallow trend isolation. The new proposed N_ESD implantation (shown in Fig. 6) on the test devices is directly realized by using the traditional ESD implantation method with light n-type impurity, which had been an optional process step in general CMOS technologies provided by the most foundries. But, the region to be implanted with the light n-type impurity is drawn in the layout of test devices with different spacing "S". To simplify investigate the dependence of the ESD-implanted region (adjusted by the spacing "S" in layout) on ESD robustness of ggNMOS devices, the layout spacing of the drain diffusion between two poly gates is fixed at 5.7 μm for all devices in the experimental test chips. The fabricated devices with different spacing "S" are measured by the curve tracer to investigate DC I-V charactertics, by the transmission line pulsing (TLP) system [12]-[14] to investigate secondary breakdown current (It2), and by the *ZapMaster* ESD simulator to investigate HBM and MM ESD robustness. The experimental results are shown in the following subsections.

4.1 DC I-V Charactertics

The measured DC I-V curves of the ggNMOS devices with different layout spacing "S" are compared in Fig. 8. The trigger (switching) voltages of the ggNMOS devices with S= 0 or 2.3 μm are 9.8V, but that of the ggNMOS device with S=4.9 μm is 9.72V. The holding points of the ggNMOS devices with the layout spacing "S" of 0, 2.3, and 4.9 μm have no obvious variation. The DC behaviors of those devices are almost the same, as those shown in Fig. 8. The new proposed ESD implantation method does not modify the channel region of the NMOS devices. When such NMOS devices are used in the output buffer as the pull-down devices, their I-V curves are similar to that of the normal NMOS device in the same CMOS process. This result provides the same device I-V behavior on the ESD-implanted NMOS, as that of normal NMOS, for working as the functional output devices in CMOS ICs.

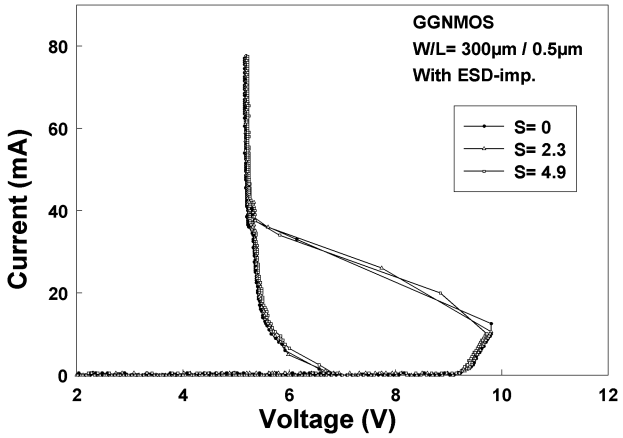

Fig. 8 The measured DC I-V curves of ggNMOS with the new proposed ESD implantation under different layout spacing "S".

4.2 TLP I-V Charactertics

The TLP-measured I-V curves of a ggNMOS with W/L= 300μm/0.5μm, fabricated in a 0.25-μm CMOS process with the new proposed ESD implantation method, are shown in Fig. 9 under the different layout spacing "S". The TLP system used in this measurement has been set up with a pulse width of 100ns and a rise time of 10ns [14]. The dependence of the second breakdown current (It2) on the layout spacing "S" of the ggNMOS fabricated with the new proposed ESD implantation method is shown in Fig. 10. The It2 of the ggNMOS with S=0μm is only 2.90A, when it has a device dimension of W/L=300μm/0.5μm. But, its It2 can be significantly improved up to 3.64A, when the spacing S is increased to 4.9μm. Under the same layout area of the ggNMOS with W/L=300μm/0.5μm (the drain diffusion between two poly gates is fixed at 5.7 μm), the It2 can be improved 25.5% by using the new proposed ESD implantation method.

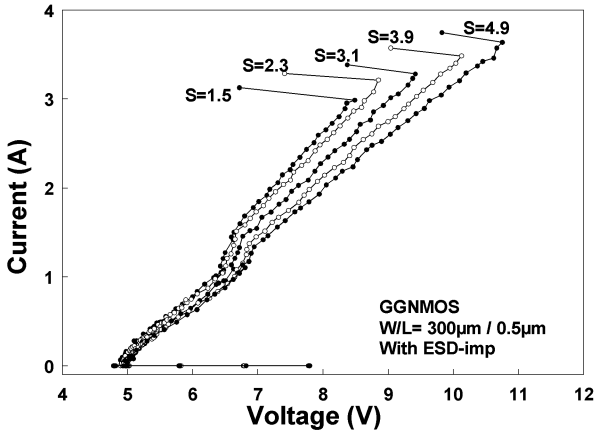

Fig. 9 The TLP-measured I-V curves of ggNMOS with the new proposed ESD implantation under different layout spacing "S".

The TLP-measured I-V curves of ESD-implanted ggNMOS under different channel width but a fixed S=1.5μm are shown in Fig. 11. The It2 of such ESD-implanted ggNMOS is linearly increased when its channel width is increased. This implies that the ESD-implanted ggNMOS with multiple fingers in layout will have good turn-on uniformity during ESD stress.

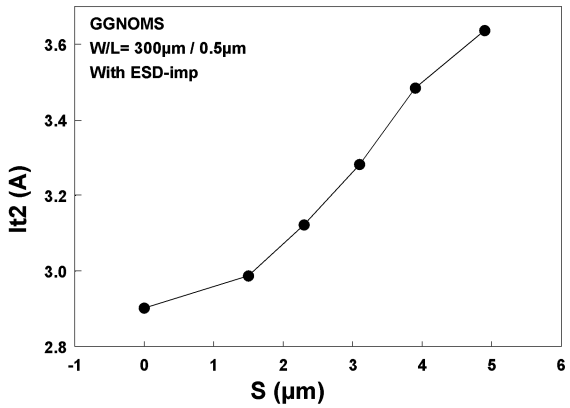

Fig. 10 The dependence of the second breakdown current (It2) on the layout spacing "S" of the ggNMOS fabricated with the new proposed ESD implantation method.

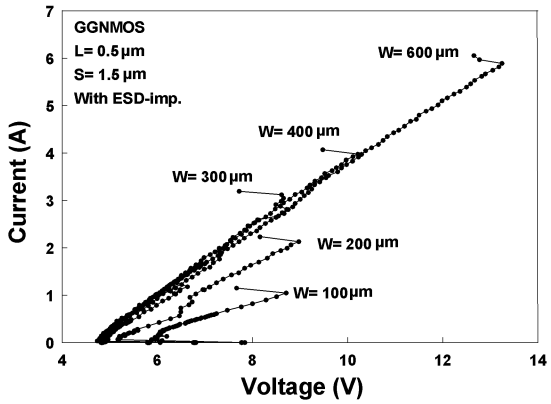

Fig. 11 The TLP-measured I-V curves of ggNMOS with the new proposed ESD implantation under different channel width but a fixed S=1.5μm.

4.3 ESD Test Results

The ESD-implanted ggNMOS devices are also verified by the ESD tester under both HBM and MM ESD stresses. The ESD failure threshold (ESD level) is defined at the minimum voltage level of ESD stress that causes the ggNMOS having a leakage current greater than 1μA under the voltage bias of 3.3V. The dependences of HBM and MM ESD levels on the channel width of ggNMOS with S= 0 or 1.5 μm are shown in Fig. 12. The HBM and MM ESD levels are linearly increased, when the channel width of ggNMOS is increased. However, as comparing the lines between the HBM and MM ESD levels under different layout spacing S, the MM ESD level has an obvious improvement if the ggNMOS is drawn with a wider S. The dependences of the HBM and MM ESD robustness on the layout spacing "S" of ESD-implanted ggNMOS, under a fixed device dimension of W/L=300μm/0.5μm, are shown in Fig. 13. With the same layout area and device dimension in the ESD-implanted ggNMOS, the wider spacing "S" can lead to higher HBM and MM ESD levels. The HBM ESD level of this ESD-implanted ggNMOS with a fixed device dimension of W/L=300μm/0.5μm is improved from the original 5.75kV (with S=0) to become 6.75kV (with S=4.9μm). The MM ESD level of this ESD-implanted ggNMOS, with W/L= 300μm/0.5μm, is also improved from the original 450V (with S=0) to become 675V (with S=4.9μm).

The ratio between the HBM and MM ESD levels (and the MM/It2 ratio) on the layout spacing "S" of the ESD-implanted ggNMOS with W/L=300μm/0.5μm are further compared in Fig. 14. The HBM/MM ESD level ratio of the ESD-implanted ggNMOS with W/L=300μm/0.5μm has a value of 12.67 when the spacing S=0μm. As seen in Fig. 14, this HBM/MM ESD level ratio can be decreased to 9.93, when the spacing "S" is enlarged to 4.9μm in the ESD-implanted ggNMOS. From the experimental results, the new proposed ESD implantation method can significantly increase the MM ESD level of the NMOS devices in sub-quarter-micron CMOS processes. The HBM/MM ESD level ratio can be successfully kept at ~10 by this novel ESD implantation method.

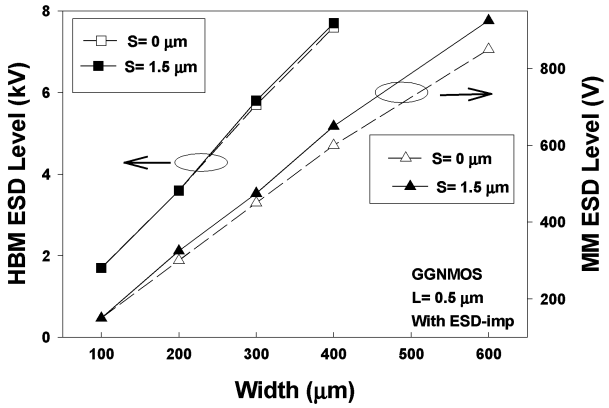

Fig. 12 The dependence of HBM and MM ESD robustness on the channel width of ESD-implanted ggNMOS with S= 0 or 1.5μm.

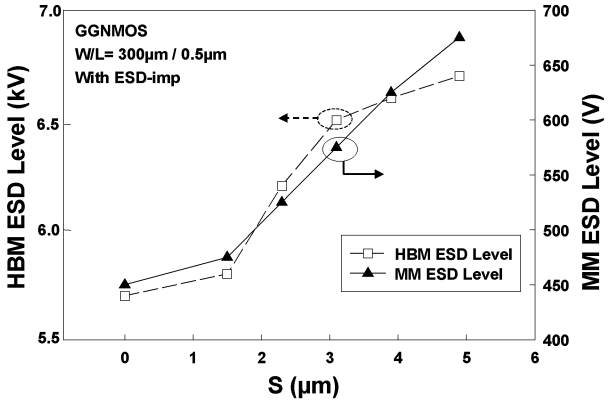

Fig. 13 The dependence of the HBM and MM ESD robustness on the layout spacing "S" of ggNMOS fabricated with the new proposed ESD implantation method.

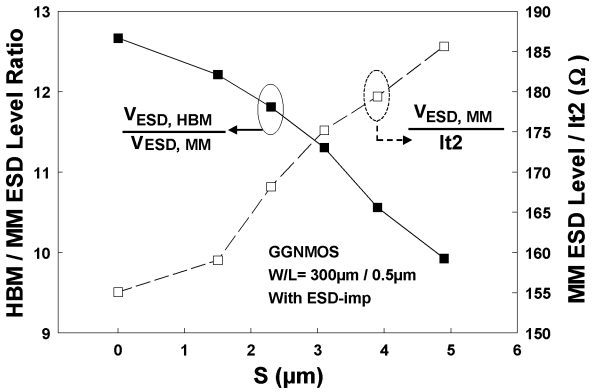

Fig. 14 The dependences of the HBM/MM ratio and the MM/It2 ratio on the layout spacing "S" of ggNMOS fabricated with the new proposed ESD implantation method.

5. Conclusion

A novel ESD implantation method proposed to significantly improve machine-model ESD robustness of NMOS devices has been practically verified in a 0.25-μm CMOS process. From the experimental results, this ESD implantation method can successfully increase the MM (HBM) ESD level of ggNMOS, with a fixed device dimension of W/L=300μm/0.5μm and the same silicon area, from the original 450V (5.75kV) to become 675V (6.75kV) when the layout spacing S is increased from 0 to 4.9 μm. The HBM/MM ESD level ratio can be successfully kept at ~10 by this ESD implantation method. The proposed ESD implantation method, which is process compatible to general CMOS processes with an additional non-critical mask layer of light-doping ESD implantation, is very suitable for using in the IC products to improve their machine-model ESD robustness.

The future work of this study is to investigate the effectiveness of the new proposed ESD implantation method on the NMOS devices with different doping concentrations of the N_ESD implantation in CMOS processes. Another future work is to verify the effectiveness of the new proposed ESD implantation method on the NMOS devices in stacked configuration [15]-[16], which had been widely used in the mixed-voltage interface I/O circuits [17].

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