Anomalous Latchup Failure Induced by On-Chip ESD Protection Circuit in a High-Voltage CMOS IC Product

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Abstract

Latchup failure induced by ESD protection circuits occurred in a high-voltage IC product. Latchup occurred anomalously at only several output pins. All output pins have nearly identical layouts except the side output pin has a N-well resistor of RC gate-coupled PMOS beside. It was later found this N-well resistor is the main cause of inducing latchup.

1. Introduction

Technological advances in ULSI and high voltage devices have made possible the developments of high-voltage integrated circuits (HVICs). In applications such as display drivers, the use of HVIC can significantly reduce system size. However, with more lightly doped drain junction in order to sustain high enough breakdown voltage, accompanied with higher operating voltage (and resultant high power dissipation), the electrical overstress (EOS) is becoming more severe in high voltage devices and poses serious threat to device reliability, such as electrostatic discharge (ESD) and latchup. In view of latchup, if the holding voltages of parasitic SCR are higher than power supply voltage (Vdd), the circuit is latchup-free [3]. It would be particularly adverse to high voltage devices since the high operating voltage would now make it more difficult to achieve latchup-free condition.

In this paper, we present an anomalous latchup failure phenomenon of a high voltage IC. Of all layout-similar output pins, only 3 pins showed latchup failure under JEDEC Standard 78 test [1]. Latchup of the first two pins (pin#22 and 24) were induced by the latchup of the third pin (pin#26), as verified in our experiments. Large power line current (Idd) existed when triggering the third pin and led to latchup. The large power line current was due to negative-gate-biasing of high-voltage PMOSs (HVPMOSs) of ESD power clamp circuits by injected electron flow building up voltage drop across the N-well resistor during the latchup test. Blocking this e^- flow by FIB (focused ion beam) cutting experiments on the IC resolved the large power line currents and latchup of pin#26 at the same time.

2. Latchup Phenomena and ESD Protection Circuits of the High-Voltage IC Product

Latchup is a state in which low-impedance path that results from an overstress that triggers a parasitic pnpn-silicon controlled rectifier (SCR) structure and persists even after removal of the triggering condition [2]. Since the power supply has then a low shunt impedance to ground at latchup, large power line current (Idd) will exist between Vdd and ground (Gnd). If this current is not otherwise limited, irreversible damage would occur to the circuit; even if the current is limited such that no irreversible damage occurs, it is possible that the low impedance state can cause circuit's malfunction.

This product is a high voltage IC and the operating voltage is 10V. It utilizes gate-triggered high-voltage PMOSs (HVPMOSs) as Vdd-to-Vss ESD power clamp circuit for whole-chip ESD protection [4]. As general ESD and latchup specifications for IC products, 2kV HBM in ESD level and +/- 100mA trigger level in JEDEC Standard 78 Test are requested to pass as the quality assurance's criteria. The product passed ESD test and had an ESD level of 3kV, however it failed at -100mA in negative trigger for latchup test. The failed pins were pin#22, 24, and 26, respectively. However, these –100mA-failed samples passed subsequent function test. The layout schema of the product is shown in Fig. 1(a). It should be noted that since all of them are HV output pins, their layout are almost identical and composed of the same cells, as shown in the chip floor plan in Fig. 1(b).

During ESD qualification process, four ESD zap modes are tested [4], with positive and negative Vdd-to-Vss ESD stress in addition. In the two Vdd- to-Vss zap tests, internal circuits are vulnerable to ESD damage if there is no ESD power clamp circuit between Vdd and Vss. Therefore, in order to clamp the ESD voltage across Vdd and Vss power lines efficiently before internal circuits are damaged by ESD overvoltage, an ESD clamp circuit is needed between Vdd and Vss. In this product, shortened gates to Vdd through a series resistor, HVPMOSs with their drains connected to Vss and sources connected to Vdd are used as an ESD power clamp circuit and named here as GRPMOSs, shown in Fig. 1(c). The GRPMOSs utilizes the parasitic capacitor Cgd of HVPMOSs and a N-well (NW) resistor to comprise an ESD-transient detection circuit. The time constant is designed in the order of sub-μs. Therefore, the resistance value of this NW resistor is quite large, in tens of kohms, because of small

Cgd value. In negative Vdd-to-Vss ESD zap, the ESD current is conducted by the forward bias of N-well/P^+ parasitic diode. In positive Vdd-to-Vss ESD stressing, due to the sub-μs-order time constant, the gates of HVPMOSs remain low. Therefore, HVPMOSs are turned on to vent ESD current. At normal circuit operation, the HVPMOSs remain off because, under normal power-on condition, the rise time of power-on voltage waveform is in ms-order, and the gate voltage of HVPMOSs can follow Vdd voltage in time and keep HVPMOSs off.

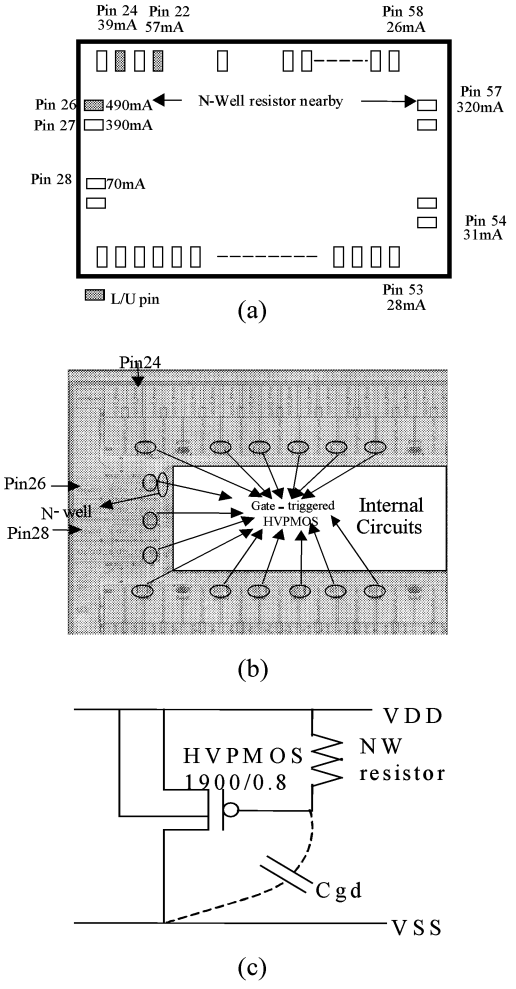


Fig. 1 (a) Whole chip layout schema. Pins in gray are latched pins. Also shown are power pin currents during trigger in subsequent wafer-level latchup tests. (b) Chip floor plan. Output pins are consisted of same cells. (c) Circuit schematic of GRPMOS. The labeled width is the sum of 19 distributed HVPMOSs in parallel.

3. Failure Analysis and Experimental Procedures

3.1. Resolving the Latchup Issue of Pin #22 and 24

For the latchup of pin#22 and 24, reviewing the layout reveals these two output pins to be identical to others on the top of the chip. And since latchup is highly layout dependent, there is no obvious root cause to the latchup of these two pins. For simple differentiation, we performed the test procedure as follows. Originally pin#26 was first latchup tested, followed by pin#24 and pin#22. By skipping pin#26 test and testing pin#22 and 24 first, the outcome was quite surprising that no latchup at pin#22 and 24 was found. As a comparison, the testing sequence was set to its original condition and pin#26 latched this time with subsequent pin#24 and 22 latchup. This reveals that the latchup event of pin#26 results in the temperature raise of IC substrate. The latchup of pin#22 and 24 are induced as an aggravated result by the heat produced by preceding latchup of pin#26.

For further confirmation, we used a simple digital thermometer to measure surface temperature of the package. It should be noted that though the response of digital thermometer was slow compared to temperature change in package, and the surface temperature between package and silicon might be quite different, measuring package surface temperature provided a fast observation in relationship between latchup resistance and temperature. Originally the surface temperature was 25°C. Applying a trigger current to pin#26 induced large power line current (about 400mA). Subsequent latchup and current-induced temperature raise (to about 110~130°C) occurred as a result. At this temperature pin#22 and 24 latched in sequential latchup test. Increasing cooling-down time between successive trigger from 1 to 5sec showed no latchup at pin#22 and 24 even in the following sequential test after pin#26 latched. Therefore, it should be concluded that latchup of pin#22 and 24 was a consequence of pin#26's latchup, and the design was quite temperature sensitive. Resolving pin#26 latchup problem also solved the following latchup of pin#22 and 24 simultaneously. Therefore, thermal-induced latchup aggravation should also be noticed during latchup testing.

3.2. Locating the latchup site

In order to locate the latchup site, we used EMission MIcroscope (EMMI) to find out the hot spots. After triggering pin#26 of decapped-latchup-failed samples into latchup, hot spots were found to locate at inside internal circuits, as shown in the right side of Fig. 2. Examining the layout revealed that hot spot corresponded to level shift circuits. The layout of level shift circuits is in Fig. 3, showing potential latchup paths.

In SCR path 1 of Fig. 3, though high-voltage P^+ thin oxide (HVP^+) connected to Vdd inside N-well to N^+ thin oxide connected to Vss consisted a parasitic SCR and was a possible latchup path, the anode-to-cathode spacing (~10um) was too far to contribute latchup. Another HVP^+ located in-between was another suspect as shown in SCR path 2 of Fig. 3. This HVP^+ was connected to V0~V4 (labeled in Fig. 3), which was biased to 10V(equal to Vdd) during latchup tests and consisted a potential latchup path.

To clarify the suspicion of this potential latchup path, V0~V4 were biased to low (0V) and samples were latchup tested again. As our prediction, no latchup occurred this time even large trigger current existed when triggering pin#26. In order to strengthen the latchup resistance of level shift circuits, Vdd and Vss guard bands (normally placed between I/O and internal circuits [3]) should be added with adequate

widths and N^+ pickups should be placed in N-well and in the SCR path 2 of Fig. 3 for improving negative latchup trigger characteristics.

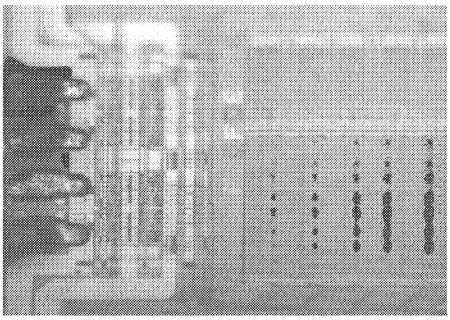


Fig. 2 The EMMI photo on latchup of decapped samples.

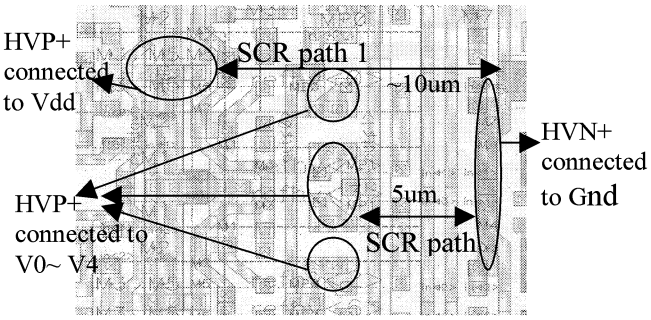


Fig. 3 Layout (fraction) of the level shift circuit in internal circuits.

3.3. Identifying the trigger source

Though the failure site was found by EMMI and proved by the subsequent experiments, the reason for initial large current during trigger that resulted in latchup remained unknown. It was assumed that there were devices triggered to turn on and conducted large currents, therefore contributing to the detection of large Idd during trigger. Since the pin#26 was comprised of the same cell as other side output pins (see Fig. 1), we investigated on other subtle layout difference in order to distinguish layout of pin#26 from others. After thorough comparison, N-well resistor beside output cell was discovered and also shown in Fig. 1(b). The N-well resistor was used as the resistor of GRPMOS ESD power clamp circuits and was shared by 19 HVPMOSs as a group. The N-well resistor had one end connected to Vdd and another connected to the gates of HVPMOSs, as shown in Fig. 1(c) for schematic and Fig. 4 for real circuit layout.

For further latchup characteristic investigation, power line current during trigger was monitored and large Idd during trigger was found for pins with N-well resistor of GRPMOS near by, recorded in Fig. 1(a). Another pin, pin#57, is opposite to pin#26 and is composed of same side output cell and a N-well resistor beside. As a further verification on influence of the N-well resistors, pin#57 were also tested for trigger characteristics. The result also showed large Idd during trigger (~300mA).

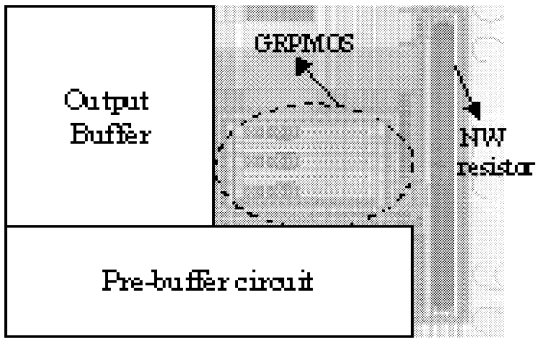


Fig. 4 Layout of the GRPMOS beside pin#26. N-well resistor was connected between gate of HVPMOSs and Vdd and was shared by 19 shunted HVPMOSs.

By using prolonged current trigger the EMMI showed hot spots on HVPMOSs that were shunted together, as shown in Fig. 5. Carefully examining the EMMI photo revealed that hot spots emerged for PMOSs of the same group, indicating PMOSs of this group were probably turned on at the same time.

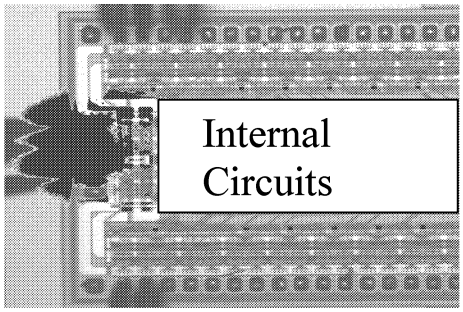


Fig. 5 EMMI photo when pin#26 was under DC trigger. Large Idd existed during trigger period. HVPMOSs with hot spots were in the same group sharing a common N-well resistor.

Combining the particular trigger characteristic of pin#26 with NW resistor beside and the hot spots on PMOS from EMMI, it indicated that GRPMOS should be substantially related to large Idd during trigger. It was assumed that the large Idd during trigger was contributed from the turning-on of GRPMOS. The cross-section view of a GRPMOS and NW resistor was shown in Fig. 6.

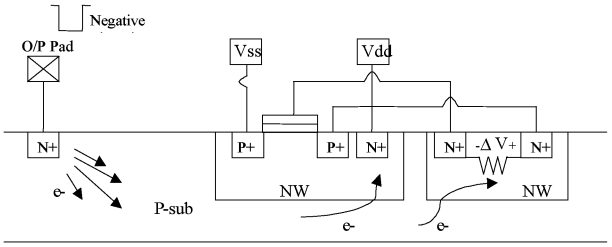


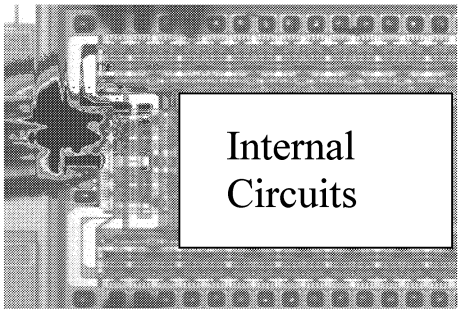
Fig. 6 Cross section of GRPMOS and NW resistor. Only one HVPMOS was shown where in actual the NW resistor is shared by 19 HVPMOSs.

First, the GRPMOSs were suspected to be coupled to turn on during negative trigger since the power-on signal of triggering current was also a transient signal. If the negative voltage was coupled to the gates of HVPMOSs via the Cgd capacitor, the gates of HVPMOSs could be biased to low and turned on PMOSs. However, considering the short RC-time constant, which was in sub-μs order as compared to the near-ms-order rise time of the trigger current, coupling turn-on of HVPMOSs was not likely.

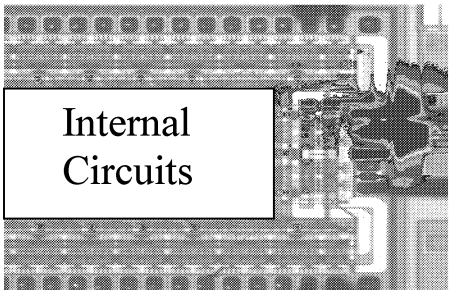
The second assumption can be realized from Fig. 6. Since electrons were injected in negative trigger, and a N^+ node of NW resistor was connected to Vdd and can collect electrons, if the N^+ pickup between pad and the NW resistor was not enough to collect electrons efficiently, the remaining electrons may reach the NW resistor, flow through it and be collected by N^+ connected to Vdd. This caused a voltage drop across the NW resistor. And since the sources of HVPMOSs were connected to Vdd and its gates were connected to other end of NW resistor, the voltage drop between two ends of the NW resistor also appeared equally across gates and sources of HVPMOSs. If the voltage drop is large, resulting in the Vgs of HVPMOSs to be more negative (larger in magnitude) than threshold voltage, HVPMOSs may be turned on. It should be noted that since the NW resistor had quite large value, therefore, only small fraction of triggering electron flow is needed for causing voltage drop large enough to turn on PMOS. And since all HVPMOSs of the same group were gate-biased through this NW resistor, they were turned on as a whole in results. The total width of these HVPMOSs was 1900μm, therefore the turning-on of these PMOSs can contribute to large current between Vdd and Vss. From the aforementioned experiments, it was known that the large current can give rise to temperature considerably and latchup degradation, finally leading to latchup of internal circuits.

In order to verify the hypothesis, FIB (Focused Ion Beam) was used to cut off the path of electron flow to prevent this e^- flow from building up a voltage drop across NW resistor and turning on HVPMOSs. Since cutting NW resistor only was not feasible (because there would be no discharge path for gates of HVPMOSs when triggered and gates of HVPMOSs would be coupled low and turn on HVPMOSs if the NW resistor was cut away only), we cut the NW resistor at both ends and shortened the gates of HVPMOSs to Vdd to turn off the HVPMOSs. The result was satisfactory. There are no large Idd during trigger and no hot spot emerged for gate reconnected to Vdd and NW cut samples, shown in Fig. 7(a). As a comparison, we tested the opposite side pin (pin#57) with another NW resistor beside on the same samples. Large current (~300mA) and hot spots still existed, as shown in Fig. 7(b).

Therefore, from the results of experiments mentioned above, we concluded the large Idd during trigger was due to the turning on of HVPMOSs, and the gates of HVPMOSs were biased to turn on these HVPMOSs because of the voltage drop built up by electrons flowing across the N-well resistor.



(a)



(b)

Fig. 7(a) EMMI on wafer-level samples with NW resistor cut off and HVPMOSs' gates reconnected to Vdd. No hot spot on EMMI and no large Idd during trigger. (b) As a comparison, pin#57 of same samples were also LU tested. Hot spot and large Idd existed.

3.4. Improvements to remove latchup source

Since the root cause of latchup in this case is the NW resistor, the modification to prevent the latchup failure can be done in several ways, with first modification involving in removing the source of large power line current and another reducing injecting carriers.

For large power line current during trigger to be diminished, HVPMOSs shall remain off during trigger. The first and most convenient method is to modify one mask (only in metal layer) to shorten the gates of HVPMOSs of ESD protection circuits to Vdd to make them always off and conduct ESD currents in breakdown mode. However, degradation in ESD performance is expected.

Another method lies in the key that the NW resistor will not build up enough voltage drop if there are not sufficient injecting carriers. In order to eliminate latchup issue while sustaining same ESD level, modification can be done by placing the NW resistor farther away from I/O cells and add N^+ guard rings [2]. Since the injected carriers from pad are recombined as they diffuse toward internal circuits, farther distance between latchup-sensitive devices and pad implies less injecting carriers and better latchup resistance. In addition, the N^+ guard rings connected to Vdd surrounding the NW resistor can collect injecting electrons of negative trigger current efficiently before the injected electrons are collected to the Vdd-end of NW resistor and result in voltage drop across it. However, modification must be done at higher cost as more layers and masks are modified.

4. Discussion

The root cause of this anomalous latchup is now identified to be NW resistor and it corresponded to the layout particularity of pin#26. Examining layout revealed that pin#26 had the nearest distance to the NW resistor and least N^+ pickups since most upper area of pin#26 is blank on silicon substrate except metal line running over the bulk substrate, as compared with other output pins which having enough N^+ pickups of neighboring pins surrounding. Therefore, triggering electrons injected from pin#26 had largest quantity to reach the NW resistor.

Referring to Fig. 2, it should be noted that, contrary to EMMI on conventional latched up samples that normally showed brighter hot spot in internal circuits at position nearest to I/O than those farther from I/O, the EMMI of LU failed samples showed brighter hot spot occurred at more inner level shift circuits. This phenomenon could be explained by Fig. 8. In general, since carriers injected from the pad experienced recombinations and collected by pickups or guard rings, they became more insufficient to induce latchup in more inner internal circuits; hence no latchup was observed above certain distance far from I/O. However, because the level shift circuits were placed in parallel in columns and connected to same pad, series resistance of metal line varies with outmost column having the largest series resistance. Once latched, the parasitic series resistor from metal line can act as current-limiting resistor, resulting in the least severe LU situation (the weakest hot spot) at the level shift circuit nearest to pad.

Though the gate-triggered structures have been widely used and proved to be efficient ESD protection circuits, the resultant LU failure caused by this structure has not been presented as authors' knowledge, and that the biasing of MOS could only occur in gate-triggered *P*MOS since the NW is connected to Vdd at one end. In the case of gate-triggered *N*MOS, the NW resistor is connected to Vss and would not draw electron flow. Thus, there would be no voltage drop across NW resistor during normal trigger, and NMOS would not be biased to turn on.

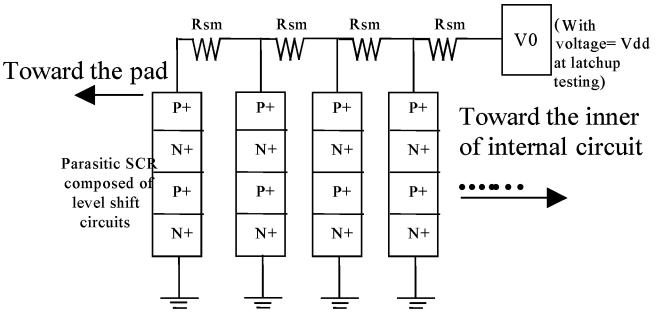


Fig. 8 Schematic of latchup paths. The pnpn parasitic SCR represents the HVP^+ to HVN^+ latchup path, and Rsm represents the parasitic series resistance of metal line.

5. Conclusion

From the experiments, the latchup failure can be ascribed to the thermal-aggravated latchup degradation by large power line current due to the turning on of HVPMOSs in ESD protection circuit, and the turning on of the HVPMOSs is due to the voltage build-up of NW resistor of injecting electrons.

The improvements to LU failure in this case can be made in two ways: One is to increase the internal circuit robustness against latchup and another is to remove the trigger source that induced large Idd during latchup tests.

Originally, there were no Vdd-Vss guard bands between I/O cells and internal circuits which were common and essential in normal chip layout for latchup resistance. And it was shown in our latchup testkeys and other reported literature that placing pickups within internal circuits improved trigger level and hardness against latchup, especially when placed inside the parasitic SCR path. Therefore, pickups should be placed between the HVP^+ and HVN^+ of level shift circuits to strengthen the resistance of internal circuit for incoming injected carriers from I/O. Also Vdd-Vss guard bands should be placed between I/O cells and internal circuits in order to intercept and collect carriers away before injecting carriers can reach internal circuit and possibly cause latchup.

To remove the trigger source, since latchup in this case has originated from electrons flowing through NW resistor, the way to remove this trigger source is to eliminate this path. Since NW resistor must remain intact for maintaining ESD performance, N+ guard ring connected to Vdd and surrounding this NW resistor can be added to collect the electrons to prevent them from biasing on HVPMOSs.

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