Failure Analysis of ESD Damage in a High-Voltage Driver IC and the Effective ESD Protection Solution

Ming-Dou Ker, Jeng-Jie Peng*, and Hsin-Chin Jiang*

Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics
National Chiao-Tung University, Taiwan
E-mail: mdker@ieee.org

*Analog IP Technology Section
SoC Technology Center
Industrial Technology Research Institute, Taiwan
E-mail: jjpeng@ieee.org

1. Introduction

Internal damage caused by ESD stress has been found in the mixed-voltage silicon chips, recently. Even with suitable ESD protection circuits around the input and output pins, the internal circuits are still damaged by the ESD stress [1]-[6]. This problem becomes more serious in silicon chips containing both the high-voltage circuit block and the low-voltage circuit block. In such mixed-voltage designs, the ground lines of the low-voltage digital circuit block and the high-voltage analog block are traditionally separated for noise consideration. With separated ground lines, the internal gate-oxide damage phenomenon is found at the digital-analog interface circuit after ESD tests.

To investigate the internal damage phenomenon of such mixed-voltage silicon chips, a high-voltage driver IC fabricated by a 1.0-μm 12V/5V 1P2M CMOS process for organic light emitting diode (OLED) display panel is used as an example. Two versions of OLED high-voltage driver IC had been fabricated. Ground lines of the original version design for high-voltage and low-voltage circuit blocks are separated. Ground lines for high-voltage and low-voltage circuit blocks in the new version IC are connected via an ESD cell. The human body model (HBM) ESD test was used to verify the ESD immunities of these two versions of IC's.

To find the ESD failure spots, some failure analysis (FA) procedures, such as decap of packaged IC's and de-layer of silicon dies, were applied to the OLED high-voltage driver IC's. The optical microscope (OM) and scanning electronic microscope (SEM) were used to find the ESD damaged failure spots of the silicon dies. By comparison with the SEM photos of ESD damaged failure spots and the related IC circuits and layout patterns, the failure reasons of ESD weak points were analyzed and found in the original version chip. An effective ESD protection solution for improving the ESD robustness of the high-voltage driver IC is proposed, which has been proved by the new version chip.

2. Internal ESD Damage of Mixed-Voltage IC's

2.1 ESD Tests for Mixed-voltage IC's

The HBM ESD equivalent circuit diagram is introduced in Fig. 1 [7], which is used to simulate the event of electrostatic charges discharging from fingertips of a human body to a silicon IC. For commercial IC's, the requirement of HBM ESD immunity is generally to pass ESD stress of at least 2.0kV with both positive and negative polarities.

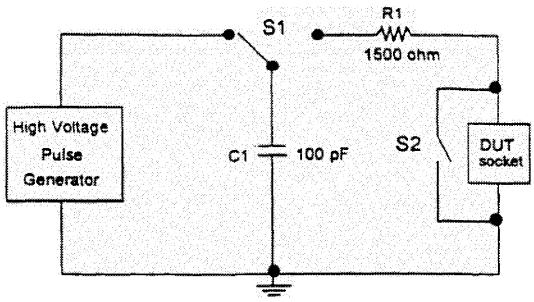

Fig. 1 ESD human body model equivalent circuit diagram of JEDEC JESD22-A114-B standard [7]. Charges are stored in the capacitor of C1 first, and then are discharged to the device under test (DUT) via the R1 of 1500ohm.

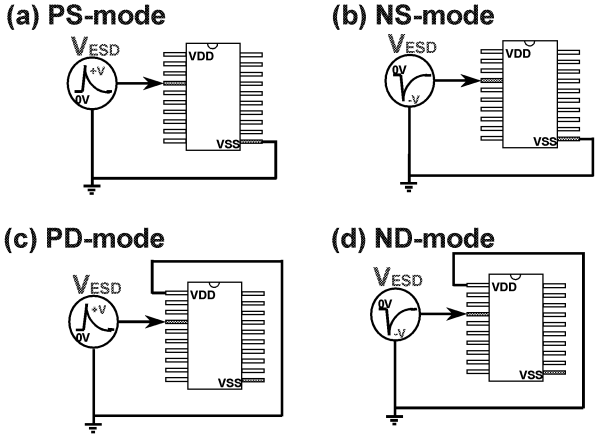

Fig. 2 Four modes of ESD stresses on an input or output pin with relatively grounded VDD or VSS pins [8].

Since an ESD stress may have positive or negative voltage polarity on an input or output pin with reference to grounded VDD or VSS pins, there are four different ESD stress modes on an input or output pin, which are shown in Fig. 2 [8]. Moreover, ESD current could enter into any pin and go out from another pin of an IC. To practically verify the whole chip ESD reliability, two additional ESD test

conditions have to be considered. These two conditions, the pin-to-pin ESD stress and the VDD-to-VSS ESD stress, are shown in Fig. 3 [6]-[7]. In Fig. 3(a), the ESD stress is applied on an input or output pin as other input and output pins are all grounded but both VDD and VSS pins are floating. In Fig. 3(b), the ESD voltage is directly applied on the VDD pin(s) with VSS pin(s) relatively grounded but all input and output pins are floating.

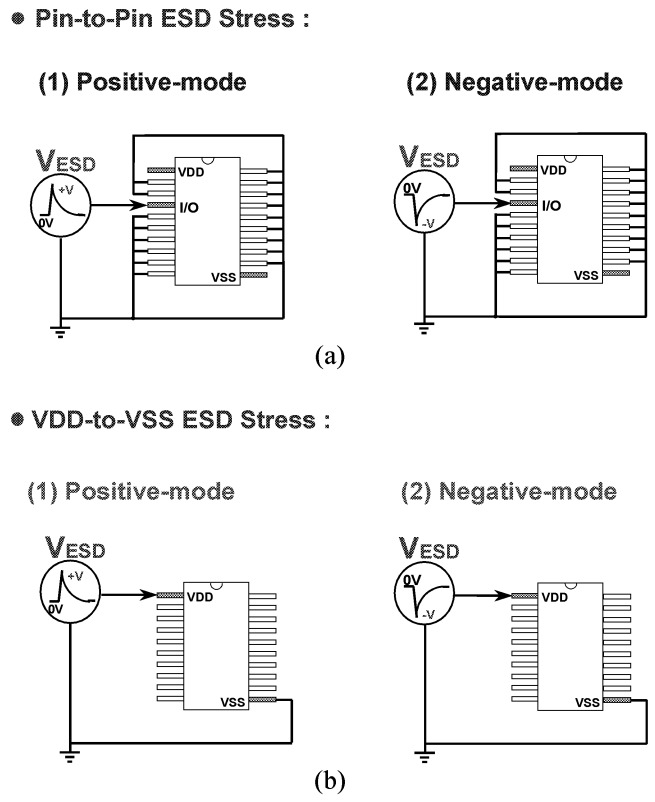

Fig. 3 Two additional ESD test conditions, (a) the pin-to-pin and (b) VDD-to-VSS ESD stresses, to verify the whole chip ESD reliability.

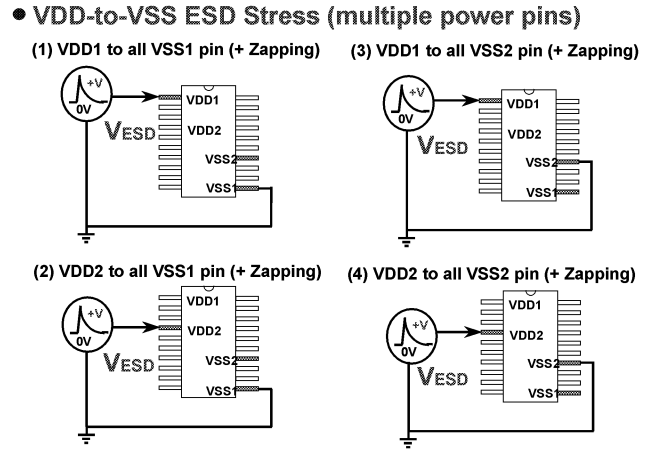

Fig. 4 ESD test for an IC with multiple power lines to verify its whole chip ESD reliability.

For an IC with multiple power lines (an mixed-voltage IC), another pin combination of ESD test shown in Fig. 4 is necessary to verify the ESD immunity of an IC product. In Fig. 4, each voltage level of VDD pin-group (ex. VDD1) should be stressed with one of the VSS pin-groups grounded (ex. VSS1). Then, the VDD pin-group under test (PUT) is stressed with another VSS pin-group relatively grounded (ex. VSS2), and so on. Until the VDD PUT is stressed with all the VSS pin-groups relatively grounded in sequence, another VDD pin-group with different voltage level (ex. VDD2) is taken as the next PUT. Except the VDD and VSS PUT's, all other pins are floating while processing the ESD test shown in Fig. 4. In these three additional test conditions shown in Fig. 3 and Fig. 4, the CMOS IC's are more vulnerable to internal ESD damage even if there are suitable input and output ESD protection circuits on the input and output stages.

2.2 ESD Protection Design for Original Driver IC

The whole chip ESD protection design for the original version of the investigated high-voltage driver IC is shown in Fig. 5. The VDDD (VDDA) shown in Fig. 5 is the low-voltage digital (high-voltage analog) power pin, and the GNDD (GNDA) is the low-voltage digital (high-voltage analog) ground pin.

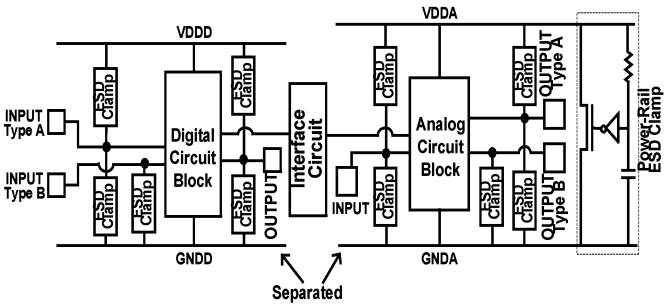

Fig. 5 The original ESD protection design of the high-voltage driver IC. There is no power-rail ESD clamp circuit in the low-voltage digital circuit block. Moreover, the power (ground) pins are separated between the digital and analog circuit blocks.

There are several ESD weak designs in the ESD protection of Fig. 5. First, for the low-voltage digital input and the high-voltage analog output stages, there are two types of ESD protection designs. In the "Type A" designs, as shown in Fig. 5, there are ESD clamp circuits both at the pad-to-VDD and the pad-to-VSS paths. But in the "Type B" designs, the ESD clamp circuits are only located at the pad-to-VSS paths, and there is no ESD clamp circuit at the pad-to-VDD paths. When a positive ESD stress is applied on the pad with the VDD pins relatively grounded, a lower ESD level might be revealed in the "Type B" designs. Second, there is no power-rail ESD clamp circuit between the VDDD and the GNDD pins. When processing the VDDD-to-GNDD ESD test shown in Fig. 3(b), the ESD current might be directly applied into the internal digital circuit block without

the protection of the power-rail ESD clamp circuit. Then, internal damage phenomenon might be revealed after the ESD stress. Moreover, the GNDD line and the GNDA line are separated. This easily causes a damage located at the interface circuit of the digital and analog circuits when the VDDA-to-GNDD, VDDD-to-GNDA, and the digital I/O to analog I/O ESD tests are performed.

2.3 Internal Damage Due to Separated Power Pins

When an ESD test is proceeded, the failure criteria to judge whether the pin under test is passed or failed after the ESD stress is dependent on the increase of leakage current and IC function tests. If both the leakage current and the function tests are within the specifications of the device under test (DUT), it is classified as passed at the operated ESD stress voltage. For example, the traced I-V characteristics of the investigated IC before and after ESD stress are shown in Figs. 6(a) and 6(b), respectively. Both of the I-V curves were measured by Tek370 curve tracer for VDDD pin with GNDA pin relatively grounded. The x-axis is the VDDD-to-GNDA voltage in 1V/div. The y-axis is the corresponding current in 100μA/div. and 2mA/div. for Figs. 6(a) and 6(b), respectively. Fig. 6(a) shows the normal I-V characteristics of VDDD-to-GNDA before the HBM ESD stress. Fig. 6(b) shows the I-V characteristics of VDDD-to-GNDA after a 1.5kV HBM ESD stress. Obviously, after the 1.5kV HBM ESD stress, leakage current at 5V between VDDD and GNDA is increased notably over 20 times of the one in the normal I-V characteristics. This indicates that there are some internal damages in the internal circuit blocks after the HBM ESD stress.

Following the test conditions described in Fig. 3 and Fig. 4, and the failure criteria mentioned above, the HBM ESD tests were performed on the original version of the OLED high-voltage driver IC. The experimental results show that the HBM ESD immunity of the original version is only 1.0kV, which is lower than the commercial specification of 2.0kV. In order to find the failure locations caused by such a low HBM ESD level, the damaged samples zapped by VDDD-to-GNDD, VDDD-to-GNDA, VDDA-to-GNDD, or VDDA-to-GNDA HBM ESD stresses were used to perform some FA procedures to find out the ESD weakness of the original version high-voltage driver IC. Figs. 7(a)-7(d) show the SEM pictures and the corresponding IC layout patterns of the failure sample stressed by the VDDD-to-GNDA HBM ESD stress. Figs. 7(a) and 7(b) are global views of all the internal ESD damaged spots. All the circled areas in Fig. 7(a) are the damaged locations taken by SEM after HBM ESD stress. Fig. 7(b) is the corresponding layout patterns of Fig. 7(a). From the zoom-in SEM picture shown in Fig. 7(c), the indicated circle is easily recognized that the internal damaged failure is the gate oxide damage on a high-voltage NMOS after ESD stress. Moreover, the layout pattern shown in Fig. 7(d), which is the corresponding layout pattern of the damaged spot of Fig. 7(c), is recognized as a part of the interface circuit between the low-voltage digital block and the high-voltage analog block.

Fig. 8 shows the interface circuit between the low-voltage digital block and the high-voltage analog block of the original version high-voltage driver IC. The voltage levels of VDDA and VDDD at normal operation are 12V and 5V, respectively. ESD current path along the interface circuit of the high-voltage driver IC under the VDDD-to-GNDA ESD stress is shown in Fig. 8. Due to the GNDD line and GNDA line are not connected together, the ESD current under VDDD-to-GNDA stress is forced along the dash line in Fig. 8. It flows through the low-voltage PMOS P3 and the gate oxide breakdown of the high-voltage NMOS N1, as shown in Fig. 8. The unexpected current flow leads to the gate oxide damage of the high-voltage NMOS N1. The failure spot shown in Fig. 7(c) is located at the node "A" of Fig. 8. The above experimental results imply that without suitable ESD protection design between the separated ground lines of the mixed-voltage design, internal damages easily happen at the interface circuit between the low-voltage digital block and the high-voltage analog block.

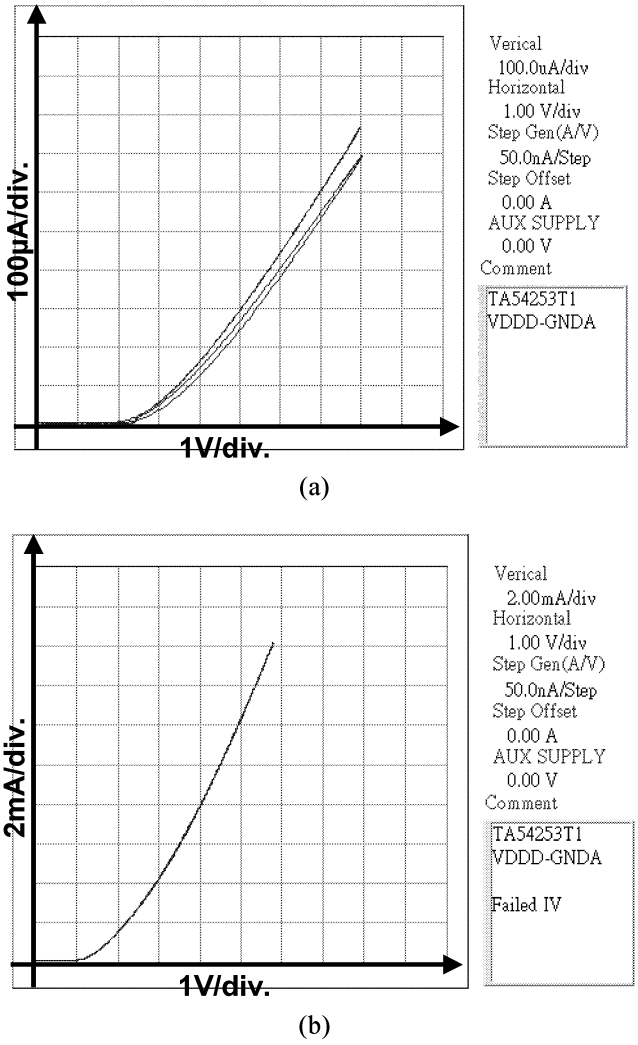

Fig. 6 The I-V characteristics of VDDA-to-GNDA (a) before HBM ESD stress (b) after +1.5kV HBM ESD stress. The x-axis is the VDDD-to-GNDA voltage in 1V/div.

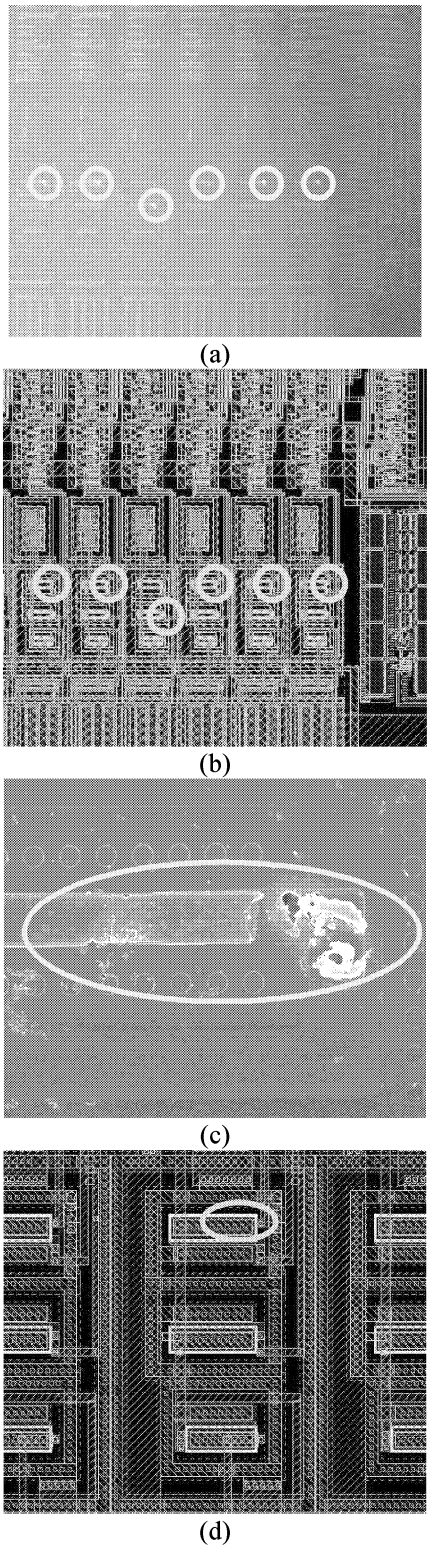

Fig. 7 (a) The SEM failure picture of the high-voltage driver IC after HBM ESD stress of VDDD-to-GNDA. The circled points show the ESD damaged locations. (b) The corresponding layout of internal circuits to the ESD damaged locations shown in (a). (c) The zoom-in SEM picture of one of the ESD stressed failure spot shown in (a). (d) The corresponding layout location of that shown in (c).

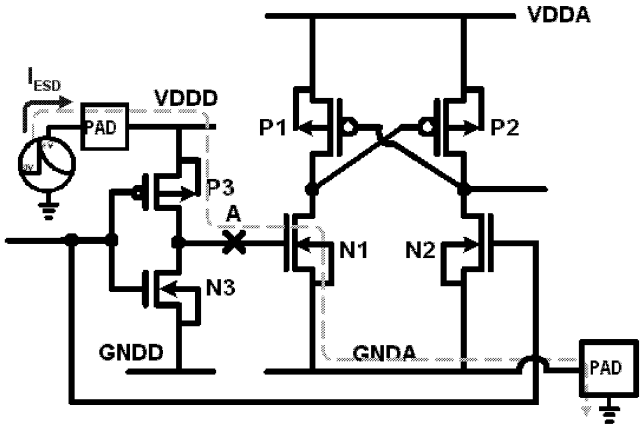

Fig. 8 The interface circuit between digital and analog blocks of the original design of the investigated high-voltage driver IC. Due to the separated GNDD and GNDA lines, the ESD current is discharged through the gate of N1 transistor under the VDDD-to-GNDA ESD stress.

3. Solutions and Experimental Results

3.1 Solutions for Solving Internal ESD Damage

To solve the internal ESD damage issue located at the interface circuit between digital circuit block and analog circuit block with separated power lines, one of the suggested ESD protection design is shown in Fig. 9 [6]. By adding extra ESD clamp circuits near the input gates of both the high-voltage and low-voltage blocks, the gate oxide of the input stage can be effectively protected.

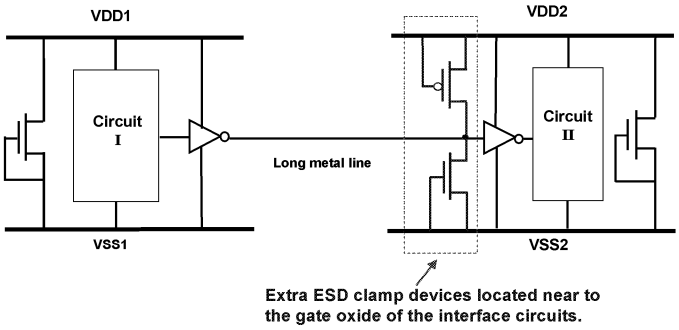

Fig. 9 Prior solution to rescue the ESD failure located at the interface circuit of an IC with separated power lines [6].

A more effective methodology to solve this kind of ESD issue is shown in Fig. 10 [9]. This methodology is known as the whole chip ESD protection scheme proposed for solving the ESD internal damage problem. As shown in Fig. 10, the separated ground lines and the power lines of different circuit blocks are connected via ESD cells. Thus, accompanying with the VDD-to-VSS power-rail ESD clamp cells, the ESD current comes from any pin can be effectively discharged without damaging the internal circuits. The ESD cell used to connect the separated ground (power) lines can be

implemented by using bi-directional diode strings [9]-[17], or even the bi-directional SCR devices [18]-[19]. The diode number in the diode strings can be adjusted for noise consideration.

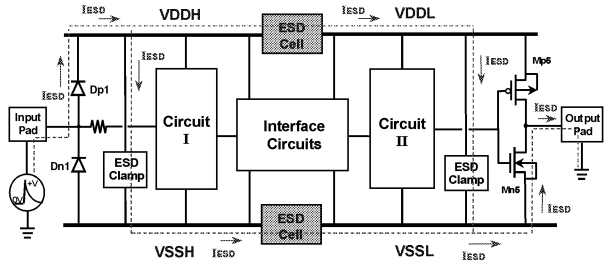

Fig. 10 A whole chip ESD protection scheme proposed for solving the ESD internal damage problem. The dash lines indicate the possible ESD current paths of a CMOS IC with mixed-voltage power supplies under pin-to-pin ESD stress.

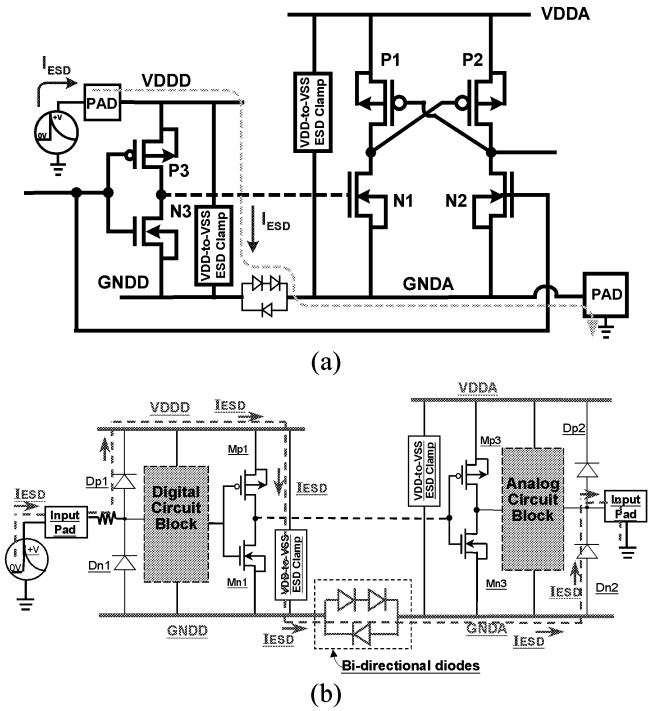

Fig. 11 The effective ESD protection solution, which was applied on the new version high-voltage driver IC for solving the internal damage issue. The dash lines indicate the possible ESD current paths under (a) VDDD-to-GNDA ESD stress, and (b) pin-to-pin ESD stress, respectively.

Fig. 11 shows the ESD protection solution to overcome such ESD failure in this investigated high-voltage driver IC. It is modified from the whole chip ESD protection scheme shown in Fig. 10. There are several differences comparing with the original design and the proposed solution shown in Fig. 11. One is that an additional ESD clamp device is added between the input/output pad and the VDD power line for the "Type B" design shown in Fig. 5. The additional power-rail ESD protection circuit is also added between VDDD and GNDD of the low-voltage digital circuit block for sustaining the VDDD-to-GNDD ESD stress. The separated ground pins, GNDD and GNDA, between digital and analog circuit blocks are connected together via an ESD cell of bi-directional multiple-diode strings [9] to provide effective ESD current discharge path. The diode in the ESD cell is formed by a p-type diode, which comprises a p+ region at the center, and a n+ ring surrounds the p+ region. Both the p+ and n+ regions are enclosed in an n-well region. The PN junction perimeter of this p-type diode is 102.9μm for each. With comparison to the whole chip ESD protection scheme shown in Fig. 10, there is no ESD cell between the separated power lines, VDDD and VDDA, in Fig. 11. This is because of the large voltage difference between VDDA and VDDD in the high-voltage driver IC product. By using the proposed ESD protection design solution, the ESD current paths under VDDD-to-GNDA and pin-to-pin ESD stresses are indicated by the dash lines of Figs. 11(a) and 11(b), respectively. According to the expected ESD current paths shown in Fig. 11, the internal damage problem can be prevented.

3.2 Experimental Results of the Modified High-Voltage Driver IC

A new version of IC layout with all mask layers change has been fabricated by the same 1.0-μm 12V/5V 1P2M CMOS process. The proposed effective ESD protection solution shown in Fig. 11 is implemented in the new version silicon chip. The HBM ESD test results for the original version and the new version of the high-voltage driver IC's are compared in Table I. The listed ESD levels in Table I are referred to the lowest (most critical) HBM ESD levels of the original version IC products. "DI" and "AO" in Table I are digital input pin and analog output pin, respectively. All the HBM ESD tests were started from 0.5kV with the KeyTek Zapmaster as an ESD simulator, and the voltage level was increased with a voltage step of 0.5kV until the DUT was failed.

Table I : ESD Level Comparisons

ESD Test	Original Version	New Version
VDDD-to-GNDD	+1.5kV	+2.5kV
VDDD-to-GNDA	+1.5kV	+2.5kV
YSCL(DI)-to-VDDA	+1.0kV	> +8.0kV
YSCL(DI)-to-VDDD	+1.0kV	> +8.0kV
ROW4(AO)-to-GNDA	+1.0kV	+2.0kV

With the help of the "Type A" ESD protection design applied on all of the I/O pins and the power-rail ESD clamp circuit between the VDD and VSS pins, the pin-to-VDD and pin-to-VSS ESD levels are obviously improved for each circuit block. For example, the YSCL low-voltage digital input pin in Table I is originally designed as the "Type B" style shown in Fig. 5 without an ESD clamp device at the pad-to-VDDD path. Besides, there is no VDDD-to-GNDD power-rail ESD clamp circuit for the low-voltage digital

circuit block in the original version. In the chip of new version, an ESD clamp of PN junction diode was inserted between the YSCL pin and the VDDD, and the VDDD-to-GNDD power-rail ESD clamp circuit was also implemented in the low-voltage digital circuit block. With such modification, the HBM ESD robustness of the YSCL pin is improved from 1.0kV to over 8.0kV for the digital circuit block.

Moreover, with the separated ground lines (GNDD and GNDA) connected via an ESD cell of bi-directional diode strings, the ESD levels of VDDD-to-GNDD and VDDD-to-GNDA are improved from 1.5kV in the original design to 2.5kV in the new design. With the modifications in the new design, the HBM ESD robustness of the whole chip was improved from 1.0kV to greater than 2.0kV.

4. Conclusion

The internal damage issue caused by ESD stress was investigated through a real case of high-voltage driver IC with separated power pins. After the HBM ESD tests applied on silicon chips of the original design, failure analysis was done with the help of OM and SEM to find out the failure spots. The results of failure analysis show that the internal damages on the interface circuit of two circuit blocks are caused due to the absence of the VDD-to-VSS power-rail ESD cell and the ESD cell of connecting different ground lines. By using the proposed effective ESD protection solution, the HBM ESD robustness of the high-voltage driver IC product can be improved to greater than 2.0kV.

References

[1] C. Duvvury, R. N. Rountree, and O. Adams, "Internal chip ESD phenomena beyond the protection circuit," *IEEE Trans. on Electron Devices*, vol. 35, no. 12, pp. 2133-2139, 1988.

[2] M. D. Jaffe and P. E. Cottrell, "Electrostatic discharge protection in a 4-Mbit DRAM," in *Proc. of EOS/ESD Symp.*, 1990, EOS-12, pp. 218-223.

[3] H. Terletzki, W. Nikutta, and W. Reczek, "Influence of the series resistance of on-chip power supply buses on internal device failure after ESD stress," *IEEE Trans. on Electron Devices*, vol. 40, no. 11, pp. 2081-2083, 1993.

[4] C. Johnson, T. J. Maloney, and S. Qawami, "Two unusual HBM ESD failure mechanisms on a mature CMOS process," in *Proc. of EOS/ESD Symp.*, 1993, EOS-15, pp. 225-231.

[5] C. Cook and S. Daniel, "Characterization of new failure mechanisms arising from power-pin ESD stressing," in *Proc. of EOS/ESD Symp.*, 1993, EOS-15, pp. 149-156.

[6] M.-D. Ker and T.-L. Yu, "ESD protection to overcome internal gate-oxide damage on digital-analog interface of mixed-mode CMOS IC's," in *Proc. of the 7th ESREF*, 1996, pp. 1727-1730.

[7] JESD22-A114-B, *JEDEC Standard for Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, JEDEC, VA, 2000.

[8] M.-D. Ker, C.-Y. Wu, and H.-H. Chang, "Complementary-LVTSCR ESD protection circuit for submicron CMOS VLSI/ULSI," *IEEE Trans. on Electron Devices*, vol. 43, no. 4, pp. 588-598, 1996.

[9] M.-D. Ker, "ESD protection circuit for mixed mode integrated circuits with separated power pins," US patent #6,075,686, Jun. 2000.

[10] K. Yoshitake, "Integrated circuit having two circuit blocks therein independently energized through different power supply terminals," US patent #4,855,863, Aug. 1989.

[11] B. J. Misek, "Method for protecting mixed signal chips from electrostatic discharge," US patent #5,926,353, July 1999.

[12] H. P. Nguyen and J. D. Walker, "Electrostatic discharge protection system for mixed voltage application specific integrated circuit design," US patent #5,616,943, Apr. 1997.

[13] F. Saleh, "System including ESD protection," US patent #5,991,135, Nov. 1999.

[14] J. S. So, "ESD protection circuits," US patent #6,025,746, Feb. 2000.

[15] C. Duvvury, E. A. Amerasekera, and S. Ramaswamy, "EOS/ESD protection for high density integrated circuits," US patent #6,040,968, Mar. 2000.

[16] J. P. Pequignot, T. Rahman, J. H. Sloan, D. W. Stout, and S. H. Voldman, "Method for providing ESD protection for an integrated circuit," US patent #6,262,873, July 2001.

[17] T. Nakura and K. Ueda, "Semiconductor integrated circuit device including electrostatic protection circuit accommodating drive by plurality of power supplies and effectively removing various types of surge," US patent #6,208,494, Mar. 2001.

[18] M.-D. Ker and H.-H. Chang, "ESD protection scheme for mixed-voltage CMOS integrated circuits," US patent #6,002,568, Dec. 1999.

[19] M.-D. Ker and H.-H. Chang, "Whole-chip ESD protection for CMOS ICs using bi-directional SCRs," US patent #6,011,681, Jan. 2000.

Acknowledgements

The authors would like to thank their colleagues, Mr. Ian Chih-Chiang Chiang, Mr. Joseph Yao-Cheng Tsai, Miss King-Ting Chiang, and Miss Mei-Chu Liu, for the help of ESD tests and failure analysis procedures done for this paper.