

Latchup Current Self-Stop Circuit for Whole-Chip Latchup Prevention in Bulk CMOS Integrated Circuits

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ABSTRACT

A latchup current self-stop methodology and circuit design, which are used to prevent damage in the bulk CMOS integrated circuits due to latchup, are proposed in this paper. In a bulk CMOS chip, the core circuit blocks are always latchup sensitive due to a low holding voltage of the parasitic SCR path. The proposed latchup prevention methodology and circuit design can detect and stop the occurrence of latchup without any process modification or extra fabrication cost. It is suitable for whole-chip latchup prevention of bulk CMOS integrated circuits. This proposed latchup current self-stop methodology and circuit have been verified in a 0.5- μm 1P3M bulk CMOS process.

1. INTRODUCTION

Due to the parasitic silicon controlled rectifier (SCR) path, latchup phenomenon had been an inherent problem for bulk CMOS IC's. Under some conditions such as terminal over-voltage stress, transient displacement currents, or ionizing radiation, the trigger in the n-well and p-substrate can cause sufficient voltage drop, which forward biasing emitter-base junctions and activating both bipolar devices of the parasitic SCR. When the current gain product of the two bipolar devices in the parasitic SCR is higher enough to sustain regeneration, the parasitic SCR can be turned on to cause latchup phenomenon [1]-[2].

There are three kinds of conventional methods to improve latchup immunity [3]-[4]. One is the process technique. For examples, epitaxial wafer, retrograde well, trench isolations, and SOI are all helpful to improve latchup immunity. The second technique is the layout skill. Adding guard-rings between PMOS and NMOS circuit blocks [5]-[8], increasing multiple well contacts, or enlarging the spacing between PMOS circuit block and NMOS circuit block are typical examples of layout skill to improve latchup immunity. The third technique is to insert

transient current detection circuits into silicon chips to detect the latchup phenomenon [9]-[10]. All of these methods are applied with extra cost for process modification or additional large layout area.

In this paper, a new methodology is proposed to prevent the core circuits from damage by latchup phenomenon. The proposed method can detect and stop the occurrence of latchup [11]. A circuit implementation of the new methodology is also proposed and verified in a 0.5- μm 1P3M bulk CMOS process.

2. LATCHUP CURRENT SELF-STOP METHODOLOGY

Fig. 1 shows the function diagram of the proposed latchup current self-stop methodology. In Fig. 1, the "Int. VDD" is the internal core power supply. When latchup sensitive path of the core circuit block shown in Fig. 1 is triggered on, a large DC current is appeared between the "Int. VDD" and ground. This large current is then detected by the current extractor and fed back to the switch (SW-A or SW-B or both) on the diagram of Fig. 1. The switch is designed with a specific threshold, so that it can be turned on or off as expected. The feedback signal from the current extractor is used to make the switch (SW-A or SW-B or both) open, so that the latchup current can be shut off under the existence of internal core power supply.

The switches shown in Fig. 1 can be either current-controlled or voltage-controlled switches. If a voltage-controlled switch is chosen, an additional current-voltage converter should be applied between the current extractor and the switch.

Although the function diagram shown in Fig. 1 is implemented with a current extractor, a voltage level extractor for sensing voltage level variation of the parasitic SCR can be used to replace the current extractor also.

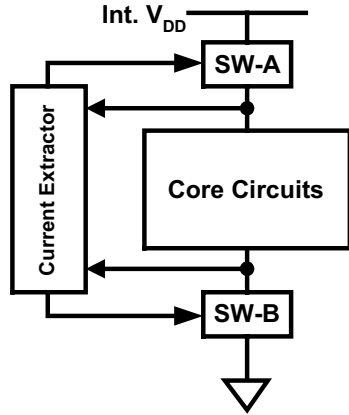


Fig. 1 The function block diagram of the proposed new latchup current self-stop methodology.

3. CIRCUIT IMPLEMENTATION

A circuit implementation for the proposed latchup current self-stop methodology is shown in Fig. 2. In Fig. 2, the numbers squared by rectangles are the signal pins connected to the bonding pads of the experiment silicon chip. Power supply is applied between pin2 and pin5, where pin2 is as VDD and pin5 is as VSS. Actually, Pin1 is connected with pin2 under normal operation. It is separated with pin2 only for experimental purpose. Pin3 is the power supply node of the ring oscillator, which is blocked with gray dashed line and is used to simulate an internal core circuit which contains a latchup sensitive SCR path. The NMOS transistors of Mn1 and Mn2 are constructed as a current mirror, which is used to implement the current extractor of Fig. 1. The resistor R between pin1 and pin7 is used to implement a current-voltage converter, which transmits the feedback current signal to the switch SW-A of Fig. 1. The inverter INV and the PMOS transistor Mp1 are used to construct a voltage-controlled switch to implement the switch SW-A for shutting off the latchup current.

Under the state of normal operation, the current through the resistor R is quite small, so that the voltage drop on the resistor R is negligible. Thus, the input stage, connected to VDD through the resistor R, of the inverter INV is biased at a “high” state. This makes the gate of the PMOS transistor biased at a “low” state, so that the PMOS is turned on and a good “1” voltage state is passed to pin3, the power supply node of the internal circuit. On the other hand the ground node (pin4) of the internal circuit, is connected to the ground bias node (pin5) through the NMOS transistor Mn1 of the current mirror. Since the dimension of the Mn1 can be enlarged enough to reduce the voltage drop of V_{gs} of Mn1, so that the ground (pin5) can pass a good “0” voltage state to the ground node (pin4) of internal circuit. Thus, the core circuit can normally operate with the desired circuit functions.

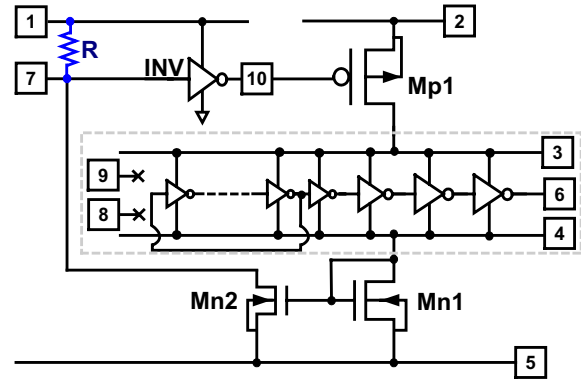


Fig. 2 A circuit implementation for the proposed latchup current self-stop methodology.

When the parasitic SCR path is triggered into the state of latchup, a large current would appear on the path from VDD to VSS through Mp1, ring oscillator, and Mn1. This large current would be mapped to the Mn2 and resistor R by the current mirror of Mn1 and Mn2. The voltage drop across the resistor R is increased tremendously by the mapped large current. This large voltage drop makes the state of the inverter INV changed, and then the PMOS switch of Mp1 is turned off. After the PMOS switch is turned off, the large latchup current flowing from VDD to VSS through the parasitic SCR is shut off, and the latchup phenomenon is removed. At the same time, as the current is shut off, the voltage drop on the resistor R is decreased to zero, so that the output state of the inverter INV is changed into a “low” state and the PMOS is turned on again. It means that the core circuit block is auto-reset and back to its normal circuit operation again.

4. EXPERIMENT RESULTS

In order to verify the proposed methodology and the designed circuit shown in Fig. 1 and Fig. 2, respectively, a silicon test chip has been fabricated in a 0.5- μm 1P3M bulk CMOS process for experimental test.

To verify the holding voltage of the core circuit block, pin3 and pin4 of the ring oscillator as indicated in Fig. 2 are connected to Tek370 curve tracer directly. The measured I-V curve is shown in Fig. 3, which indicates that the holding voltage is only 1.9V. As the holding voltage is smaller than the VDD power supply voltage (5V), the parasitic SCR is inherently sensitive to the external trigger source.

To ensure the ring oscillator is functional normally, a voltage power supply of 5V is applied between the pin3 and the pin4 of Fig. 2. The voltage waveforms of the ring oscillator output stage and the VDD power supply are measured and shown in Fig. 4. It is clear that the ring oscillator can normally operate.

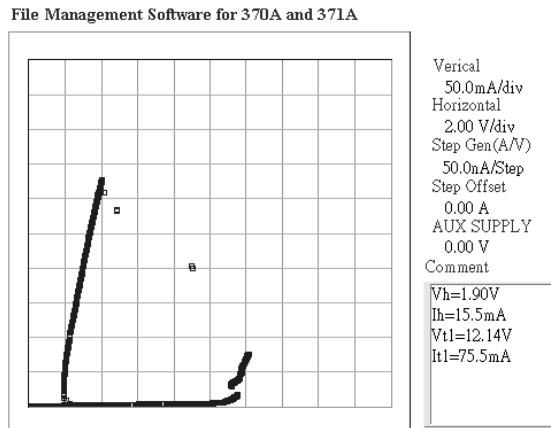


Fig. 3 The I-V characteristics of the parasitic SCR in the ring oscillator, which is measured by Tek370 curve tracer.

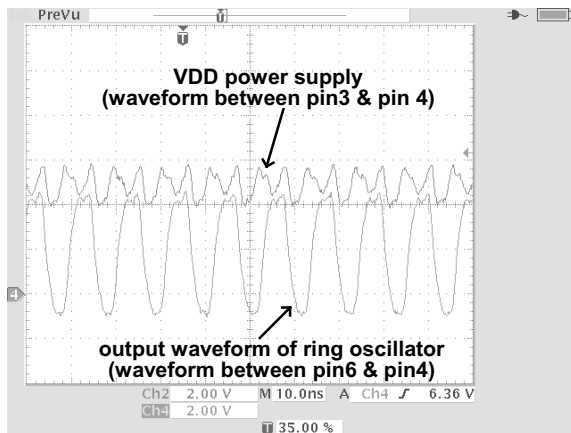
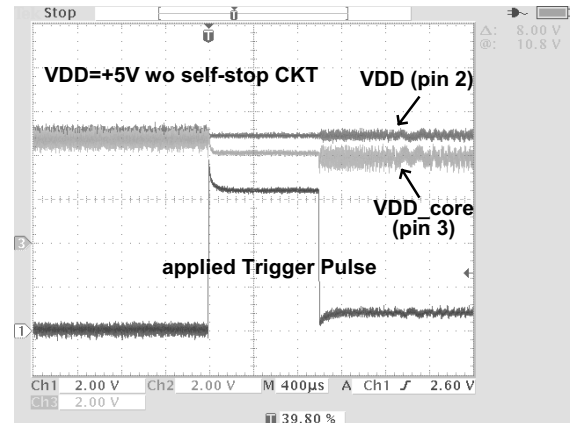


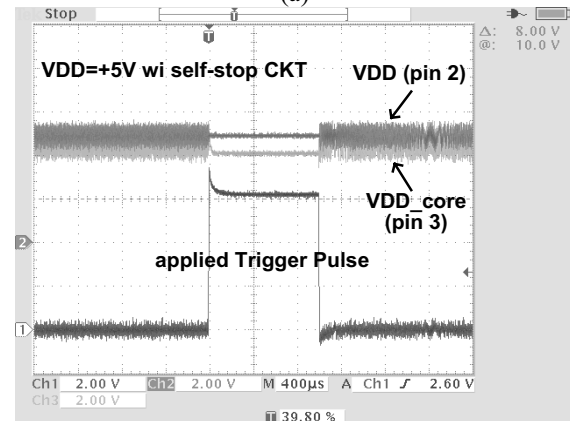
Fig. 4 The monitored voltage waveforms of the ring oscillator in time domain. The ringing one is the output stage waveform, and the upper one is the VDD power supply.

The rest parts of the designed circuit shown in Fig. 2 are the current mirror as a current extractor, resistor as a current-voltage converter, inverter on the feedback network, and PMOS as a switch to turn off the latchup current. Except the resistor R, the other parts are all implemented on the silicon test chip, and verified to be functional when they are normally operated with a VDD level of 5V. The resistor R, connected between pin1 and pin7, is implemented by a discrete resistor in this experiment. It is verified that the resistance value of the used discrete resistor is with less than 3% variation after a 100mA DC current flowing through it for over 10 minutes. It indicates that the used discrete resistor can be treated as a constant value resistor when processing the experiments. For on-chip application, this resistor can be implemented by a poly resistor, a n-well resistor, or a diffusion resistor in CMOS IC's.

When processing function test of the designed circuit shown in Fig. 2, pin1 and pin2 are connected together and applied with varied VDD levels of power supply. Pin10 is optionally connected to system ground to disable the function of the latchup prevention circuit.



(a)



(b)

Fig. 5 The voltage waveforms of the external and internal core VDD when a trigger pulse is applied on the parasitic latchup sensitive SCR path. The external supplied VDD is 5V in this figure. After the pulse triggering, the core VDD is latched at 4V in (a) when the latchup prevention circuit is disabled, and not changed in (b) when the latchup prevention circuit is normally operated.

The measured waveforms of the proposed circuit for latchup prevention with a VDD power supply of 5V are shown in Fig. 5. For the waveforms shown in Fig. 5(a), pin10 is connected to system ground to turn on the PMOS switch, Mp1. This makes the function of latchup prevention circuit disabled, and makes the internal circuit to be latched much easier when the trigger pulse is applied. In Fig. 5(a), voltage levels of external and internal core VDD are almost the same before the trigger pulse is applied. However, after the trigger pulse is applied, voltage level of the internal core VDD is lowered down and latched at about 4V when the function of the proposed

latchup prevention circuit disabled. In Fig. 5(b), pin10 of Fig. 2 is not connected to ground, so that the latchup prevention circuit is enabled. Under this condition, voltage level of the internal core circuit (pin3) is kept at the same level before and after the trigger pulse is applied. Therefore, the core circuit can be really free from latchup with the help of the latchup prevention circuit.

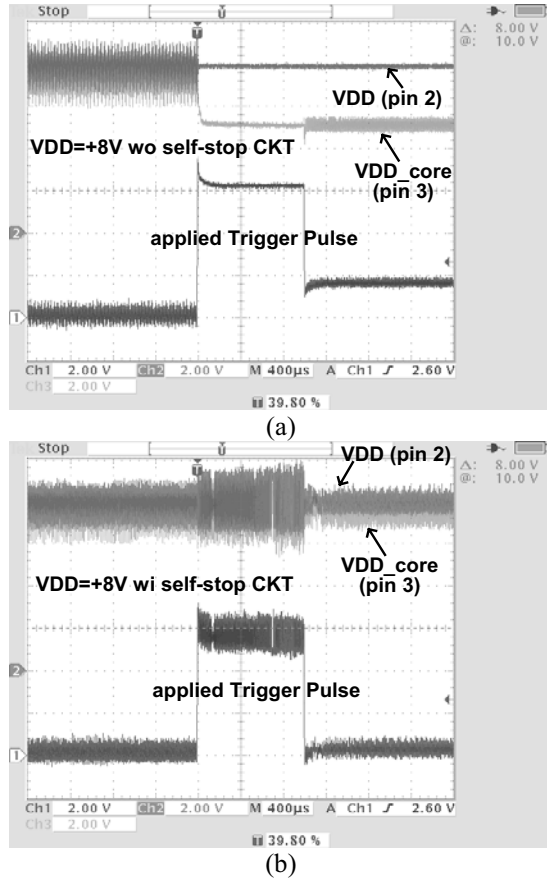


Fig. 6 The voltage waveforms of the external and internal core VDD when a trigger pulse is applied on the parasitic latchup sensitive SCR path. The external VDD is further increased to 8V in this figure. After the pulse triggering, the core VDD is latched at 5V in (a) when the latchup prevention circuit is disabled, and not changed in (b) when the latchup prevention circuit is normally operated.

In order to ensure the latched voltage level in Fig. 5 is due to the sum of the parasitic SCR holding voltage and the V_{DS} of the current mirror, a higher voltage level VDD power supply is chosen. The measured waveforms of the proposed circuit for latchup prevention with a VDD power supply of 8V are shown in Fig. 6. It is clear that the results of the measured waveforms have a little higher latched voltage level, as compared with the ones shown in Fig. 5. The higher latched voltage level is due to a larger latchup current when the VDD level is increased from 5V to 8V.

5. CONCLUSIONS

A high efficient latchup current self-stop methodology and circuit for whole-chip latchup prevention have been proposed and verified in this paper. By a variety of experiments applied on the silicon test chip, the proposed methodology and designed circuit are proved to meet the requirement of latchup prevention. Except the function to self-stop the latchup current, the core circuit can be auto-reset by the designed circuit. By implementing this simple circuit with only a small layout area, all bulk CMOS IC products can be designed free to latchup damage.

6. REFERENCES

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