ON-CHIP ESD PROTECTION CIRCUIT DESIGN WITH NOVEL SUBSTRATE-TRIGGERED SCR DEVICE IN SUB-QUARTER-MICRON CMOS PROCESS

Ming-Dou Ker and Kuo-Chun Hsu

Integrated Circuits & Systems Laboratory, Institute of Electronics
National Chiao Tung University, Hsinchu, Taiwan

ABSTRACT

A novel design concept to turn on the SCR device by applying the substrate-triggered method is first proposed in the literature for effective on-chip ESD protection design. To avoid the transient-induced latch-up issue, the substrate-triggered SCR devices are stacked in the ESD protection circuits. The turn-on efficiency of SCR can be greatly improved by applying the substrate-triggered method. The on-chip ESD protection circuits designed with the substrate-triggered SCR devices for input pad, output pad, and power pad have been successfully verified in a 0.25-μm CMOS process. The substrate-triggered SCR device with a smaller layout area of only 40μm×20μm can sustain the HBM ESD stress of higher than 7kV.

1. INTRODUCTION

To provide effective electrostatic discharge (ESD) protection for CMOS IC's, the on-chip ESD protection circuits have to be added around the input, output, and power pads of the CMOS IC's. The lateral Silicon Controlled Rectifier (SCR) device was therefore used in the input (or output) ESD protection circuits to effectively protect the CMOS IC against ESD damage [1]. Due to the low holding voltage (Vhold, about ~1V in general CMOS processes) of SCR device, the power dissipation (Power ≅ I_{ESD}×Vhold) located on the SCR device during the ESD stress is less than that located on the other ESD protection devices (such as the diode, MOS, BJT, or field-oxide device) in CMOS technology. Therefore, the SCR device can sustain a much higher ESD level within smaller layout area in the CMOS IC's. But, the SCR devices often have a higher trigger voltage (~20V) in the sub-quarter-micron CMOS technology, which is generally greater than the gate-oxide breakdown voltage of the input stages. Therefore, the SCR devices need the additional secondary protection circuit to perform the overall ESD protection function [1]. To provide more effective on-chip ESD protection, the modified lateral SCR (MLSCR) [2] and the low-voltage-trigger SCR (LVTSCR) [3]-[4] had been invented to reduce the trigger voltage of the SCR devices. Moreover, some advanced circuit techniques [5]-[7] had been also reported to improve ESD level of the ESD protection devices.

In this paper, the on-chip ESD protection circuits designed with the novel substrate-triggered SCR (STSCR) devices for input pad, output pad, and power rails are proposed and verified in a 0.25-μm CMOS process. Such STSCR devices are designed to be kept off during the normal circuit operating condition, and to be quickly triggered on during the ESD-zapping condition.

2. CHARACTERISTICS OF SUBSTRATE-TRIGGERED SCR (STSCR) DEVICE

The device structure of the traditional lateral SCR device is shown in Fig.1, where the anode (P+ diffusion) of SCR is connected to a pad and the cathode (N+ diffusion) is grounded in a P-substrate CMOS process. The trigger voltage of such a lateral SCR device is depended on the breakdown voltage of the N-well to P-substrate junction, which is about ~20V in a 0.25-μm CMOS process. The proposed STSCR device structure is shown in Fig.2, where the SCR current paths are indicated by the dashed lines. As comparing to the traditional lateral SCR device structure, an extra P+ diffusion is inserted into the STSCR device structure as the trigger node. The inserted P+ diffusion is connected out as the trigger node of the STSCR device. When a trigger current is applied into the trigger node, the STSCR will be triggered on into its latch state. The additional N-well regions under the cathode (N+ diffusion) of the STSCR device is used to further enhance the turn-on speed of the STSCR for effective ESD protection purpose.

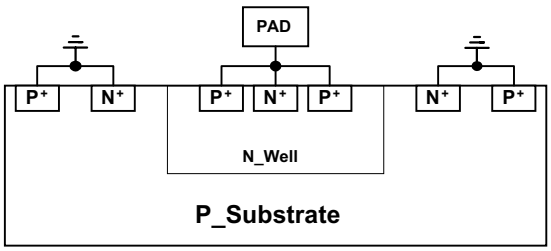


Fig.1 Device structure of the traditional lateral SCR device.

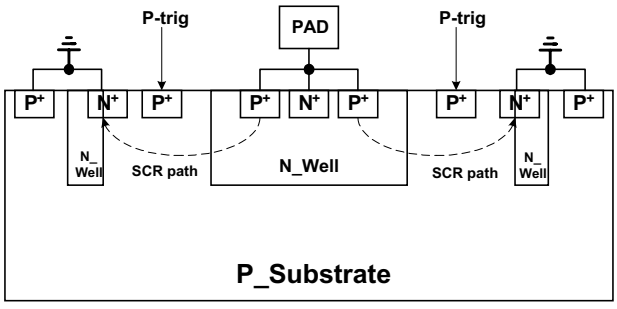
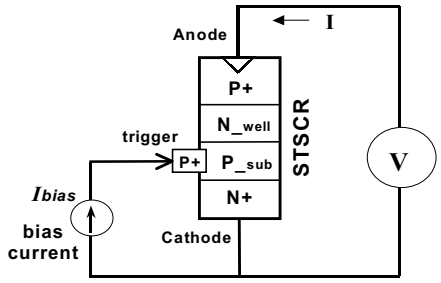
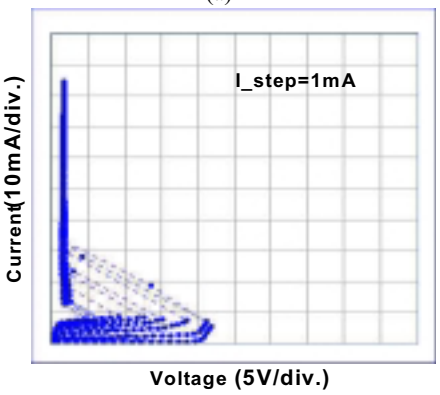


Fig.2 Device structure of the proposed STSCR device.

Such a STSCR device has been drawn in layout and fabricated in a 0.25-μm CMOS process. The experimental setup to measure the I-V characteristics of the STSCR device is illustrated in Fig.3(a), and the measured results are shown in Fig.3(b). The trigger current that applied into the trigger node has a step of 1mA in Fig.3(b). When the STSCR device has no substrate-triggered current (Ibias=0), the STSCR is turned on by its N-well to P-substrate junction breakdown. In Fig.3(b), the switching voltage of the fabricated STSCR device is as high as 22V, when the substrate-triggered current is zero. But, the switching voltage of the fabricated STSCR device is reduced to only 9V, when the substrate-triggered current is 5mA. Moreover, the switching voltage of the fabricated STSCR device is reduced to only 1.85V, which almost equals to the holding voltage (~1.35V) of the STSCR, when the substrate-triggered current is increased to 8mA. So, the STSCR can be triggered on by applying the trigger current into this trigger node. The dependence of the switching voltage of the STSCR device on the substrate-triggered current is shown in Fig. 4. The higher the substrate-triggered current leads to a much lower switching voltage in the STSCR device.



(a)



(b)

Fig.3 (a) The experimental setup used to measure the I-V curves of the STSCR device, and (b) the measured I-V curves of the STSCR device.

With a lower switching voltage in the STSCR device, the turn-on speed of STSCR device can be further improved to quickly discharge the ESD current. This is a very excellent feature of this STSCR device for using in the on-chip ESD protection circuits. However, another issue of using the SCR device as the ESD protection device is the transient-induced latch-up concern [8], when the IC is under normal circuit operation. Therefore, the total holding voltage of the ESD protection circuit with the SCR devices must be designed greater than the maximum voltage level of VDD in the normal circuit operating condition to avoid the latch-up issue. This can be achieved by stacking the STSCR devices in the ESD protection circuits. Fig. 5 shows the dependence of the total holding voltage on the temperatures of the STSCR devices with different number of stacked STSCR devices. The total holding voltage will become smaller when the operating temperature is increased, because the current gain (β) of the parasitic bipolar transistor in the SCR device is increased with the increase of operating temperature. But, the total holding voltage can be still raised up by increasing the number of the stacked STSCR devices. Such stacked STSCR devices can be simultaneously triggered on, when the trigger currents are simultaneously applied into the trigger nodes of the STSCR devices.

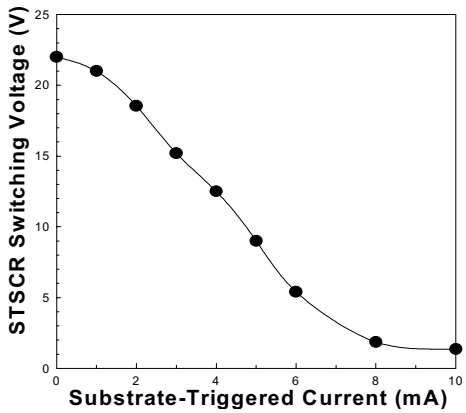


Fig.4 Dependence of the switching voltage of the STSCR on the substrate-triggered current in the STSCR device.

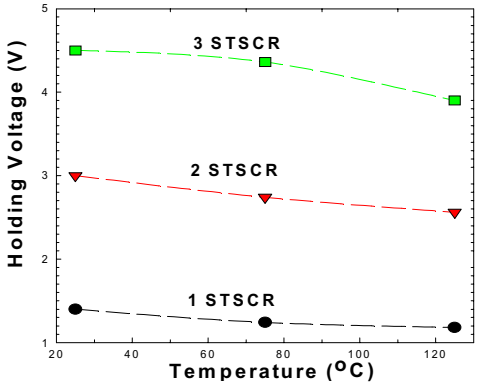


Fig.5 The temperature dependence on the total holding voltage of the stacked STSCR devices with different stacked number.

3. ON-CHIP ESD PROTECTION DESIGN

3.1 ESD Protection Design for the Input/Output Pads

The ESD protection circuits for input and output pads, realized with the stacked STSCR devices, are shown in Figs. 6(a) and 6(b). All the p-trigger nodes of the stacked STSCR

devices are connected to the output of the ESD-detection circuit, which is formed with a resistor and an inverter. The input of the inverter is connected to VDD through the resistor R. The resistor R is better realized by using the diffusion resistance for the concern of antenna effect [9]. A capacitor C is placed between the input of the inverter and VSS. This capacitor can be formed by the parasitic capacitance at the input node of the inverter. In the normal circuit operating condition with VDD and VSS power supplies, the input of the inverter is kept at VDD. Therefore, the output of the inverter is biased at VSS due to the turn-on of NMOS in the inverter. The p-trigger nodes of the stacked STSCR devices are biased at VSS by the output of the inverter, so the stacked STSCR devices are guaranteed to be kept off in the normal circuit operating condition.

When the positive-to-VSS ESD stress zapping on the pad, the input of the inverter is initially kept at zero, and the inverter is biased by the ESD energy on the pad. The RC in the ESD-detection circuit is designed to keep the input of inverter with a relative low voltage level during the ESD stress condition. Thus, the output of the inverter is charged up to high by the ESD energy to generate the trigger current into the p-trigger nodes of the stacked STSCR devices. Therefore, the STSCR devices are turned on by the trigger current generated from the inverter output, and the ESD current is discharged from the pad to VSS through the stacked STSCR devices.

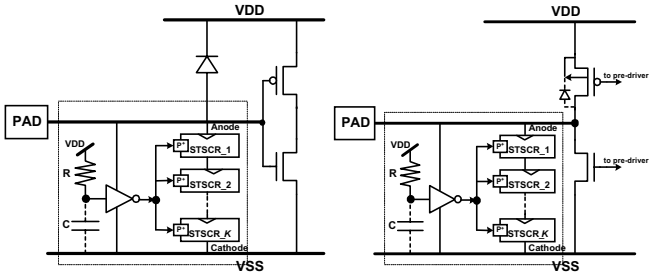


Fig.6 The ESD protection circuits for the (a) input pad, and (b) output pad, by using the proposed STSCR devices in stacked configuration.

3.2 ESD Protection Design for the Power Rail

The STSCR device can be also applied to design the power-rail ESD clamp circuits. The VDD-to-VSS ESD clamp circuit realized with the stacked STSCR devices is shown in Fig.7. The number of the stacked STSCR devices between the VDD and VSS power rails is dependent on the maximum voltage level between the VDD and VSS in the normal circuit operating condition to avoid the latch-up issue. The function of the ESD-detection circuit is similar to the ESD-detection circuit used in the I/O pads, but the RC is designed with a time constant of about ~1μs to distinguish the VDD power-on event (with a rise time of ~ms) or ESD-stress events (with a rise time of ~ns). During normal VDD power-on transition (from low to high), the input of the inverter in Fig.7 can follow up in time with the power-on VDD signal, so the output of the inverter is kept at zero. Hence, the stacked STSCR devices are kept off and don't interfere the functions of internal circuits.

When a positive ESD voltage is applied to the VDD pin with the VSS pin relatively grounded, the RC delay will keep the input of the inverter at a low voltage level for a long time, therefore the output of the inverter will become high to trigger the stacked STSCR devices. While the stacked STSCR devices are triggered on, the ESD current is discharged from VDD to VSS through the stacked STSCR devices. By suitable design on the ESD-detection circuit, the stacked STSCR devices can be quickly triggered on to discharge the ESD current.

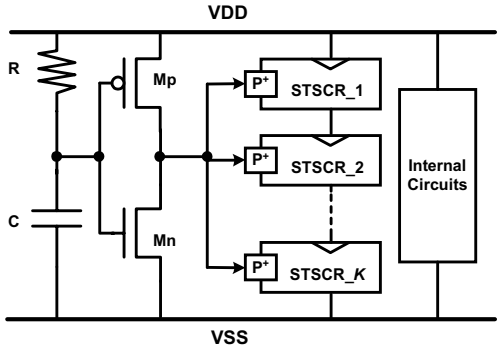


Fig.7 The VDD-to-VSS ESD clamp circuit realized with the stacked STSCR devices.

4. EXPERIMENTAL RESULTS

The proposed ESD protection circuits have been designed with different number of stacked STSCR devices and fabricated in a 0.25-μm CMOS process. The human-body-model (HBM) and machine-model (MM) ESD stresses are applied to the ESD protection circuit to verify the ESD robustness of the design shown in Fig.7. The ESD test results are compared in Fig.8. Because the total holding voltage of the stacked configuration between the VDD and VSS power rails is increased with the number of the stacked STSCR devices, the HBM and MM ESD levels of the ESD protection circuit is decreased with the increase on the number of the stacked STSCR devices. However, it is still high enough for ESD protection. If the ESD protection circuit is realized with 3 stacked STSCR devices for 3-V IC applications, the HBM (MM) ESD robustness is as high as 7.5kV (725V), where each STSCR device is realized with a layout area of only 40μm×20μm in the 0.25-μm CMOS process. This has verified the excellent area-efficiency of the ESD protection circuits realized with the proposed stacked STSCR devices.

In order to investigate the turn-on efficiency of the ESD protection circuit realized with the stacked STSCR devices, a voltage pulse with a pulse width of 400ns and a rise time of 10ns is applied to the VDD of Fig.7. First, one stand-alone STSCR device without ESD-detection circuit is tested. The STSCR cannot be triggered on until the pulse

height of the applied voltage pulse is increased up to 20V. After the triggering on, the voltage level on the VDD line is clamped to ~2.4V. The voltage waveform on the VDD line, clamped by the stand-alone STSCR device without ESD-detection circuit, is measured and shown in Fig.9. Because of the internal output resistance of the pulse generator and the turn-on resistance of the STSCR device, the clamped voltage (~2.4V) is greater than the holding voltage (~1.35V) of a STSCR device measured in Fig.3.

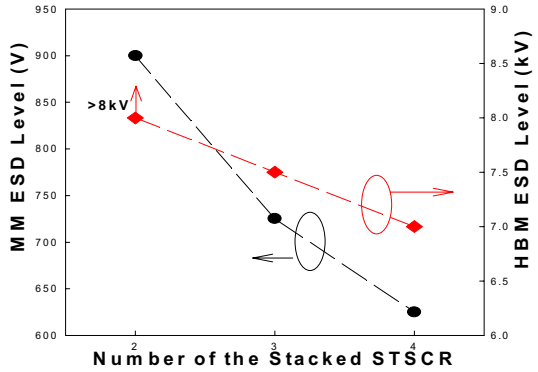


Fig.8 Dependence of HBM and MM ESD levels on the number of the stacked STSCR devices.

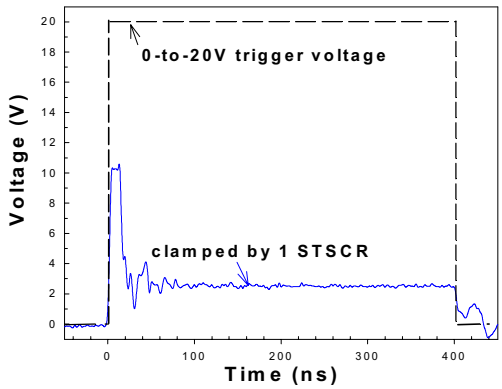


Fig.9 The measured voltage waveform on the VDD line, clamped by the stand-alone STSCR device without ESD-detection circuit, when a 0-to-20V voltage pulse is applied to the VDD line with the VSS grounded.

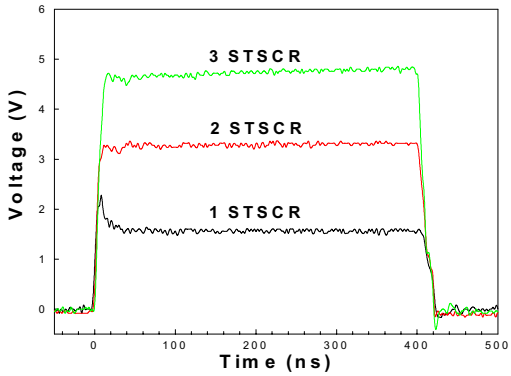


Fig.10 The measured voltage waveforms at the VDD line clamped by the ESD protection circuit with ESD-detection circuit and different number of stacked STSCR devices.

On the contrary, even if the ESD protection circuit designed with multiple stacked STSCR devices, the voltage pulse with a smaller pulse height can trigger on the ESD protection circuit if there is the ESD-detection circuit. In Fig.10, a 0-to-5V voltage pulse waveform applied on the VDD line is clamped to 1.6V (3.2V) by the ESD protection circuit with one (two) stacked STSCR devices and the ESD-detection circuit. A 0-to-8V voltage pulse, applied to the ESD protection circuit with three stacked STSCR devices and ESD-detection circuit, is clamped to ~4.7V in Fig.10. When the voltage pulse is applied to the VDD pin, the voltage pulse is quickly clamped to a low voltage level within several ns. This has successfully verified the turn-on speed of the proposed STSCR devices to fast discharge the ESD transient current of ESD events. The clamped voltage level of the ESD protection circuit can be linearly adjusted by changing the number of stacked STSCR devices for practical applications in CMOS IC products with different VDD voltage levels.

5. CONCLUSION

ESD protection circuits, designed with the substrate-triggered SCR devices in stacked configuration, have been successfully verified in a 0.25-μm CMOS process. The ESD protection circuits with the stacked STSCR devices and ESD-detection circuit have the advantages of low switching voltage, low holding voltage, fast turn-on speed, occupied smaller layout area, and a much higher ESD robustness, which are very useful in CMOS IC products fabricated in sub-quarter-micron CMOS processes.

6. REFERENCES

[1] R. Rountree, "ESD protection for submicron CMOS circuits : issues and solutions," in *IEDM Tech. Dig.*, 1988, pp.580-583.

[2] C. Duvvury and R. Rountree, "A synthesis of ESD input protection scheme," *Proc. of EOS/ESD Symp.*, 1991, pp.88-97.

[3] A. Chatterjee and T. Polgreen, "A low-voltage triggering SCR for on-chip ESD protection at output and input pads," *IEEE Electron Device Letters*, vol.12, pp.21-22, 1991.

[4] M.-D. Ker, *et al.*, "Complementary-LVTSCR ESD protection scheme for submicron CMOS IC's," *Proc. of . IEEE Int. Symp. on Circuits and Systems*, 1995, pp.833-836.

[5] M.-D. Ker, H.-H. Chang, and C.-Y. Wu, "A gate-coupled PTLSCR/ NTLSCR ESD protection circuit for deep- submicron low-voltage CMOS IC's," *IEEE Journal of Solid-State Circuits*, vol.32, pp.38-51, 1997.

[6] M.-D. Ker, T.-Y. Chen, and C.-Y. Wu, "ESD protection design in a 0.18-μm salicide CMOS technology by using substrate-triggered technique," *Proc. of IEEE Int. Symp. on Circuits and Systems*, 2001, vol. 4, pp. 754-757.

[7] M.-D. Ker, *et al.*, "Novel input ESD protection circuit with substrate-triggering technique in a 0.25-μm shallow-trench-isolation CMOS technology," *Proc. of IEEE Int. Symp. on Circuits and Systems*, 1998, vol.2, pp. 212-215.

[8] G. Weiss and D. Young, "Transient-induced latchup testing of CMOS integrated circuits," *Proc. of EOS/ESD Symp.* 1995, pp. 194-198.

[9] S. Krishnan and A. Amerasekera, "Antenna protection strategy for ultra-thin gate MOSFETs," *Proc. of IEEE Int. Symp. on Reliability Physics*, 1998, pp.302-306.