Design of Negative Charge Pump Circuit with Polysilicon Diodes in a 0.25-μm CMOS Process

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ABSTRACT

A charge pump circuit realized with the substrate-isolated polysilicon diode in the 0.25-μm CMOS process is proposed. With the polysilicon diode, the stable negative voltage generation can be realized in general sub-quarter-micron CMOS process without extra process modification or additional mask layer. The device characteristic of polysilicon diode and the voltage waveforms of the negative charge pump circuit have been successfully verified in a 0.25-μm CMOS process with grounded p-type substrate.

Keywords

Polysilicon diode, charge pump circuit.

1. INTRODUCTION

Charge pumps circuits have been widely used in CMOS ICs, such as the nonvolatile memories [1], DRAM [2], low-voltage circuits [3], low-voltage phase-locked loop [4]-[5], and the RS232 series bus of personal computer. Conventional charge pumps use the MOS intended to operate as diode. Due to the body effect, the output voltage of the MOS charge pump circuit is often lower than that of the pure diode charge pump circuit. To reduce the threshold voltage of MOS in the chain, some schemes had been reported [6]-[10]. However, in the low-voltage operation with VDD below 1.8V, the conventional MOS charge pump circuits demand more stages than the pure diode charge pump circuit. To overcome the body effect in low-voltage operation, the P-N junction diode was used in charge pump circuits again. However, in the typical CMOS process with p-type substrate, the N-well cannot be negative because the p-substrate is grounded. Neither the P-N junction diode nor the MOS diode is good enough for charge pump circuit in low-voltage operation. Moreover, if the circuit needs to generate a negative voltage in CMOS IC with a positive VDD and 0-V VSS, such a negative voltage cannot be generated and stored in any diffusion junction with the common grounded p-substrate.

In this paper, a novel diode structure has been successfully realized in the polysilicon layer of a 0.25-μm CMOS process with grounded p-substrate. Such a polysilicon diode is fully process-compatible to general sub-quarter-micron CMOS processes without extra mask and additional process step. The anode and cathode of the proposed polysilicon diode are fully isolated to common p-substrate, therefore the negative voltage can be pumped from the simple diode-capacitor pump circuit. The generated negative voltage can be stored between the polysilicon diodes and capacitor without interference from the grounded p-substrate of the CMOS ICs.

2. POLYSILICON DIODE

In the sub-quarter-micron CMOS processes, the gate electrode materials of PMOS had been changed to p-type polysilicon because of work function consideration and short channel effects, but the NMOS still uses the n-type polysilicon [11]. To form different types of gate electrodes, the CMOS process changes to form intrinsic polysilicon layer first, and then dopes n-type or p-type impurities into polysilicon layer. Therefore, forming a diode with the p-n junction in polysilicon layer becomes practicable.

The device structure of polysilicon diode, as shown in Fig. 1, is a polysilicon layer including a p-type and an n-type highly doping regions. The whole polysilicon layer is disposed over a gate oxide layer. Under the oxide layer, a shallow-trench-isolation (STI) layer is located on silicon substrate. In terms of manufacturing process, an intrinsic polysilicon layer is deposited after gate oxide growing. Then, the p-type (n-type) highly doping region on the polysilicon is doped with the same process step of PMOS (NMOS) source/drain implantation. Therefore, the proposed polysilicon diode is fully process-compatible to general CMOS processes without extra process modification. Because of the polysilicon diode has no p-n junction in the common substrate, the polysilicon diode can keep the positive or negative voltage isolating from the common substrate. In the polysilicon diode, an additional un-doped center region is located between the p-type and the n-type highly doping regions. The length of the center region, Lc, of the polysilicon diode can affect the device I-V characteristics. To examine the polysilicon diode device, test chips had been fabricated in a standard salicided 0.25-

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μm CMOS process. The photography of a fabricated polysilicon diode is shown in Fig. 2.

The measured I-V curves of the fabricated polysilicon diodes with different spacings of the center region (between N+ and P+ regions) under forward-biased and reverse-biased conditions are shown in Fig. 3, where the length Lc is changed from 0.25 ~ 1.5μm. The dependence of the cut-in voltage (defined with 1-μA forward-biased current) on the length of center region (Lc) is shown in Fig. 4. When Lc increases from 0.25 to 0.7 μm, the cut-in voltage of polysilicon diode increases from 0.46 to 0.6 V. When Lc is longer than 0.7 μm, the cut-in voltage of polysilicon diode keeps in the range between 0.5 to 0.6 V.

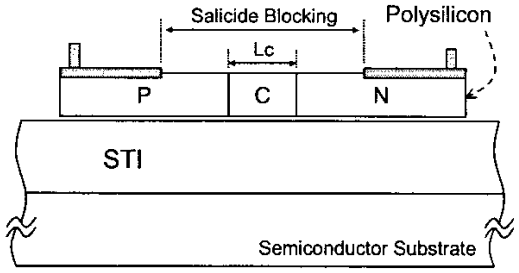

Figure 1 The device cross-sectional view of polysilicon diode.

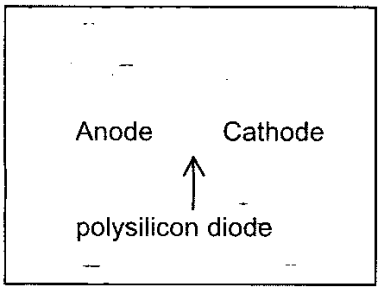

Figure 2 The photography of a fabricated polysilicon diode in a 0.25-μm CMOS process with a junction perimeter of 30μm.

The relation between the length of center region of polysilicon diode and its reverse-biased breakdown voltage is shown in Fig. 5. The breakdown voltage of polysilicon diode increases, when the spacing Lc increases. When Lc equals to 0.7 μm, the breakdown voltage of polysilicon diode equals to 7.7 V (defined at 1-μA reverse-biased current), which is a little smaller than that (8.1 V) of the N+/P-well junction breakdown voltage. When the Lc increases to 1 μm, the breakdown voltage increases to 19.2 V, which is close to the breakdown voltage (18.9 V) of N-well/P-substrate junction. Therefore, the breakdown voltage of a polysilicon diode can be simply adjusted for different applications by only changing the length of center region. Moreover, when the Lc increases to 1.5 μm, the breakdown voltage of polysilicon diode significantly increases to 34.4 V, which is much greater than the breakdown voltage of any p-n junction in sub-quarter-micron CMOS technology.

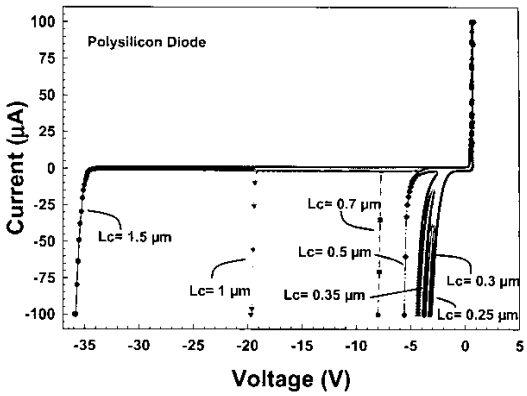

Figure 3 The DC I-V characteristics of polysilicon diode with different length of center region.

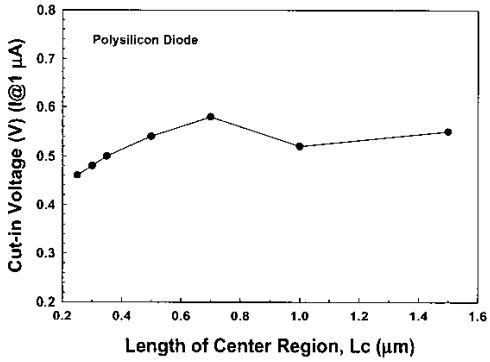

Figure 4 The cut-in voltage of polysilicon diode variation versus different length of center region.

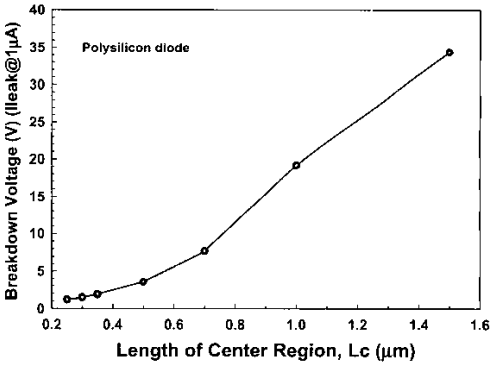

Figure 5 The relation between the length of center region of polysilicon diode and its reverse-biased breakdown voltage.

3. CHARGE PUMP CIRCUIT

Fig. 6 shows the circuit diagram of the proposed negative charge pump circuit. The clock generator, Vs, is used to provide the charge-pump source. The capacitor C1 is used to couple the voltage generated from the charge-pump source to the node A. The diodes PDa and PDb are polysilicon diodes using to pump output voltage, Vout, to be negative. These elements, Vs, C1, PDa, and PDb basically form the negative charge pump circuit. The capacitor C2 is used to keep the Vout stable. The polysilicon diodes PD1, PD2, ., and PDn are used as the voltage regulator to adjust the output negative voltage level. In the steady state, the output voltage of the negative charge pump circuit without the clamping diodes PD1~ PDn can be calculated as

$$Vout = -Vs + Vcutin1 + Vcutin2. \quad (1)$$

Vcutin1 and Vcutin2 are the cut-in voltages of the polysilicon diodes PDa and PDb, respectively. Vs is the voltage amplitude of the clock generator. The output voltage (Vout) can be further clamped by the diode string (PD1 ~ PDn) to the desired negative voltage level.

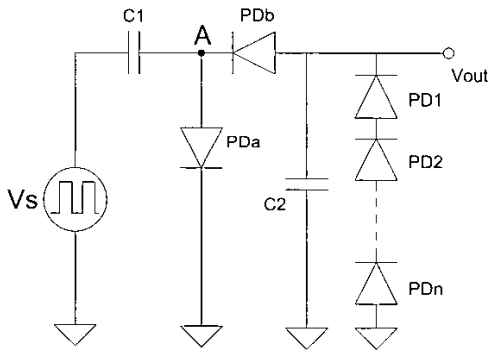

Figure 6 The proposed negative charge pumping circuit with polysilicon diodes.

4. EXPERIMENTAL RESULTS

4.1 Pumping with External Clock Generator

Fig. 7 shows the measured steady-state waveforms of the proposed negative charge pump circuit with a 10-kHz 3-V external clock signal, which is provide by the HP 8110A Pulse Generator. The voltage amplitude of the node A is the same as Vs, but the high voltage of node A is regulated to 0.6 V by the polysilicon diode PDa. The output voltage, Vout, of the negative charge pumping circuit is therefore pumped to –2.4 V.

Fig. 8 shows the measured waveforms under the power-on start-up transition of the proposed negative charge pump circuit with an external clock signal. The Vout can be quickly pumped to negative voltage at the first falling edge of Vs.

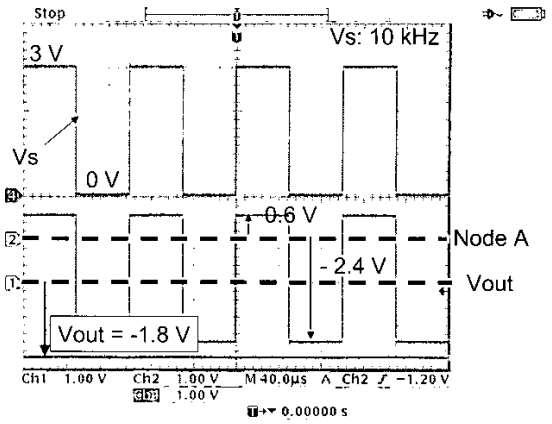

Figure 7 With a 10-kHz 3-V external clock signal, a stable -1.8 V is generated by the proposed charge pump circuit.

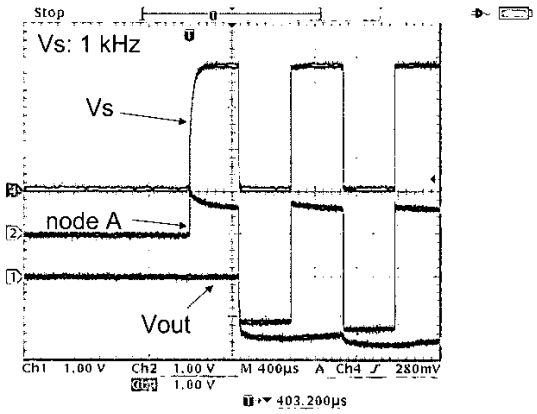

Figure 8 The negative voltage pumping transition of the proposed charge pump circuit in the start-up transition.

4.2 Pumping with On-Chip Clock Generator

An on-chip 101-stage CMOS ring oscillator is also fabricated as the clock signal source of the proposed negative charge pump circuit. Fig. 9 shows the pumping waveform of the charge pump circuit with a rise time of 0.1 ms during the VDD power-on transition. Such VDD is used to supply the 101-stage CMOS ring oscillator. The settling time on Vout defined as the time interval from 10% to 90% of full scale of the output voltage is 2.2 ms. Fig. 10 shows the output waveforms under different rise times of the VDD power-on transition. When the rise time of VDD increase to 1 ms, the settling time increases to 2.6 ms.

Fig. 11 shows the measured voltage waveforms of the negative charge pump circuit when the clamping diode string has two polysilicon diodes. With VDD of 2.5V, the ring oscillator has a voltage swing of 2.5V (V_B in Fig.11). The output voltage (Vout) can be successfully clamped to –1.2V. From those experimental results, including the voltage waveforms measured in time domain, the circuit

performance of the proposed negative charge pump circuit has been successfully verified.

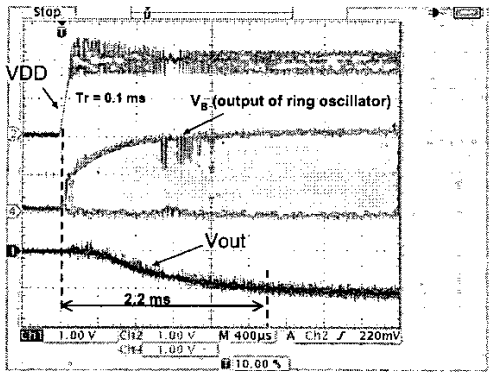

Figure 9 The negative voltage pumping transition of the proposed charge pump circuit during the VDD power-on transition.

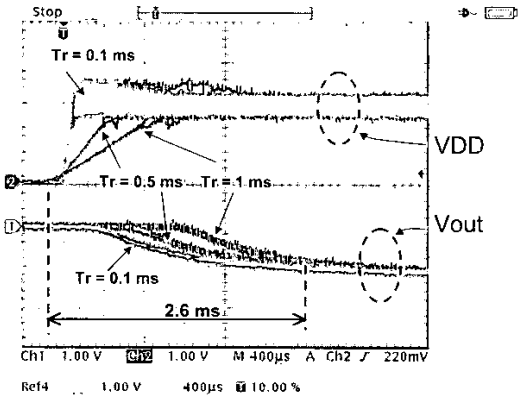

Figure 10 The negative voltage pumping transition of the proposed charge pump circuit during the VDD power-on transition.

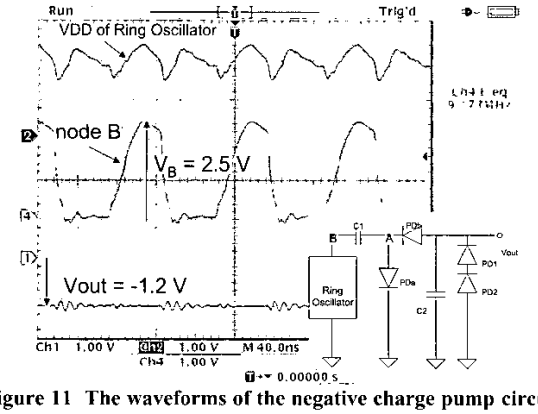

Figure 11 The waveforms of the negative charge pump circuit when the clamping diode string has two polysilicon diodes.

5. CONCLUSION

A negative charge pump circuit realized with the process-compatible polysilicon diodes has been successfully verified in a 0.25-µm CMOS process. The cut-in voltage and breakdown voltage of the polysilicon diode can be adjusted by drawing different spacing on the length of the center region in layout, without any extra process modification. The pumped negative voltage level can be further adjusted by simply changing the number of diodes, which are stacked from the output node to ground. The proposed charge pump circuit can be modified to generate a positive voltage level, which is greater than VDD, for different circuit applications.

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