Design on LTPS p-i-n Diode and its Application for Whole-Panel Electrostatic Discharge Protection

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The secondary breakdown current (It2) of p-i-n diodes under different doping types and spacings in "i" region have been investigated by transmission line pulsing (TLP) system. Using p-i-n as ESD protection device, the successful whole-panel ESD protection of 2.2-inch LTPS TFT-OLED display of the panel-B has been proposed and verified to be more robust than that of the panel-A with traditional NMOS and PMOS ESD protection design. Moreover, the I-V curve shifting and failure analysis with hot-spot pictures explain the failure behavior of the p-i-n diodes under ESD zapping.

1. Introduction

As the time of system-on-panel (SOP) is approaching, ESD reliability issue was not only the upcoming but also a worth-concern problem, when the drivers, controllers, and memories are integrated on a glass substrate. Some papers related to the ESD stress of LTPS TFTs utilizing TLP system had been reported in 1,2). The secondary breakdown characteristics of LTPS TFT devices under gate-driven and substrate-triggered techniques have been investigated by TLP system 3-4). Especially, the measurement results had shown that the DC I-V curve shifting of LTPS TFT MOS structure after negative-to-VSS (NS) mode low-level ESD stress was extremely serious 4), therefore such TFT MOS structure could be unreliable and weak for ESD protection.

To solve NS-mode damages on NMOS structure, the p-i-n diodes are proposed and investigated in this paper. The It2 of p-i-n diodes with different doping types and spacings in the intrinsic area have been measured by TLP system. The panel-B using p-i-n diodes as ESD protection devices has been verified and compared to the panel-A with traditional NMOS and PMOS devices as ESD protection.

2. Fabrication and Structure of LPTS p-i-n Diodes

Fig. 1 shows the layout top-view of the proposed LTPS p-i-n diodes, which were fabricated on glass substrate. Firstly, a buffer oxide and an α-Si:H films were deposited on glass substrate by PECVD system. Next, XeCl excimer laser was used to crystallize α-Si:H film, and then the poly-Si film was patterned. Subsequently, ion doping and activation were carried out to form the p-i-n junction diodes. Moreover, hydrogenation was used to improve device performance. LTPS devices were finished after contact holes and source/drain metal were formed. The layout parameters for ESD consideration are the spacing "S" of "i" region and the doping types of this "i" region, as that shown in Fig. 1.

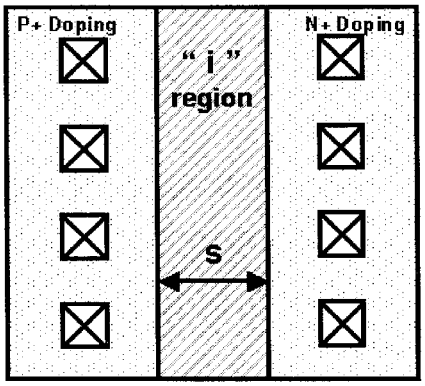


Fig. 1 The layout top-view of the proposed p-i-n diode. The "i" region can be intrinsic or doped with p^-/n^- dopants.

3. It2 of LTPS p-i-n Diodes

The failure criterion was defined as the TLP I-V curve showing an obvious change on its

turn-on resistance or obvious damages on the top-view of devices. The TLP measured I-V curves of the p-i-n diodes with the spacing "S" of "i" region of 5 μm under forward TLP stress were shown in Fig. 2. The layout of the p-i-n diodes is drawn with channel width of 400 μm in multiple-finger style. The p-i-n diode with p^- doping type shows both the smallest turn-on resistance and the highest It2 among such three diodes. Moreover, the p-i-n diode with n^- doping type in "i" region shows irregular TLP I-V curve due to the non-uniform conduction on ESD current path. The It2 of p-i-n diodes under forward TLP stress increases with the dimension "S" shrinking, obviously in n^- doping type of "i" region, as shown in Fig. 3. The proposed p-i-n diodes with p^-/n^- doping in "i" region have higher It2 compared to that with intrinsic doping type, when "S" is smaller than 5μm. This is due to the turn-on resistance is a function of doping concentration and the spacing of "i" region. In such p-i-n diodes, both the spacing "S" and doping type should be a trade-off design between ESD robustness and leakage current consideration. In the previous work 4), the p-i-n diodes under reverse TLP stress are much weaker than that under forward TLP stress. In the whole-panel ESD protection design, the p-i-n diodes were designed to conduct ESD current under forward-bias condition.

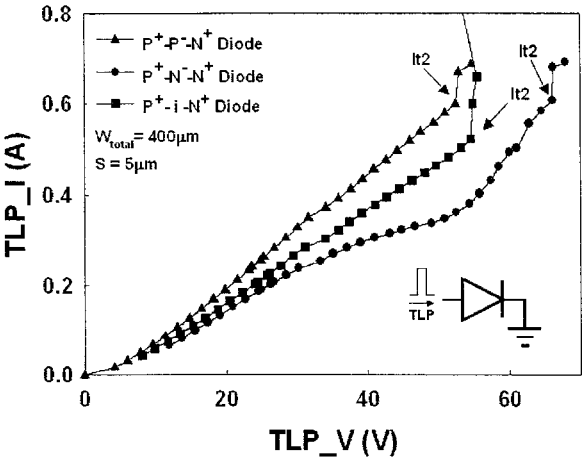


Fig. 2 The TLP measured I-V curves of the proposed p-i-n diodes with different doping types on the center "i" region under forward-bias stress.

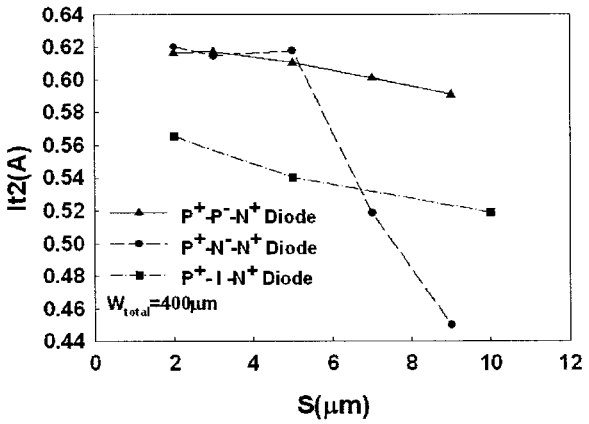


Fig. 3 The relationship between It2 and the spacing "S" of "i" region of the proposed p-i-n diodes with different doping types under forward TLP stress.

4. ESD Protection Designs of Panel-A and Panel-B

The 2.2-inch TFT-OLED panel-A with traditional ESD protection design, which used the Gate-Ground NMOS (GGNMOS) and the Gate-VDD PMOS (GDPMOS) as ESD protection devices to prevent ESD surge from input pad to VDD/VSS, has been shown in Fig. 4. The dimensions (W/L) of GGNMOS and GDPMOS are drawn as 800μm/6μm and 1200μm/6μm, respectively. When the input pad of panel-A is under positive ESD zapping with VSS grounded (the PS mode), ESD current is discharged through only NMOS path by avalanche breakdown, as that shown by dash line in Fig. 4.

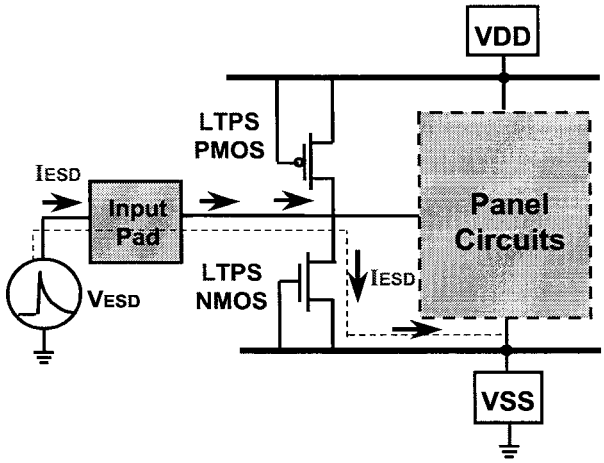


Fig. 4 The traditional ESD protection design of panel-A with GGNMOS and GDPMOS as ESD protection devices.

The successful whole-panel ESD protection design with p-i-n diodes and effective VDD-to-VSS ESD clamp circuit in the panel-B is shown in Fig. 5. The ESD protection diode is drawn with dimension (W/L) of 1246μm/4μm. When positive-to-VSS (PS) mode ESD stress occurs at the input pad, the main ESD current will flow through the path 1 to VDD power line by forward diode, and then the ESD current is discharged through VDD-to-VSS ESD clamp circuit. The other ESD current could be discharged through the path 2 by the diode with avalanche breakdown mechanism. The design spirit of this successful panel-B is to create more low-impedance ESD conducting paths when ESD surge occurs.

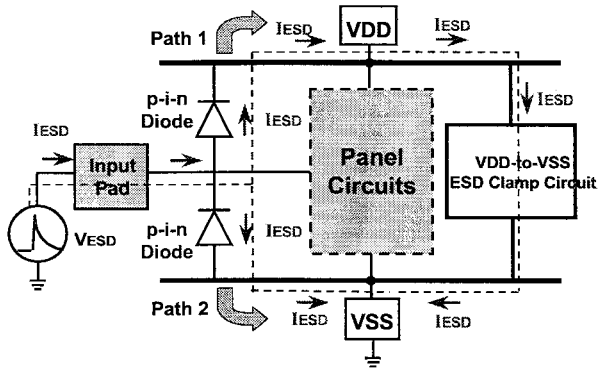


Fig. 5 The ESD protection circuit of panel-B includes the p-i-n diodes and VDD-to-VSS clamp circuit.

The VDD-to-VSS ESD clamp circuit consists of ESD detection circuit and ESD clamp device (M_{ESD}), as that shown in Fig. 6 5). Before ESD zapping, the nodes V_X and V_G have the initial voltage levels the same as that in VSS power line, because the panel is in the floating condition without power supplies. The ESD voltage has a rise time about ~10ns. The voltage level of V_X is increased much slower than the voltage level on the VDD power line, because the RC circuit has a time constant in the order of microsecond (μs). Due to the delay of the voltage increase on the node V_X, the Mp device is turned on by ESD energy and conducts some ESD voltage into the node V_G to turn on M_{ESD}. The turned-on M_{ESD}, which provides a low-impedance path between the VDD and VSS power lines, can clamp ESD voltage across the VDD and VSS power lines. So, the panel circuits can be effectively protected without ESD damages. When the panel is in the normal operating condition with the normal power supplies, the M_{ESD} device has to be kept off to avoid power loss from VDD to VSS.

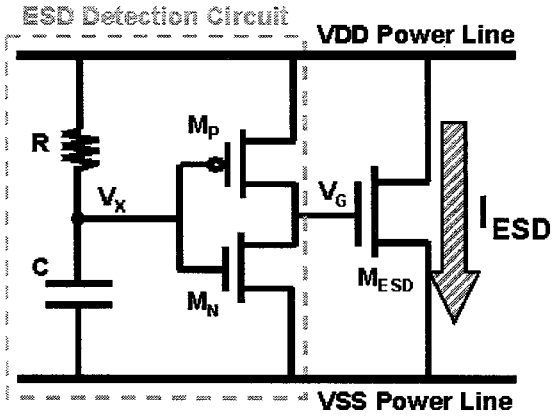


Fig. 6 The circuit diagram of VDD-to-VSS ESD clamp circuit in panel-B.

5. Failure Behavior of Whole-Panel ESD Protection Circuits

Since the portable small sized LTPS TFT panel concerns the power consumption, the definition of failure criteria of whole-panel ESD testing in this work are defined as: (1) the leakage current under normal operating voltage is larger than 1μA, or (2) the obvious failure spots on the top-view of device (physical damages) is formed. Fig. 7 shows the DC I-V curve shifting of p-i-n diode to VSS after NS mode 300V Machine-Model (MM) ESD stress. The failure criterion 1 is used to determine the failure threshold of p-i-n diode in this ESD zapping condition.

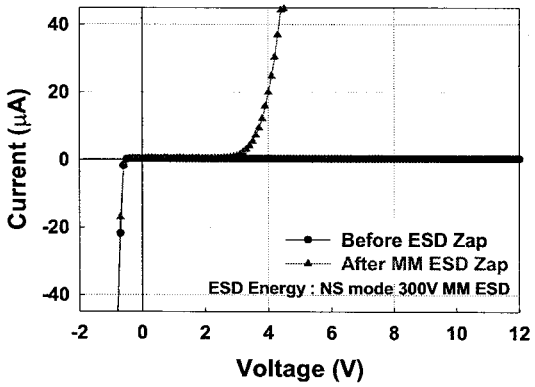
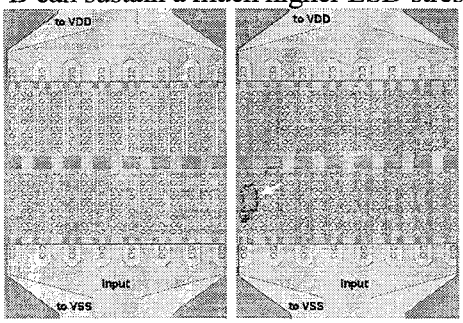


Fig. 7 The DC I-V curve shifting of the ESD protection diode to VSS after NS mode 300V MM ESD stress.

In Fig. 8(a), the failure spots under NS mode 450V MM ESD zapping are almost located on the diode to VSS, which indicates that most of the ESD current under NS mode ESD zapping conducted through the forward-biased diode to VSS. Therefore, a few failure spots are visible on the diode to VDD. In Fig. 8(b), the failure spots under PS mode 475V MM ESD zapping are uniformly distributed on both the p-i-n diode to VDD and the p-i-n diode to VSS, which also indicates that whole-panel ESD protection scheme in panel-B has more ESD conducting paths when ESD surge occurs. Therefore, the panel-B can sustain a much higher ESD stress.



(a) (b)

Fig. 8 The failure spots on the ESD protection diodes under (a) NS mode 450V MM ESD stress, and (b) PS mode 475V MM ESD stress.

6. Comparison of ESD Robustness between Panel-A and Panel-B

Fig. 9 shows the positive-to-VSS (PS), negative-to-VSS (NS), positive-to-VDD (PD), and negative-to-VDD (ND) modes of ESD zapping conditions on an input/output pin. The designed display panel should be tested under at these four modes of ESD zapping conditions on every pin. After ESD testing on all the pins of panel, ESD level of panels should be defined as the worst condition among the four modes of all pins. The maximum sustaining ESD voltages of panel-A and panel-B under four modes MM ESD stresses are compared in Table 1. The NS mode is the worst case among the four modes of ESD zapping in either panel-A or panel-B. In panel-A, ESD stress in PD and ND modes are discharged through GDPMOS, and ESD stress in PS and NS modes are discharged through GGNMOS, because the ESD conduction in panel-A is only with one path. The ESD characteristics of GDPMOS are more robust and reliable than that of GGNMOS, due to the latent damages in GGNMOS device 4). However, ESD robustness of panel-B with the proposed p-i-n diodes and effective VDD-to-VSS ESD clamp circuit has been greatly improved 175% (from 100V to 275V) under the NS-mode ESD stress. The ESD characteristics of the proposed p-i-n diodes are more reliable and robust than that of GDPMOS and GGNMOS. Therefore, the panel-B is a successful whole-panel ESD protection design using the p-i-n diodes and VDD-to-VSS ESD clamp circuit as ESD protection devices.

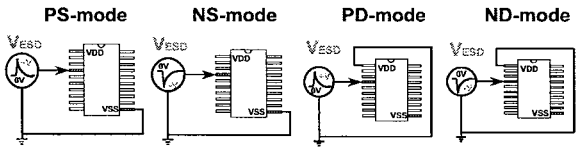


Fig. 9 The ESD zapping conditions include PS, NS, PD, and ND modes on an input/output pin.

Table 1 Comparison on the maximum sustaining pass ESD voltages between the panel-B and panel-A.

	PD	ND	PS	NS
Panel-A (old-design)	350V	275V	250V	100V
Panel-B (new-design)	350V	375V	350V	275V

7. Conclusion

ESD robustness of the p-i-n diodes with different doping types of "i" region has been investigated in this work. According to the ESD characteristics of p-i-n diodes, the diode with p^- doping type in "i" region has a lower turn-on resistance and a higher It2. With good reliability and high ESD robustness of p-i-n diodes, whole-panel ESD protection design with p-i-n diodes and VDD-to-VSS ESD clamp circuit has been verified to be a successful ESD protection design for system-on-panel application.

8. References

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