High ESD Robust TFT Devices with Source-Side Body Contacts for I/O Applications

Ming-Dou Ker[1], Chih-Kang Deng[1], Tang-Kui Tseng[2],
Sheng-Chieh Yang[3], An Shih[3], and Yaw-Ming Tasi[3]

[1] Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics
National Chiao-Tung University, Taiwan, e-mail: mdker@ieee.org

[2] ESD Protection Technology Department, System-on-Chip Technology Center
Industrial Technology Research Institute, Taiwan.

[3] Advanced Technology Research Center, Toppoly Optoelectronics Corporation, Taiwan.

Abstract -- The new structure of Low Temperature Poly-Si (LTPS) Thin-Film-Transistor (TFT) device for ESD protection was proposed in this paper. Different to the conventional TFT devices, the new proposed TFT device employs source-side body contacts (SSBC) structure to improve ESD robustness and to suppress the kink effect. The secondary breakdown current (It2) of the SSBC TFT device has been investigated by measurement with the transmission line pulsing (TLP) system. The experimental results have confirmed that the proposed SSBC TFT device has higher ESD robustness than that of the conventional TFT device.

1. Introduction

LTPS processed poly-Si has been widely used as a material for mobile applications such as the display of digital cameras and notebook computers, because the electron mobility of LTPS TFT device is about 100-times larger than that of the conventional amorphous silicon TFT device. System on panel (SOP), combing memory and controller with driver circuits on a glass substrate, will be the most suitable applications for LTPS TFT device in the near future.[1)] Recently, LTPS TFT technology has been applied to integrate the peripheral driver circuits of Active Matrix Liquid Crystal Display (AMLCD) for cost reduction and power consumption issues. The ESD reliability issue of TFT-LCD system will become more and more serious, when more circuits are integrated on the panel. Some papers related to ESD robustness of LTPS devices had been reported.[2,3)]

In this work, a new LTPS TFT device structure with source-side body contacts (SSBC) is proposed and verified to perform a higher ESD performance for the future system-on-panel integration applications. .

2. Device Structure and Fabrication

The layout top view and the schematic symbol of the proposed SSBC TFT device are shown in Fig. 1. The asymmetrical layout of SSBC TFT device is drawn in finger style with each unit finger width of 50μm. Total width of the SSBC TFT device is 600μm for I/O applications. But, the channel length is varying from 3μm to 15μm in the test panel to verify its impact on ESD robustness. The p^+ body pickup is specially inserted in the source region close to the channel region. A parasitic p^+-p-n^+ diode can be therefore formed in the polysilicon film between source and drain regions.

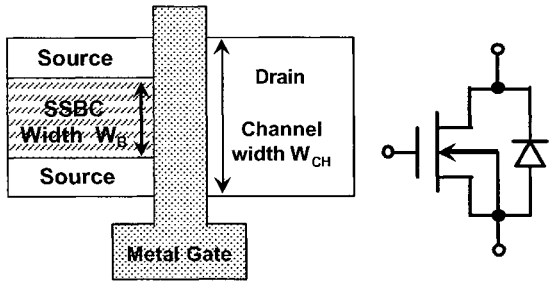


Fig. 1 Layout top view and schematic symbol of LTPS TFT device with source-side body contact.

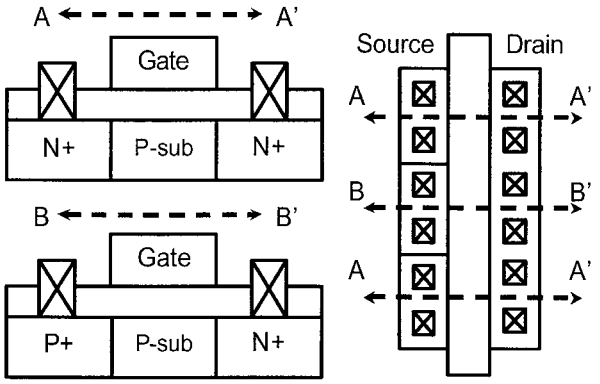


Fig. 2 The cross-sectional views along the AA' and BB' lines on the SSBC device structure.

Fig. 2 shows the cross-sectional views along the AA' and BB' lines on the top view of the proposed SSBC TFT device. The p+ body contact was put at the middle of the source region along the BB' line. Because the source is grounded under normal circuit operation, the extra p+ region in source region does not cause error function to this device.

Without any extra mask, the fabrication of SSBC TFT device is fully comparable to general TFT processes. First, a buffer oxide and α-Si:H films were deposited on glass substrate by PECVD system. Next, XeCl excimer laser was used to crystallize α-Si:H film and then the active region was patterned. Subsequently, ion doping and activation were carried out. TEOS oxide was deposited as gate insulator and followed by gate metal deposition and patterning. LTPS devices were completed after formation of contact holes and metallization. Finally, hydrogenation was used to improve device performance.

3. Measurement Results

The measured transfer characteristics of SSBC TFT device compared to that of the conventional n-type TFT device are nearly the same, as those shown in Fig. 3. The inserted picture in Fig. 3 compares the field effective mobility between the SSBC TFT and the conventional TFT devices. The mobility of SSBC TFT is found to be lower than that of the conventional TFT device due to the reduction of effective channel width. However, the additional p+ body contact in the source region does not degrade device performance too much, when the device operates at high drain and gate voltage.

The kink point of SSBC TFT device compared to that of the conventional TFT is shown in Fig.4. The kink point is determined as the point where the drain conductance starts to increase with the drain voltage.[4] The SSBC TFT device has a higher drain voltage under the same gate voltage due to the hot holes, which are released by body contacts on source side. Therefore, the SSBC TFT device with body contacts has lower kink effect.[5] The devices with longer channel lengths have nearly no difference on kink points because of their less electrical field near the drain. So, the SSBC TFT device has good immunity for kink effect under short channel length.

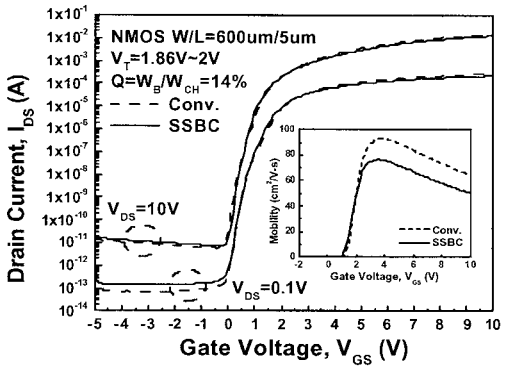


Fig. 3 The transfer characteristics of the conventional and the SSBC LTPS TFT devices.

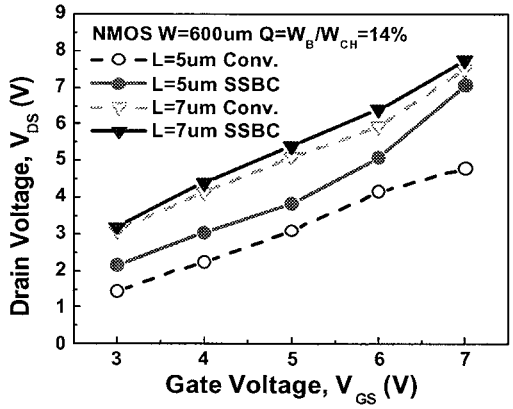
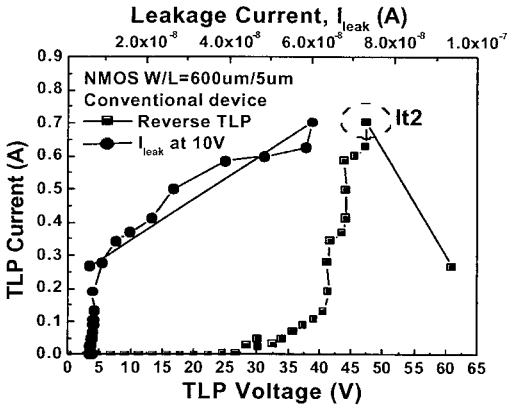
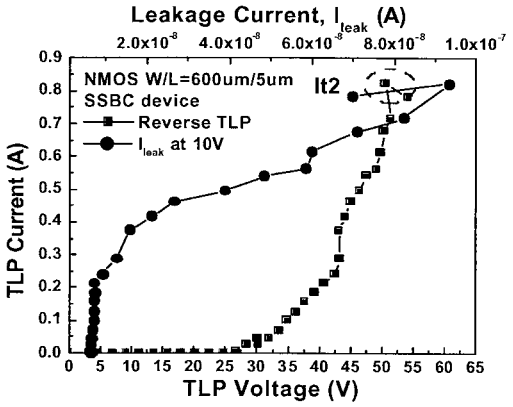


Fig. 4 The kink point for the conventional TFT and the SSBC LTPS TFT devices under different channel lengths.



(a)



(b)

Fig. 5 The TLP I-V curves and leakage currents of (a) the conventional TFT, and (b) the SSBC TFT, devices under reverse TLP stress.

If TLP current was injected from drain to source with the gate of TFT device connected to source, the device was under reverse TLP stress. On the contrary, when the TLP current was injected from source to drain, the device was under forward TLP stress. The TLP measured I-V curves and its related leakage currents of the conventional TFT and the new proposed SSBC TFT devices have been shown in Figs. 5(a) and 5(b), respectively. The failure criteria is defined as the leakage current increasing one order at 10V bias, or the TLP I-V curve obviously shows a negative resistance region. The It2 value is defined as the current at the beginning of the secondary breakdown point with negative resistance. Over the It2 point, the devices were permanently damaged. The relation between It2 and different channel lengths of the SSBC and the conventional TFT devices under reverse TLP stress is compared in Fig. 6. The SSBC TFT device has another reverse diode path to conduct the TLP current. Therefore, the It2 values of SSBC TFT devices are higher than that of the conventional TFT devices.

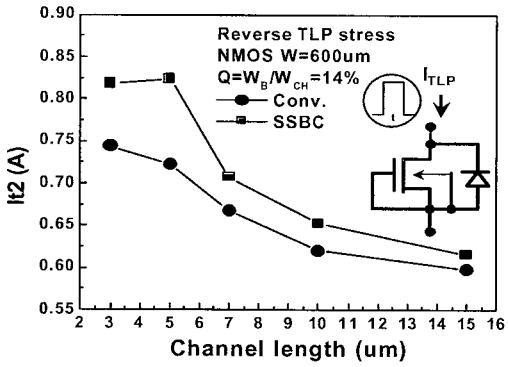


Fig. 6 The dependence of It2 levels on the channel lengths of the conventional TFT and the SSBC TFT devices under reverse TLP stress.

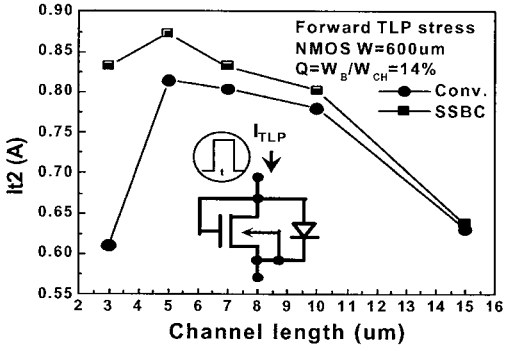


Fig. 7 The dependence of It2 levels on the channel lengths of the conventional TFT and the SSBC TFT devices under forward TLP stress.

The It2 values of the SSBC TFT device compared with that of the conventional TFT device with different channel lengths under forward TLP stress are shown in Fig. 7. The short channel devices have higher It2 values due to lower turn-on resistance. On the other hand, under forward TLP stress, the channel of TFT device is turned on to conduct TLP current, so those have better It2 values compared with those under reverse TLP stress. Moreover, the It2 values of SSBC TFT devices are larger than those of conventional TFT devices due to the

source-side body contact, which creates another diode path under forward TLP stress. This indicates that the SSBC TFT device can sustain higher ESD stress before permanent failure.

The TFT device with L of 3μm under forward TLP stress has the lowest It2 value due to the minimum design rule (L_{min} = 4μm) in our process. Furthermore, the short channel device has very high electrical field near the drain and the insulator under forward TLP stress. A large number of high energy carriers crowding in surface may cause the lowest It2 value in the conventional TFT device with L of 3μm.

After understanding TLP characteristics of SSBC TFT device, the effect of source body contacts is investigated. The source side body percentage Q = W_B/W_{CH}, where the W_B is total source side body width, and the W_{CH} is channel width. In Fig. 8, the SSBC NMOS device with a Q of 14% in source region gains the best It2 value under forward and reverse TLP stresses.

Finally, the conventional TFT device and the new proposed SSBC TFT device are tested by the machine-model (MM) ESD simulator. The dimension (W/L) of the TFT is 600μm/ 5μm with unit finger width of 50μm in the layout. The failure pictures of SSBC TFT device under MM ESD zapping of 275V, and the conventional TFT device under MM ESD zapping of 225V, are shown in Figs. 9 (a) and 9(b), respectively. ESD robustness of SSBC TFT device is more superior to that of conventional TFT device.

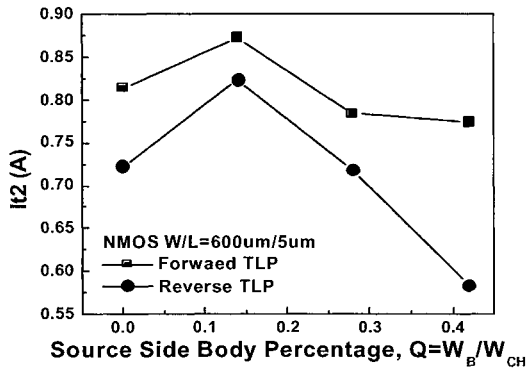
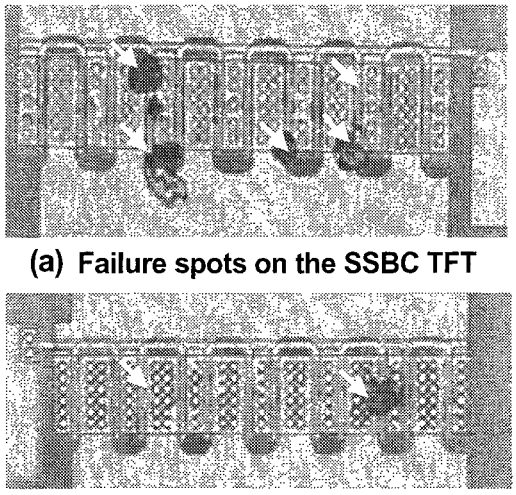


Fig. 8 The dependence of It2 level on the source-side body percentage under forward and reversed TLP stresses.



(a) Failure spots on the SSBC TFT

(b) Failure spots on the conventional TFT

Fig. 9 The failure pictures of (a) SSBC TFT under MM ESD zapping of 275V, and (b) the conventional TFT under MM ESD zapping of 225V.

4. Conclusion

The TLP characteristics of SSBC TFT devices have been investigated in this paper. The experimental results have confirmed that the new proposed SSBC TFT device has higher ESD robustness than that of the conventional TFT device under forward and reverse TLP stresses. Moreover, the SSBC device with a source-side-body percentage Q of 14% achieves better ESD performance. In addition to ESD robustness, the SSBC TFT device can suppress the kink effect, which is a good device for I/O applications in the system-on-panel integration.

5. References

1) Y. Matsueda, S. Inoue, and T. Shimoda, AMLCD 2001 Tech. Dig., (2001) 77.
2) B.-C. Jeon, K.-C. Moon, and S.-C. Lee, ESD/EOS 2002 Symp., (2002) 362.
3) M.-D. Ker, T.-K. Tseng, An Shin, S.-C. Yang, and T.-M. Tasi, AMLCD 2002 Tech. Dig., (2002) 251.
4) M. Koyangi, H. Kurino, T. Hashmoto, H. Mori, K. Hata, Y. Hiruma, T. Fujirmori, I.-W. Wu, and A.-G. Lewis, IEDM 1991 Tech. Dig., (1991) 571.
5) C.-M. Park, J.-S. Yoo, and M.-K. Han, SSDM 1997, (1997) 350.