

Test Structure and Verification on the MOSFET under Bond Pad for Area-efficient I/O Layout in High-pin-count SOC IC's

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ABSTRACT

For saving the layout area of I/O cells in SOC chips, a test chip with large size NMOS devices placed under bond pads has been fabricated in 0.35- μm 1P4M 3.3V CMOS process for verification. The bond pads had been drawn with different layout patterns on the inter-layer metals to investigate the impact of bonding stress on the active devices under the pads. The measurement results, including thermal shock and temperature cycling tests, show that there are only little variations between devices under bond pads and devices beside bond pads. This discovery can be applied to save layout area for on-chip ESD protection devices or I/O devices of IC products, especially for the high-pin-count SOC IC's.

I. INTRODUCTION

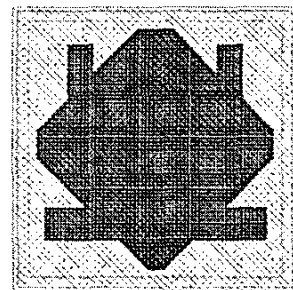
According to the lower operation speed of IC products in the past, design of bond pads has been ignored in the IC design flow. As device feature sizes of IC technologies are shrunk more rapidly than the size of bond pad, and the number of I/O pins increases for more complex interfaces, the layout area occupied by bond pads in a silicon chip is getting larger. The increasing I/O pins and their layout area lead to more complex interconnection and increasing die cost. If the active devices of a chip can be placed under bond pads, the die cost would be reduced obviously and the design flexibility would be also improved.

For conventional chip designs, active devices would not be placed under bond pads because circuit designers cannot make sure whether the device characteristics are still acceptable, or not, after the stress of packaging process. To make sure whether devices placed under bond pads are all right or not, there are some researches done in the past [1]-[3]. In those researches, studies of the gate leakage current [1], failure percentage after reliability tests [2], and second breakdown voltages [3] of devices placed under bond pads have been investigated. Besides, bond pads have been designed with some changes from the conventional bond pad structure. To improve the bonding reliability, the metal layer beneath the most top metal layer of bond pad is suggested to be patterned [4]. To reduce the parasitic effect for high-speed I/O circuits, the low-capacitance bond pad structure had been reported with different layout patterns [5].

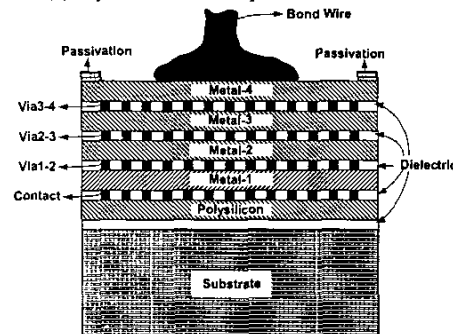
To save layout area for high-pin-count IC's, the active devices under such low-capacitance bond pads are studied and experimentally tested in a 0.35- μm CMOS process.

II. TEST CHIP DESIGN TO VERIFY DEVICES UNDER BOND PADS

A set of device designs with NMOS transistors has been fabricated in a 0.35- μm 1P4M 3.3V CMOS process to understand whether if the NMOS transistor placed under bond pad would be damaged by the wire bonding process or not. Bond pads used in this experiment are all with the same passivation window size of $86\mu\text{m}\times 86\mu\text{m}$ and top metal size of $96\mu\text{m}\times 96\mu\text{m}$. Besides, bond pad pitch in the silicon test chip is $116\mu\text{m}$. All the NMOS transistors in the silicon test chip are drawn with the same feature size and layout style. The NMOS has total channel width of $2016\mu\text{m}$ and channel length of $0.5\mu\text{m}$. The layout of the NMOS transistor is drawn in 21 fingers with each unit finger width of $96\mu\text{m}$. The drain, gate, source, and bulk of NMOS are all connected to a standalone bond pad for each terminal in the silicon test chip.



(a) Layout view of bond pad used in Device-1



(b) Cross-sectional view of (a)

Fig. 1 (a) Layout pattern of the conventional bond pad used in Device-1, which is beside a NMOS transistor, (b) the corresponding cross-sectional bond pad structure of (a).

The “Device-1” is the first device design, and constructed by four bond pads in line and a NMOS transistor between two of these bond pads. This NMOS device, which is placed conventionally beside bond pads instead of under bond pad, is used as a reference device of the test chip. Experimental results from this reference device can be used as a set of basic reference data. The corresponding layout pattern of the bond pad in this device and its cross-sectional view are shown in Fig. 1(a) and Fig. 1(b), respectively. The dark area in center of Fig. 1(a) is shaped by a plurality of via plugs. From Fig. 1(b), it is clear that there is no active device under the bond pad structure.

The second design, named as “Device-2”, is constructed by four bond pads in line for the four terminals of a NMOS transistor, and a NMOS transistor placed directly under one of these bond pads. The layout view of the bond pad with a NMOS device under it in “Device-2” is shown in Fig. 2(a). The NMOS device symbol in Fig. 2(a) indicates that there is a NMOS device beneath the Metal-2 layer of this bond pad. Its corresponding cross-sectional view is shown in Fig. 2(b). The layout drawings of Metal-2 and Metal-3 layers are kept as flat planes (not patterned) for the bond pad with a NMOS device under it in Device-2.

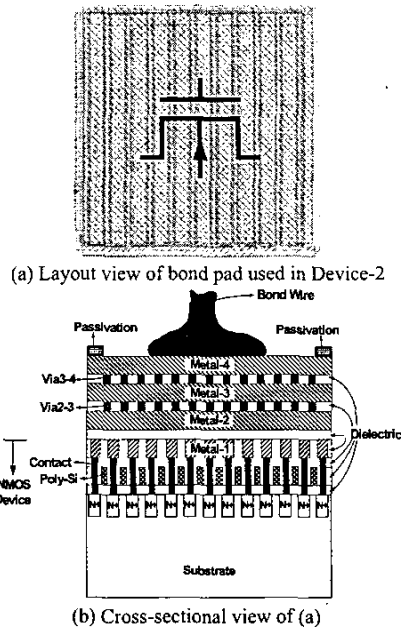


Fig. 2 (a) Layout pattern of the bond pad with a NMOS transistor under Metal-2 in Device-2, and, (b) the corresponding cross-sectional bond pad structure of (a). The NMOS device symbol in (a) indicates that there is a NMOS device beneath the Metal-2 layer of this bond pad.

The third design of device group, which includes “Device-3”, “Device-5”, and “Device-7” designs, is constructed by four bond pads in line for the four terminals of a NMOS transistor, and a NMOS transistor placed directly

under one of these bond pads. In the third design, the bond pad with a NMOS transistor placed under it is constructed by a NMOS transistor, which is placed under Metal-2 layer, and a patterned Metal-3 layer. Metal-2 and Metal-4 layers of this designed bond pad are both in a large area of un-patterned plate. Its cross-sectional structure is shown in Fig. 3(a). The corresponding layout views of the bond pads with a NMOS transistor under each of them in Device-3, Device-5, and Device-7 are shown in Fig. 3(b), Fig. 3(c), and Fig. 3(d), respectively. As shown in Fig. 3(b)-(d), the Metal-3 layout drawings are drawn with different patterns to investigate the relationship between different layout patterns and sustainable bonding stress. The NMOS device symbols on the bond pad layout patterns indicate that there is a NMOS transistor under the patterned metal layer(s) for each of these bond pads.

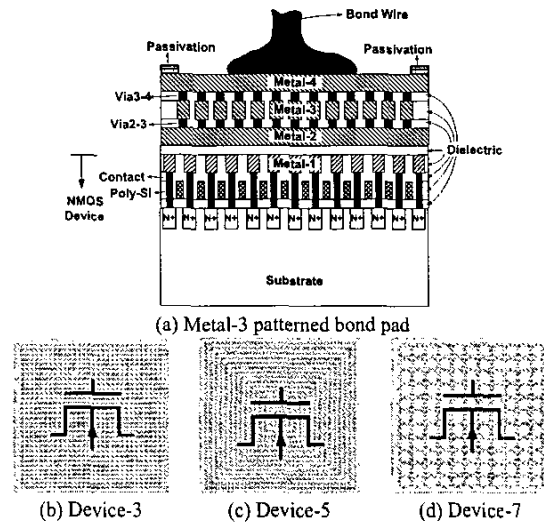


Fig. 3 Layout designs of bond pads with NMOS devices placed under Metal-2. (a) Cross-sectional bond pad structure of Metal-3 patterned devices, (b)-(d) show the patterned Metal-3 layer layouts of Device-3, Device-5, and Device-7, respectively. The NMOS device symbols on the bond pad layout patterns indicate that there is a NMOS transistor under the patterned metal layer(s) for each bond pad.

The fourth design of device group, which includes “Device-4”, “Device-6”, and “Device-8” designs, is also constructed by four bond pads in line for the four terminals of a NMOS transistor, and a NMOS transistor placed directly under one of these bond pads. In the fourth design, the bond pad with a NMOS transistor placed under it is composed of a NMOS transistor beneath Metal-2 layer. The metal layers, Metal-2 and Metal-3, are drawn with different layout patterns for each device. Metal-4 layer of the designed bond pad is in a large area of un-patterned plate. Cross-sectional view of the designed bond pad structure is shown in Fig. 4(a). The corresponding layout views of the bond pads with a NMOS transistor under each of them in Device-4, Device-6, and Device-8 are shown in Fig. 4(b), Fig. 4(c), and Fig. 4(d),

respectively. As shown in Fig. 4(b)-(d), the Metal-2 and Metal-3 layout drawings are drawn with different patterns to investigate the relationship between different layout patterns and sustainable bonding stress. The NMOS device symbols on the bond pad layout patterns indicate that there is a NMOS transistor under the patterned metal layer(s) for each of these bond pads. The designed patterns applied on Metal-2 and Metal-3 layers of the fourth design group are the same with the patterns applied on the Metal-3 layers of the third design group. In other words, the layout patterns of Metal-2 and Metal-3 layers in Device-4, Device-6, and Device-8 are the same with the layout patterns of Metal-3 layer in Device-3, Device-5, and Device-7, respectively. These designed layout patterns on metal layers, Metal-2 and Metal-3, and the active device region of bond pads are modified from the prior report on low-capacitance bond pad for high frequency applications [5]. Therefore, except saving layout area of a silicon chip, the parasitic capacitance of the proposed bond pad design can be lowered when comparing with that of a conventional bond pad.

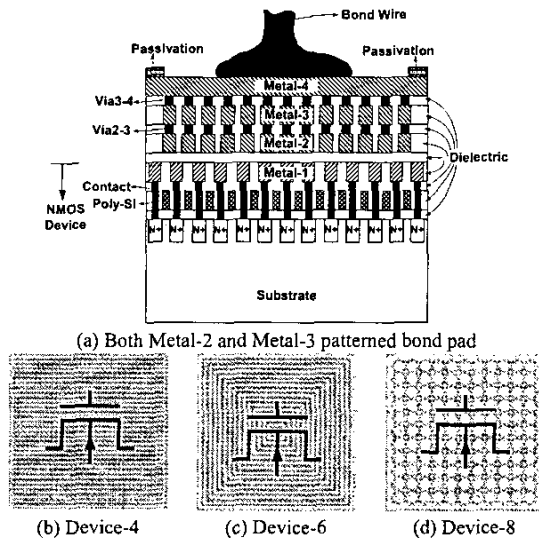


Fig. 4 Layout designs of bond pads with NMOS devices placed under Metal-2. (a) Cross-sectional bond pad structure of Metal-2 and Metal-3 patterned devices, (b)-(d) show the patterned Metal-2 and Metal-3 layouts of Device-4, Device-6, and Device-8, respectively. The NMOS device symbols on the bond pad layout patterns indicate that there is a NMOS transistor under the patterned metal layer(s) for each bond pad.

III. EXPERIMENTAL RESULTS

The proposed bond pad design in this paper is to verify whether the NMOS transistor placed under bond pads with different Metal-2 and Metal-3 layout patterns would be damaged by the assembly process steps or not. First step of the verification work is to measure the wafer-level DC

characteristics of the NMOS transistor in the designed devices. By probing the four terminals of each NMOS transistor on the wafer, the NMOS DC characteristics before wire bonding can be measured by HP4155 semiconductor parameter analyzer. The threshold voltage (V_t) of all the NMOS transistors on the test chips should be within the range listed on the process control management (PCM) specification released by foundry [6]. The off state drain current (I_{off}) with drain voltage (VD) biased at VDD level of 3.3V and the gate leakage current (IG) with gate voltage (VG) biased at VDD level should be both acceptable for different applications.

After the wafer-level measurements, assembly of the test chip samples is then taken in two different types of package : side-brazed dual inline (DIP) package and plastic DIP package. The side-brazed package is a kind of package with its leadframe uncovered by plastic molding compound. Thermal stress of the compound molding process and the mismatch of coefficients of thermal expansion (CTE) after compound molded could be the reasons of device performance degradation of the NMOS transistors placed under bond pads. Consequently, the purpose of performing these two types of package is to verify whether the performance of the NMOS transistors would be further degraded by the compound molding process or not. The wire bonders for side-brazed package and plastic package are Panasonic HW22U-H and ESEC 3008, respectively. The DC I-V characteristics of the NMOS transistors after assembly for both types of packaged IC's were measured. While comparing with the wafer-level measurement data, if the gate leakage current (IG), or off state drain current (I_{off}), or the threshold voltage (V_t) of the NMOS transistor in the test chip are shifted obviously after assembly process steps, it is known that the device performance is affected by the wire bonding process or the compound molding process.

For the side-brazed DIP packaged samples, normal bonding force of the corresponding wire bonder, Panasonic HW22U-H, is 50g and normal treated bonding power is 80mW. The applied bond ball diameter is 100 μ m (or 4mil) and the taken bond wire diameter is 25.4 μ m (or 1mil) in the experiments. To make sure whether the device performance of the NMOS transistor placed under bond pad would be affected by the wire bonding force or not, the applied wire bonding force was controlled and split into several conditions. The split conditions of wire bonding force are 0.75 \times , 0.85 \times , 1 \times , 1.25 \times , 1.3 \times , 1.5 \times , and 1.75 \times of normal wire bonding force of 50g. In other words, the applied wire bonding forces are 37.5g, 42.5g, 50g, 62.5g, 65g, 75g, and 87.5g for each split condition. When the wire bonding force is increased, the bond ball on the bond pad would be spread into a more unexpected shape with a larger occupied area. For wire bonding force larger than 87.5g, the shape of bond ball would be spread into an unacceptable larger area. This large bond ball area could lead to the short circuit phenomenon of bond balls on adjacent bond pads. Fig. 5 shows the optical microscope (OM) photos of bond balls on bond pads applied with different wire bonding forces.

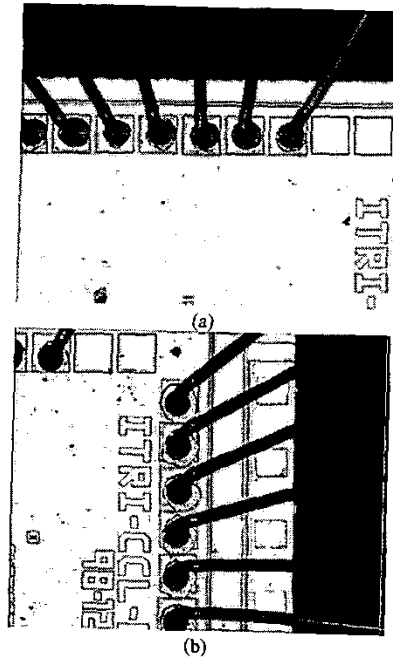


Fig. 5 The bond ball sizes are (a) not dispersed by 1x of normalized bonding force (50g), and (b) dispersed obviously by 1.75x of normalized bonding force (87.5g). Adjacent bond pads might be connected together by the dispersed bond balls caused by a larger bonding force.

For the plastic DIP packaged samples, normal bonding force of the corresponding wire bonder, ESEC 3008, is 51g and normal treated bonding power is 850mW. The applied bond ball diameter is about 80 μ m (or 3.1mil) and the taken bond wire diameter is 30.5 μ m (or 1.2mil) for the experiments. The molding process temperature for these samples is 175°C, which is a conventional temperature degree for compound molding process.

The dependencies of wire bonding force and the DC characteristics of the NMOS transistors for different designed devices in the test chip are shown in Fig. 6. Results in Fig. 6 are from the samples assembled by side-brazed packages, which are not treated by the compound molding process. In Fig. 6, measurement results of Device-1 design, which is known as a NMOS transistor beside bond pads, are highlighted by relatively larger size triangle symbols as a data reference level. The x-axes of Fig. 6 are the normalized bonding forces, which are the actually applied wire bonding forces normalized by a normal bonding force of 50g. In other words, 1x of normalized bonding force equals to applied wire bonding force of 50g; 0x of normalized bonding force means device characteristics before applying wire bonding force (or, the wafer-level measurement results). Fig. 6(a) shows the relationship between threshold voltage (V_t) and normalized wire bonding force. It is clear that the variation range of NMOS threshold voltage (V_t) is only from 0.54V to 0.58V after different levels of wire bonding force.

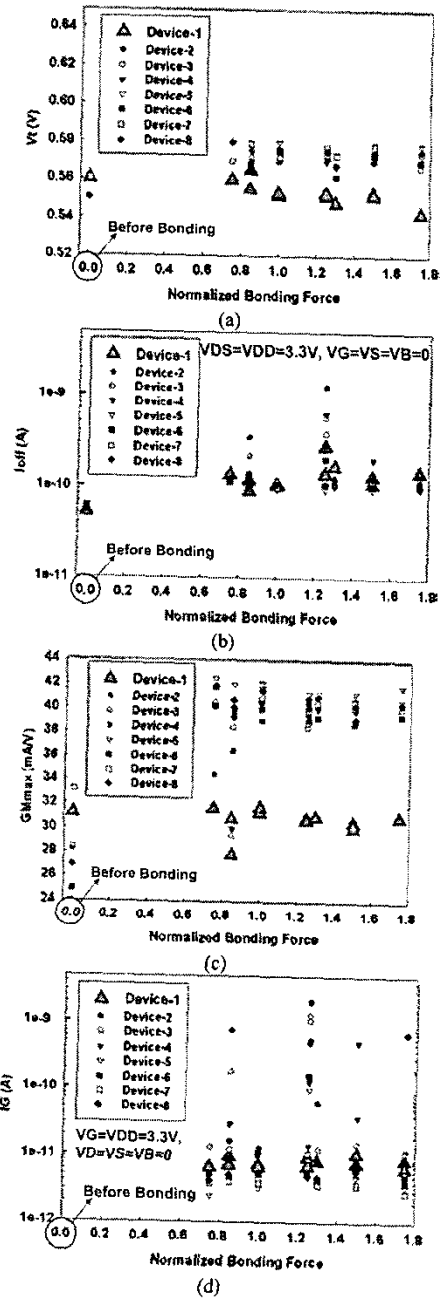


Fig. 6 The dependencies of wire bonding force and device DC characteristics of (a) threshold voltage (V_t), (b) off-state drain current (I_{off}), (c) maximum gm (GM_{max}), and (d) gate leakage current (I_G) of NMOS transistors beside bond pads (Device-1) or beneath patterned metal layers of bonding pads (Device-2 ~ Device-8).

Fig. 6(b) shows the relationship between off state drain current (I_{off}) and normalized wire bonding force. Although

there is a larger range of variation for the results of applying $1.25\times$ of normalized wire bonding force (62.5g), the off state drain current (I_{off}) is still in the order of $1nA$, which is reasonable for a large NMOS transistor with its channel width of $2016\mu m$. Fig. 6(c) shows the relationship between maximum transconductance (GM_{max}) and normalized wire bonding force. When comparing with the Device-1 design, results of other devices in Fig. 6(c) are shifted about 50%. Fig. 6(d) shows the relationship between gate leakage current (I_G) and normalized wire bonding force. Although results in Fig. 6(d) are varied from the order of $10pA$ to the order of $1nA$ when comparing with the Device-1 design, it is still very small for a NMOS transistor with large channel width of $2016\mu m$.

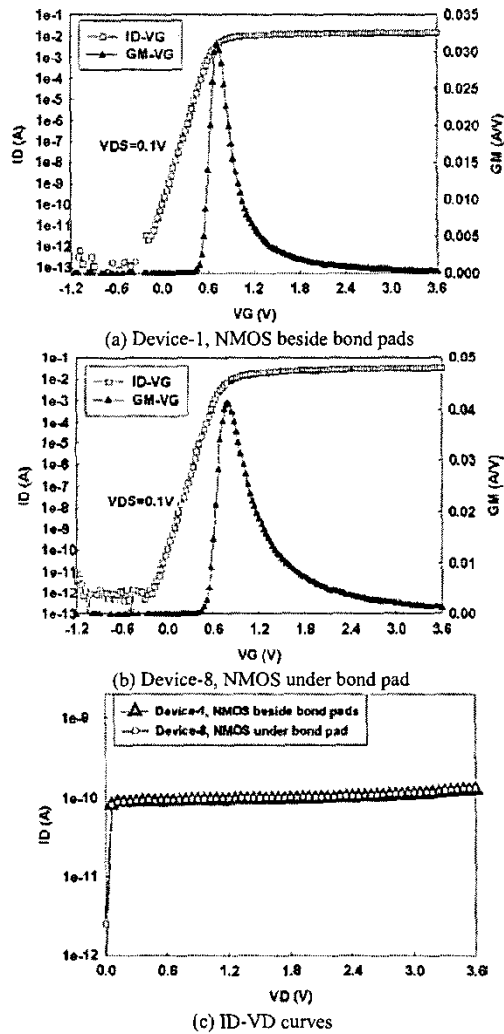


Fig. 7 Comparison of device DC characteristics after compound molding: (a) ID-VG curve of Device-1, (b) ID-VG curve of Device-8, (c) ID-VD curves of Device-1 and Device-8.

Fig. 7 shows the measurement data from plastic DIP packaged samples. The drain current (I_D) and transconductance (GM) with drain-source voltage (V_{DS}) biased at $0.1V$ versus gate biased voltage (V_G) after compound molding for Device-1 and Device-8 are shown in Fig. 7(a) and Fig. 7(b), respectively. For Fig. 7(a) and Fig. 7(b), the x-axis and left hand y-axis are the gate biased voltage (V_G) and the measured drain current (I_D) of the NMOS transistor, respectively. The right hand y-axis is about the transconductance (GM) of the NMOS transistor. Although the drain current (I_D) with gate voltage (V_G) biased at $-1.0V$ is changed from several $0.1pA$ of Fig. 7(a) to several pA of Fig. 7(b), the variation is very small for the NMOS transistor with large channel width of $2016\mu m$. Besides, the V_G value at maximum transconductance (GM) value are almost the same for both Fig. 7(a) and Fig. 7(b). This indicates that the threshold voltage of the NMOS transistor is not shifted obviously for NMOS transistors placed beside or under bond pads. The Device-1 and Device-8 NMOS I-V curve of drain current (I_D) versus drain biased voltage (V_D) with other terminals (gate, source, and bulk) shorted to ground after compound molding are shown in Fig. 7(c). The x-axis and y-axis of Fig. 7(c) are the drain biased voltage (V_D) and the drain current (I_D) of the NMOS transistor, respectively. From Fig. 7(c), the waveform with triangle symbols is from Device-1 with a NMOS transistor beside bond pads, and the waveform with rectangular symbols is from Device-8 with a NMOS transistor under bond pad. So, it can be concluded that the off state drain current (I_{off}), which is defined as the drain current amplitude while drain voltage biased at V_{DD} level of $3.3V$ and the other terminals connected to ground level of $0V$, is kept in the same order of $100pA$ for NMOS placed beside and under bond pads after compound molding process.

Fig. 8 shows the measurement results from the wafer-level NMOS transistors and the plastic DIP packaged samples. After assembly processes applied on these samples, both temperature cycling and thermal shock tests were applied onto the samples. Both of these thermal tests were applied with 200 cycles for each in condition C ($-65^\circ C \sim 150^\circ C$) of US military standard MIL-STD-883E [7]-[8]. Fig. 8(a) shows the relationship between the drain current (I_D) and the gate biased voltage (V_G) in the subthreshold region with $0.1V$ drain biased voltage for Device-5 with a NMOS transistor placed under the bond pad. There are four curves in Fig. 8(a), which were measured from the samples at different conditions. These four curves are almost overlapped into one curve in the subthreshold region of the NMOS transistors. This indicates that the switching speeds of the NMOS transistors were neither degraded by the assembly process steps, nor the thermal tests applied on the samples. Fig. 8(b) shows the relationship between the off state drain current (I_{off}) and different devices in the test chip. It indicates that there is no difference on I_{off} of different devices for varied split conditions. In other words, the off state drain currents (I_{off}) of the NMOS transistors on the samples of designed test chip were not affected by the assembly process steps or the applied thermal tests. Fig. 8(c) shows the relationship

between the gate leakage current (IG) and different devices in the test chip. From Fig. 8(c), the gate leakage current (IG) after the assembly process steps was increased by 1~2 orders when comparing with the wafer-level measurement data; the gate leakage current (IG) after the thermal tests was increased by 2~3 orders when comparing with the wafer-level measurement data. Although the gate leakage currents are increased, they are still smaller than the order of 10pA for a NMOS transistor with its channel width of 2016 μ m.

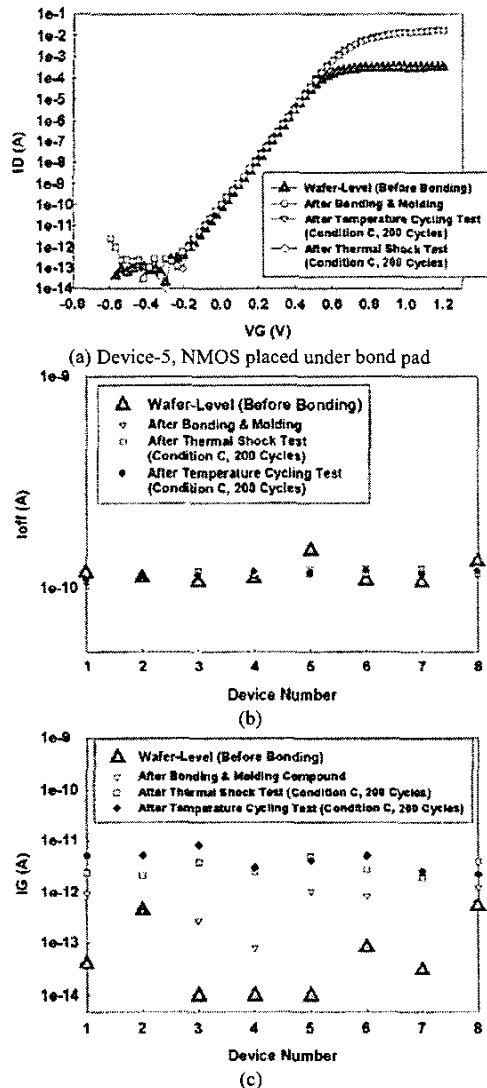


Fig. 8 The dependencies of device DC characteristics and assembly process steps. (a) Drain current (I_D) versus gate biased voltage (V_G) of NMOS device placed under bond pad, (b) off-state drain current (I_{off}) versus varied designed devices after specific assembly process step, (c) gate leakage current (IG) versus varied designed devices after specific assembly process step.

IV. CONCLUSION

A silicon chip with the large size NMOS transistors placed directly under bond pads has been verified in a 0.35- μ m 1P4M 3.3V CMOS process. DC characteristics of the NMOS devices were measured for 4 major steps of assembly, which are known as wafer-level probing, after wire bonding (side-brazed DIP packaged samples), after compound molding (plastic DIP packaged samples), and after life time thermal tests (temperature cycling and thermal shock tests). After a series of experimental investigations and DC characteristics measurements, the device performances of NMOS transistors placed under bond pads have been proved to be with only little variations with that placed beside the bond pads. These results are acceptable for general CMOS IC products to save chip layout area. Therefore, not only ESD protection devices or I/O devices can be placed under bond pads for different applications, but also the parasitic capacitance of bond pad can be reduced by the patterned metal layers and the N+ diffusion region beneath the bond pad. Without any extra process steps, the proposed method of devices placed under bond pads makes the chip layout placement be more flexible and with the advantage of cost reduction for high-pin-count IC products.

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