DESIGN OF 2.5V/5V MIXED-VOLTAGE CMOS I/O BUFFER WITH ONLY THIN OXIDE DEVICE AND DYNAMIC N-WELL BIAS CIRCUIT

Ming-Dou Ker and Chia-Sheng Tsai
Nanoelectronics and Gigascale System Lab.
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

ABSTRACT

This paper presents a 2.5V/5V mixed-voltage CMOS I/O buffer that does not need a CMOS technology with a dual-oxide option and complex bias circuits. The proposed mixed-voltage I/O buffer with simpler circuit structure can overcome the problems of leakage current and gate-oxide reliability, which occurring in the conventional CMOS I/O buffer. In this work, the new proposed design has been realized in a 0.25-μm CMOS process, but it can be easily scaled toward 0.18-μm or 0.15-μm processes to serve a 1.8V/3.3V mixed-voltage I/O interface.

1. INTRODUCTION

The transistor's dimension had been scaled down toward the nanometer region and the circuit power supply voltage also decreases as well [1]. Obviously, the smaller transistor dimension makes the chip area smaller to save silicon cost. The lower power supply voltage results in lower power consumption. With the advancement of modern CMOS technology, chip design quickly migrates to the lower voltage level. But, some peripheral components or other ICs are still operated with the higher voltage levels (3.3V or 5V) [2]. In other words, there are chips with different supply voltages coexisting in a system. In order to interface chips with different supply voltages, the conventional CMOS I/O buffer is unsuitable anymore. Several problems may arise with it about the gate-oxide reliability [3], the hot carrier degradation [4], and the undesirable leakage current paths [5], [6].

The conventional CMOS I/O buffer in a 0.25-μm CMOS process is shown in Fig. 1. The internal circuit is operated with Vdd of 2.5V, but the input signal at the I/O pad may rise up to 5V in the tristate input mode. In this high-voltage input mode, the gates of the pull-down NMOS and the pull-up PMOS are controlled at 0V and 2.5V by pre-driver circuit, respectively, to turn off the pull-down NMOS and the pull-up PMOS. But, if the input voltage at the pad rises as high as 5V, the parasitic drain-to-well junction diode in the pull-up PMOS will be forward biased to cause a leakage current path from pad to Vdd. Furthermore, because the |Vgd| of the pull-up PMOS equals to 2.5V, which is higher than |Vtp|, this PMOS conducts incorrectly and causes another leakage current path from pad to Vdd. In addition to leakage current, overstress across gate-oxide is a great danger to mixed-voltage applications. Besides, the pull-down NMOS and transistors in the input buffer also suffer overstress voltage across their thin gate oxides. The thin gate oxide may become leaky due to tunneling effect or dielectric breakdown. If the electric field across the thin gate oxide is too large, it may even be permanently damaged.

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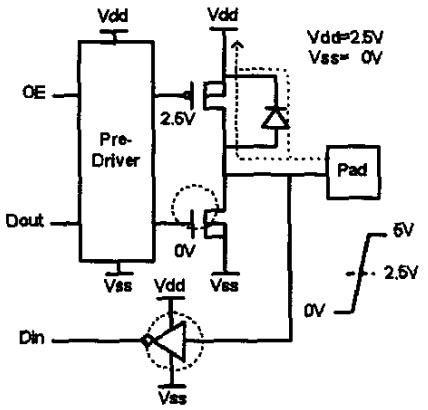

Figure 1. The conventional CMOS I/O buffer in tristate input mode.

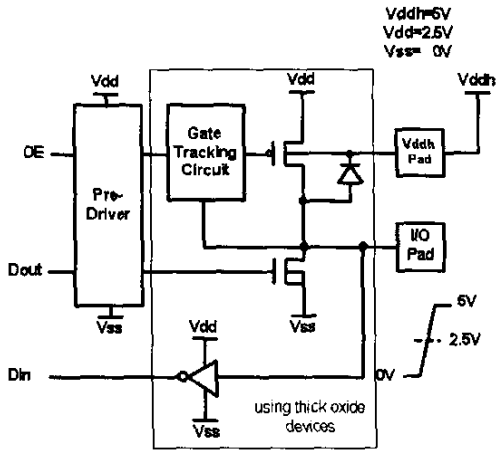

Figure 2. The mixed-voltage CMOS I/O buffer with a dual-oxide option and external N-well bias.

To overcome these problems, the I/O buffer for mixed-voltage interface with a dual-oxide option and an external n-well bias has been reported, which is shown in Fig. 2. To solve the problem of gate-oxide reliability, the dual-oxide (thin and thick oxide layers) option [7], [8] is often used in CMOS technology. Because the thick gate oxide can avoid gate oxide breakdown, transistors that may suffer excessive gate-oxide stress should be replaced with thick oxide devices, and other internal transistors remain with thin gate oxide. To prevent leakage current paths from the pad through the parasitic drain-well junction diode to Vdd with the lower voltage source, the body-terminal is coupled to a new pad that is connected with the higher external voltage source. Thus, the parasitic drain-well junction diode is reverse biased, and there is no leakage current from the I/O pad to Vdd.

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However, the gate tracking circuit block is still redesigned to prevent the leakage current path resulting from incorrectly conducting of the pull-up PMOS.

The mixed-voltage I/O buffer with a dual-oxide option and external N-well bias is easy to be designed, but it just affects a temporary solution for mixed-voltage applications. It has some drawbacks. First of all, it increases the cost of wafer fabrication with the dual-oxide option in CMOS processes. Second, the use of dual oxide changes the threshold voltages of the pull-up/pull-down transistors and degrades the performance of the I/O buffer. Third, the requirement of the additional pad and associated metal connection delivering the bias to the body terminal of PMOS transistors increases the difficulty in layout routing. Forth, in the pull-up PMOS, because the body terminal is coupled to an external voltage source higher than the voltage of the source terminal, which is coupled to internal voltage supply, its threshold voltage is increased due to the body effect.

In this work, a new circuit design for the mixed-voltage I/O buffer with simpler circuit structure has been proposed to overcome the problems of leakage current and gate-oxide reliability in the mixed-voltage I/O interface, without using the dual-oxide process option and the external n-well bias.

2. DESIGN CONCEPT

With cost consideration, the mixed-voltage I/O buffer with a dual-oxide option and external N-well bias is not suitable applied in the mass-production IC products. The mixed-voltage I/O buffer with only thin oxide device and dynamical n-well bias is often used in IC products. The design concept of such I/O circuit is shown in Fig. 3. In the block diagram, the MN0 and MN1 are connected in the stacked configuration, which has been widely applied to the mixed-voltage I/O buffer [9]-[13]. To explain how the stacked-NMOS works, we assume that the gate of MN1 is discharged to 0V to turn it OFF and the I/O pad is driven by a 5-V input signal. Because the gate of NMOS MN0 is coupled to Vdd=2.5V, the drain terminal of MN1 will be charged to about 2.5-0.6=1.9V, where the NMOS has a threshold voltage of 0.6V. The gate-oxide stress voltages are derived as:

For MN0 $|Vgd|=2.5V \le 2.5V$, $|Vgs|=0.6V \le 2.5V$, and
For MN1 $|Vgd|=1.9V \le 2.5V$, $|Vgs|= 0V \le 2.5V$.

It is obvious that the gate-oxide stress of neither MN0 nor MN1 exceed 2.5V. In other circuit operating cases, such as MN1 is turned OFF and the I/O pad is driven by 2.5-V or 0-V signals or MN1 is turned ON and consequentially the I/O pad is discharged to 0V, all gate-oxide stress voltage of MN1 and MN2 are less than 2.5V.

Moreover, the gate tracking circuit is designed to prevent the leakage current path resulting from incorrectly conducting of the pull-up PMOS. So this circuit block must realize the following functions:

- ***In transmit mode:***
  The gate tracking circuit must transfer the signal from pre-driver to the gate terminal of the pull-up PMOS transistor exactly.
- ***In receive mode(tristate mode):***
  If the I/O pad is driven by 5-V signal, the gate tracking circuit will charge the gate of the pull-up PMOS transistor to 5V as well, for turning this PMOS OFF completely and preventing leakage current flow from the pad to Vdd through it.
  If the I/O pad is driven by 0-V signal, the gate tracking circuit should switch the gate terminal of the pull-up PMOS transistor to 2.5V. The pull-up PMOS is kept off.

If the I/O pad is driven by 2.5-V signal, the gate voltage of the pull-up PMOS transistor can be any level between 5V and 2.5V, because the drain and source terminals of the pull-up PMOS transistor are at the same voltage level. It was often biased at Vdd of 2.5V in this condition.

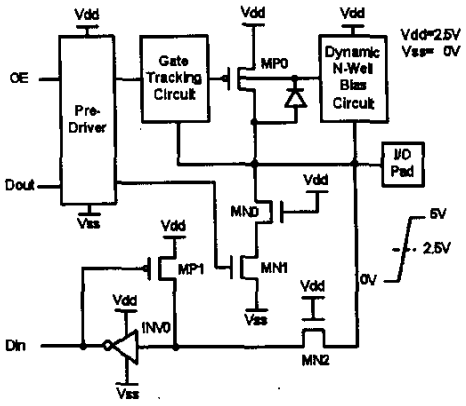

Figure 3. A mixed-voltage CMOS I/O buffer with only thin oxide device and dynamic N-well bias. Only the standard 2.5-V 0.25-μm CMOS device is used to build up the circuit blocks for 5V-tolerant input applications.

Besides, the dynamic n-well bias is designed to prevent the leakage current flows through the parasitic drain-well junction diode. The driving ability of a MOS is related to |Vbs| because of the body effect. So, if the pull-up PMOS or any other PMOS transistors whose n-well terminals are controlled by the dynamic n-well bias are turned ON for normal circuit operating, their n-well terminals should be biased at 2.5V at once to achieve the best performance. If these PMOS transistors are not in use, their n-well terminals can be kept floating, which will be charged through the parasitic drain-well or source-well junction diodes until these parasitic diodes are cut off. Note that there is no static leakage current path in the condition.

The input buffer is composed of the NMOS transistor MN2, the PMOS transistor MP1, and the inverter INV0. MN2 can block the voltage level of the input signal at the pad higher than 2.5V to protect internal circuits from gate-oxide degradation. For example, if the I/O pad, or the drain of MN2, is driven by a 5-V input signal, the source of MN2 will be charged to only about 2.5-0.6=1.9V. Although MN2 prevent excessive gate-oxide stress efficiently, but it also makes that the input voltage level of inverter INV0 can not rise as high as 2.5V to completely turn off the pull-up PMOS in INV0. As a result, the static power consumption is increased because the pull-up PMOS is not completely off with a sub-threshold current. So, the MP1 is added to serve a pull-up element to pull the final voltage level of logical "1" from 1.9V to 2.5V.

3. CIRCUIT IMPLEMENTATION

3.1 Prior Design

Fig. 4(a) shows a prior art of the mixed-voltage CMOS I/O buffer designed with only thin oxide device and dynamic N-well bias [9]. The NMOS transistors MN3, MN4 and PMOS transistors MP2, MP3, MP4 compose the gate tracking bias circuit. The NMOS transistor

MN5 and PMOS transistors MP5, MP6, MP7 compose the dynamic n-well bias circuit. The body terminals of all PMOS transistors in the gate tracking circuit and the dynamic n-well bias circuit are connected to the output node of the dynamic n-well bias circuit, which is called as "floating n-well." This circuit has overcome the problems of gate-oxide reliability and leakage current paths, but it used too many devices to realize the desired circuit functions. The more device components used in the I/O buffer often increase the layout area for the I/O cell and cause a more complex metal interconnection in the I/O cell.

3.2 This New Design

The new design in this work to realize such mixed-voltage I/O buffer with less device components is shown in Fig. 4(b). When the OE signal is at the logical "0", the I/O buffer is operating in the transmit mode. In this mode, the I/O pad signal should raise or fall according to the Dout signal, which is controlled by the internal circuits of IC. The lower output port of pre-driver is directly connected to the gate of MN1 just as a common I/O buffer. The upper output port of pre-driver is connected to the gate of pull-up PMOS through the gate tracking bias circuit. If the signal at this port is kept at logical "0", it will be fully transferred to the gate of MP0 through MN2 to pull up the I/O pad with an output voltage level of 2.5V. The logical "0" signal turns on MP0 and MP4, then the floating n-well is biased at vdd=2.5V. If the signal at the upper output port of pre-driver is kept at logical "1", the gate of MP0 is first charged to about Vdd-|Vtp| through MN2. Consequently, the I/O pad and the drain of MN1 are discharged to about 0V by the turned-on MN0 and MN1. Therefore, MP1 are turned on until the gate of MP2 is discharged to about |Vtp|. At this moment, MP2 is turned on to continually charge up the gate of MP0 to Vdd of 2.5V, so the MP0 can be fully turned off. In this condition, MP4 is also turned off. The floating n-well is biased at a voltage of Vdd because of the parasitic source-well junction diode of MP0 and MP4.

When the I/O buffer is operating in the receive mode (tristate mode), the upper and lower output ports of pre-driver will be logical "1" and logical "0", respectively, to turn MP0 and MN1 off. The Din signal will follow up the input signal at the I/O pad. In order to prevent leakage current through the channel of the pull-up MP0 to Vdd, MP3 is used to track the gate voltage with the input signal voltage level as reference. When the I/O pad voltage exceeds Vdd+|Vtp| such as 5V, MP3 conducts and the gate of MP0 is charged to 5V. So, MP0 can be completely turned off to prevent any leakage current through the channel of MP0. In this condition, the MP4 is also turned off, and the floating n-well of MP0 is biased by the 5-V input signal through its drain-well junction diode. As a result, there is no static leakage current flowing through the parasitic drain-well junction diode of MP0 to Vdd.

In order to transfer the signal from I/O pad to Din, MN0, MP5, and INV0 are used. In the input circuit, the drain of MN1 is kept at 2.5V due to the operation of weak pull-up PMOS MP5 and the INV0. Thus, MP1 is turned on and the gate of MP2 is charged to 5V to fully turn MP2 off. The parasitic drain-well junction diode of MP1 helps charging, too. Keeping MP2 off can avoid the 5-V input signal at the gate of MP0 to damage devices in the pre-driver.

When the I/O pad voltage falls to 0V, the drain voltage of MN1 does, too. Thus, the gate voltage of MP2 falls to about 0.7V and MP2 is turned on to charge the gate of MP0 to 2.5V. In this condition, MP0 is still fully turned off, and there is no leakage current flowing through MP0. Note that direct connection of the gate of MP2 to the I/O pad is prohibited due to the electrostatic discharge (ESD) consideration. The ESD protection device should be also added into the mixed-voltage I/O circuit [13].

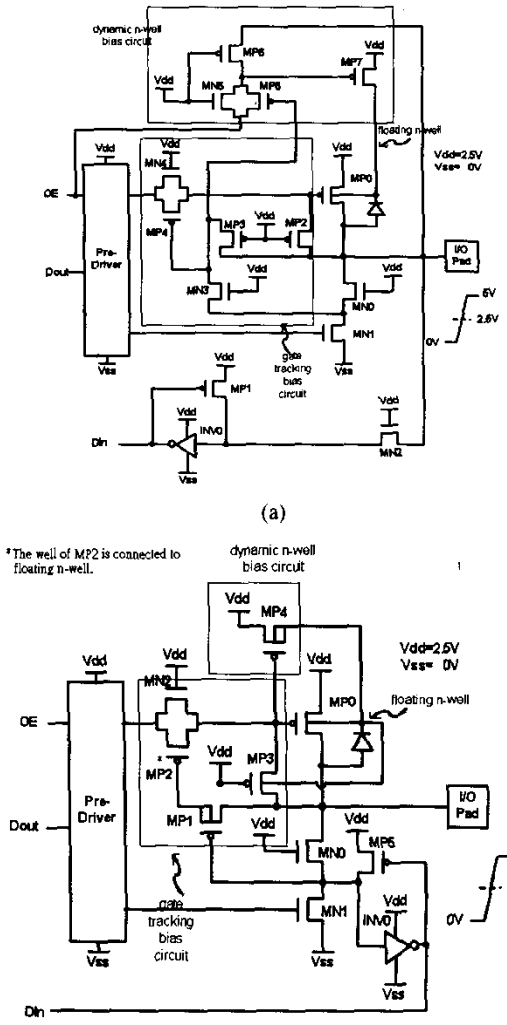

Figure 4. (a) A prior design of the mixed-voltage CMOS I/O buffer with only thin oxide device and dynamic N-well bias. (b) The new circuit proposed in this work to realize the mixed-voltage CMOS I/O buffer with less device components for saving silicon cost.

4. SIMULATION RESULTS AND LAYOUT

The SPICE simulation waveforms on the new proposed mixed-voltage I/O buffer are shown in Fig. 5. A 30-pF load is added to the I/O pad in the simulation. Fig. 5(a) shows the circuit behavior of the circuit in Fig. 4(b) in the transmit mode, and Fig. 5(b) shows circuit behavior of in the receive mode (tristate mode). To mimic the real conditions of circuit operation, the I/O pad signal in Fig. 5(b) is created by an identical mixed-voltage I/O buffer. It is seen that functions of the I/O buffer are correct and the dynamic n-well bias acts as

expectancy. Because of the gate tracking bias circuit, |Vgd| of MP0 is always below the nominal voltage 2.5V, so gate-oxide degradation can be successfully prevented.

Fig. 6 shows the layout of the proposed mixed-voltage I/O buffer in Fig. 4(b), which is realized in a 0.25-μm shallow-trench- isolation salicided CMOS process. The gate tracking bias circuit is composed of NMOS transistor MN2, as well as PMOS transistors MP1, MP2, and MP3. The input buffer is composed of PMOS transistor MP5, inverter INV0; and the stacked NMOS MN0 and MN1. A testchip drawn with the traditional design and this new proposed design on the mixed-voltage I/O buffers is now under fabrication. The detailed measurement results will be shown in the presentation.

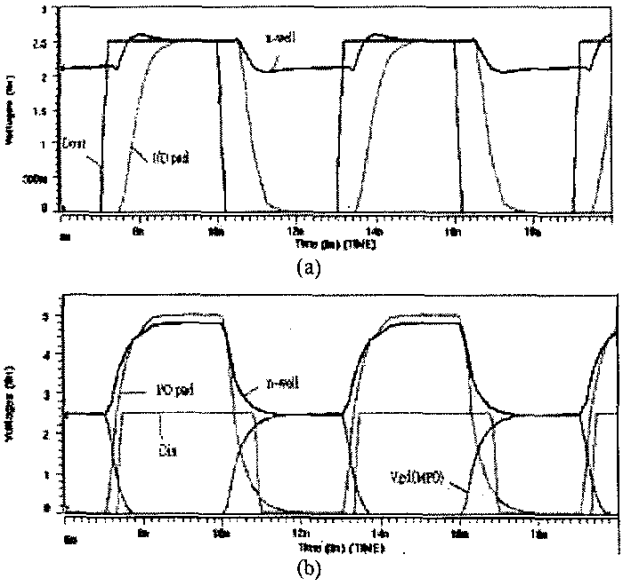

Figure 5. Simulation waveforms on the new proposed mixed-voltage I/O buffer (a) in the transmit mode, and (b) in the receive mode (tristate mode), with a 30-pF load at the I/O pad.

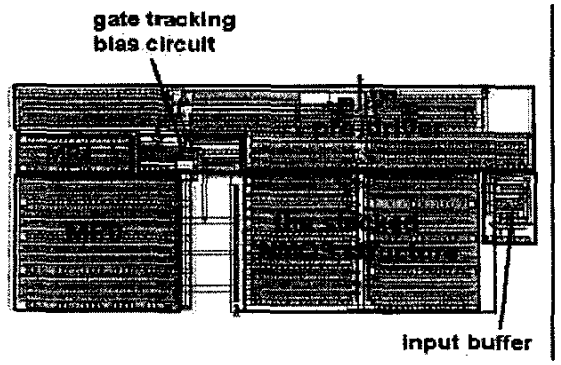

Figure 6. Layout of the new proposed mixed-voltage I/O buffer realized in a 0.25-μm CMOS process.

5. CONCLUSION

The comparisons among several kinds of mixed-voltage CMOS I/O buffers have been listed in Table 1. The mixed-voltage CMOS I/O buffer with only thin oxide device and dynamic N-well bias is better then that with a dual-oxide option and external N-well bias, on almost every hand except complexity. Too complicated circuits make it difficult in layout routing. So, it is an objective to simplify the prior arts of the mixed-voltage CMOS I/O buffer with less device components. The new mixed-voltage CMOS I/O buffer proposed in this work can achieve this objective and preserve the advantage of only using thin oxide CMOS process.

Table 1: Comparisons among several kinds of mixed-voltage CMOS I/O buffers.

	Cost (lower is better)	Performance (higher is better)	Complexity (lower is better)
Type-A	High	Low	Low
Type-B	Low	High	High
Type-C	**Low**	**High**	**Low**

Type-A: The mixed voltage I/O buffer with a dual-oxide option and external N-well bias (the prior art).

Type-B: The mixed-voltage I/O buffer with only thin oxide devices and dynamic N-well bias (the prior art).

Type-C: The mixed-voltage I/O buffer with only thin oxide devices and dynamic N-well bias (this new design).

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