# INTERFERENCE OF ESD PROTECTION DIODES ON RF PERFORMANCE IN GIGA-HZ RF CIRCUITS

*Ming-Dou Ker and Chien-Ming Lee*

Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

## ABSTRACT

The power gain and noise figure of two kinds of diode structures in a 0.25-μm CMOS process is investigated by using the two-port GSG measurement in radio-frequency region (~GHz). The power gain is degraded by ESD device with larger layout area and more serious at higher operating frequency. The noise figure is increased by ESD device with larger layout area and also is more serious at higher frequency. After the comparison on the power gain and MM ESD level between the poly-gated diode and the STI diode, the poly-gated diode is more suitable for ESD protection in RF circuits.

## I. INTRODUCTION

The parasitic effect of ESD devices would degrade the power gain S21 and increase the noise figure in RF circuit. So, the input port ESD devices need special design considerations. There are some requests for ESD protection device in RF integrated circuits: low parasitic capacitance, constant input capacitance, insensitive to substrate coupling noise, and good ESD performance [1]. The traditional input port ESD device is the gate-grounded NMOS (GGNMOS). The GGNMOS is often designed with a large device dimension and wider drain-contact- to-poly-gated layout spacing to sustain an acceptable ESD level [2]-[3]. To further improve ESD level of the NMOS with a large device dimension, the gate coupled circuit technique [4]-[6] or the substrate-triggering circuit technique [7] had been designed to uniformly trigger on the multiple fingers of the ESD protection NMOS. Besides, the additional silicide-blocked mask had been included into the deep submicron CMOS process to increase ESD robustness of the ESD clamp device. The schematic cross-sectional view of a GGNMOS with the silicide-blocked drain region is illustrated in Fig. 1. But, the GGNMOS with a larger device dimension and a wider drain diffusion junction contributes a larger parasitic drain capacitance to the input pad. The overlapped gate-to-drain capacitance also contributes to the input pad. Such GGNMOS is not suitable for RF ESD application.

A typical request for an RF input pad with maximum loading capacitance is only 200fF [8]. This target not only includes the ESD protection devices but also the bond pad itself. In order to fulfill these requirements, diodes are commonly used for ESD protection in I/O circuits. Moreover, by adding a turn-on efficient ESD clamp circuit across the power rails of the ESD protection circuit formed by the diodes, the overall ESD level of the input pin can be significantly improved [9].

In this paper, the STI diodes and poly-gated diodes were investigated by two-port GSG pad structure to measure the noise figure and S21. The ESD tester and TLPG (transmission line pulse generator) system are used to measure ESD level and It2 of ESD devices. Finally, the comparison on STI diode and poly-gated diode is done to decide the most suitable device for RF ESD application.

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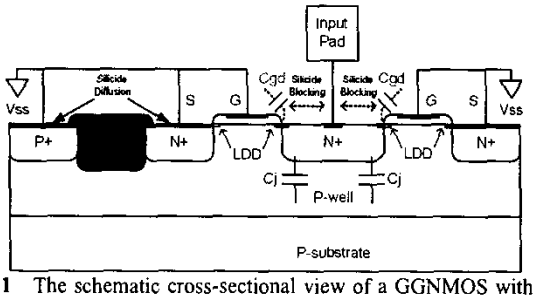


**Fig.1** The schematic cross-sectional view of a GGNMOS with the silicide-blocked drain region.

## II. DIODES

Diodes had been commonly used as ESD protection devices. The working regions can be distinguished as two parts: the forward bias region and the reverse bias region. Under the forward bias region, the current of diode would rise rapidly after its cut-in voltage (~0.6V), and has an on-resistance Ron of 1~5 Ohm. Under the reverse bias region, the current would rise rapidly after its junction breakdown voltage (about -8V in 0.25-μm process). In the forward bias region, the width of depletion region will decrease while the forward voltage across diode increases. So, the parasitic capacitance of forward bias diode will be increased. In the reverse bias region, the width of depletion region will increase to avoid the minority carrier to pass through the depletion region. The saturation current (Is) in the reverse bias region is very small (~nA). The parasitic capacitance of reverse bias diode will be decreased, because the width of depletion region increases when the reverse bias voltage across the diode increases.

Diodes have highly doped p+ and n+ diffusions separated by a low-doped region. At low current level the low-doped region is like a resistor in series with either the anode or cathode of the diode. However, at high current level, the low-doped region becomes strongly conductivity modulated, so the on-resistance of the diode at high current level is much lower than at low current level. This characteristic is good for diode in ESD condition. The power generated by ESD current on the diode can be calculated as :

$$Power = I_{ESD} \times Vop = I^2_{ESD} \times Rop \qquad (1)$$

The $I_{ESD}$ is the ESD current, which depends on the ESD voltage on the pad. The Vop is the operating point voltage of the diode under the ESD stress and the Rop is the operating point resistance of the diode under the ESD stress. The ESD level of diode operating in forward bias region is better than that in reverse bias region. By adding a turn-on efficient ESD clamp circuit across the power rails, the diodes can be designed to operate in forward bias region [9]. Therefore, he size of input diodes did not need too large. The Vdd-to-Vss ESD clamp circuit did not contribute parasitic effect to RF input pad. So, the size of Vdd-to-Vss ESD clamp can be drawn as large as you want to possess a high ESD level. Diode in forward bias operation is very useful in RF ESD application.

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### *A. STI Diode*

STI (shallow-trench-isolation) diode is the traditional diode structure. The foundry always supplies the model of STI diode. The schematic cross-sectional view of STI diode is shown in Fig. 2(a), where it is a n+/p-well diode. The N+ diffusion (cathode) and P+ diffusion (anode) are separated by shallow trench isolation (STI). The P+ diffusion surrounds the N+ diffusion. In ESD condition, the ESD current path along the diode is shown by the dashed line in Fig. 2(a). The ESD current would flow from P+ diffusion to N+ diffusion under the STI layer.

The practical layout of a unit cell of the STI diode and its symbol are drawn in Fig. 2(b). The device cross-sectional view along the line A--B of Fig. 2(b) is corresponding to that drawn in Fig. 2(a). The N+ diffusion is drawn at the center of the cell, and the P+ diffusion connected to VSS surrounds the whole unit cell at the outside. The device layout parameters are also shown in Fig. 2(b). X is the length of the N+ diffusion. S is the minimum length of STI. W is the width of the N+ diffusion. The parameter of W was changed in the testchips to investigate the power gain S21, noise figure, and ESD level of these STI diodes.

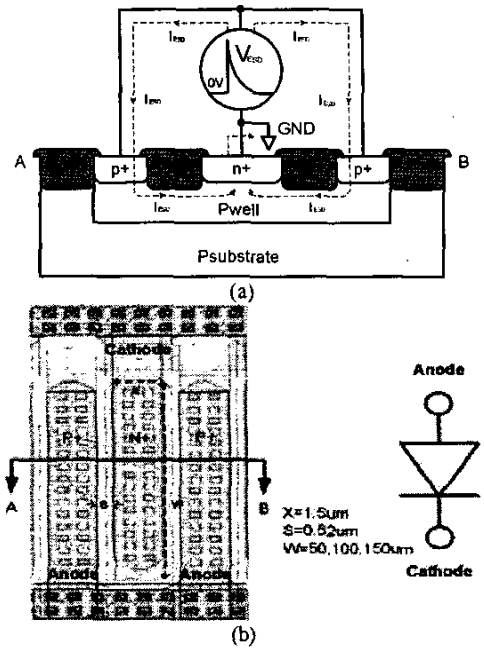


**Fig.2** (a) The schematic cross-sectional view of a STI diode. (b) The practical layout of a unit cell of the STI diode and its symbol.

### *B. Poly-gated Diode*

The poly-gated diode uses a poly gate to isolate its cathode (N+) and anode (P+). The schematic cross-sectional view of poly-gated diode is shown in Fig. 3(a). The N+ diffusion (cathode) and P+ diffusion (anode) are separated by the poly gate. In ESD condition, the ESD current path along the poly-gated diode is shown by the dashed line in Fig. 3(a). The ESD current would flow from P+ diffusion to N+ diffusion under the poly gate. Because the design rule of minimum gate length is smaller than the minimum STI length, the distance between N+ diffusion and P+ diffusion in the poly-gated diode can be shortened. Moreover, there is no STI isolation wall between N+ diffusion region and P+ diffusion region. The ESD current can flow the path under the poly gate directly. The route of ESD current in this poly-gated diode is shorter than that in the STI diode. The resistance of the ESD current path can be decreased. So, the ESD level will be increased in comparison to that of STI diode under the same layout area. But for the RF ESD application, the poly-gated diode has the additional gate oxide capacitance seen by the input pad. This will cause the RF performance to degrade more than STI diode. We would check it in a 0.25-μm salicided logic CMOS process by measuring power gain S21 and noise figure directly.

The practical layout of a unit cell of the poly-gated diode and its symbol are drawn in Fig. 3(b). The device cross-sectional view along the line C--D of Fig. 3(b) is corresponding to that drawn in Fig. 3(a). The N+ diffusion is drawn at the center of the cell, and the P+ diffusion connected to VSS surrounds the whole unit cell at the outside. The device layout parameters are shown in Fig. 3(b), too. X is the length of the N+ diffusion. L is the minimum length of the poly gate. W is the width of the N+ diffusion. The parameter of W was changed in the testchips to investigate the power gain S21, noise figure, and ESD level of these poly-gated diodes.

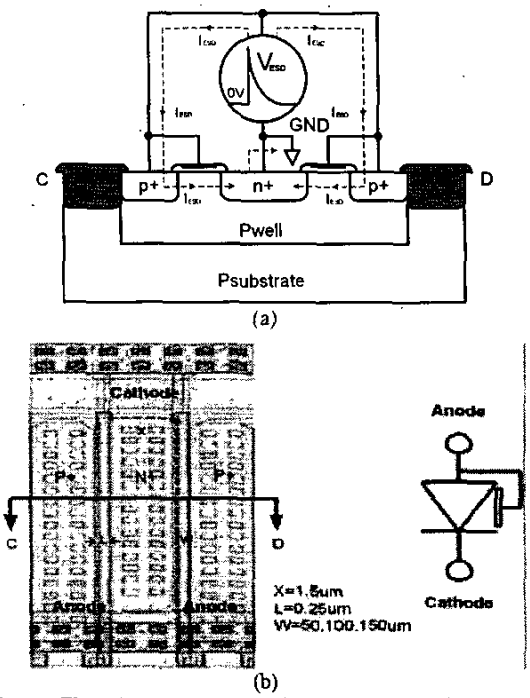


**Fig.3** (a) The schematic cross-sectional view of a poly-gated diode. (b) The practical layout of a unit cell of the poly-gated diode and its symbol.

## III. EXPERIMENTAL RESULTS

### *A. Power Gain S21*

The STI and poly-gated diodes with different device sizes had been fabricated in a 0.25-μm salicided CMOS process. The 20-GHz S-parameter measurement system HP85122A is used to measure the power gain (S21) of the fabricated STI diodes and poly-gated diodes under different device dimensions. It can measure the magnitude, phase, and group delay of two-port networks to characterize their circuit behavior. The power gain S21 of those fabricated diodes is measured from 1.2GHz to 6GHz with a step of 300MHz. The

experimental setup to measure power gain S21 of ESD device is shown in Fig. 4. The ESD device is connected between signal line and ground. The DC bias voltage in signal line is 1.25V. The input port is the 50ohm source and the output port is the 50ohm load.

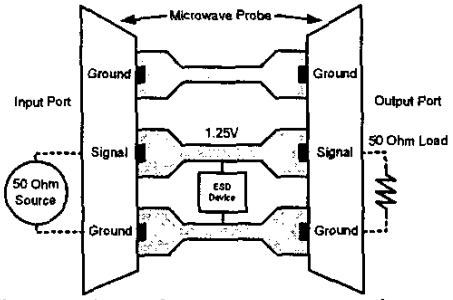


**Fig.4** The experimental setup to measure the power gain S21 and noise figure of ESD protection devices.

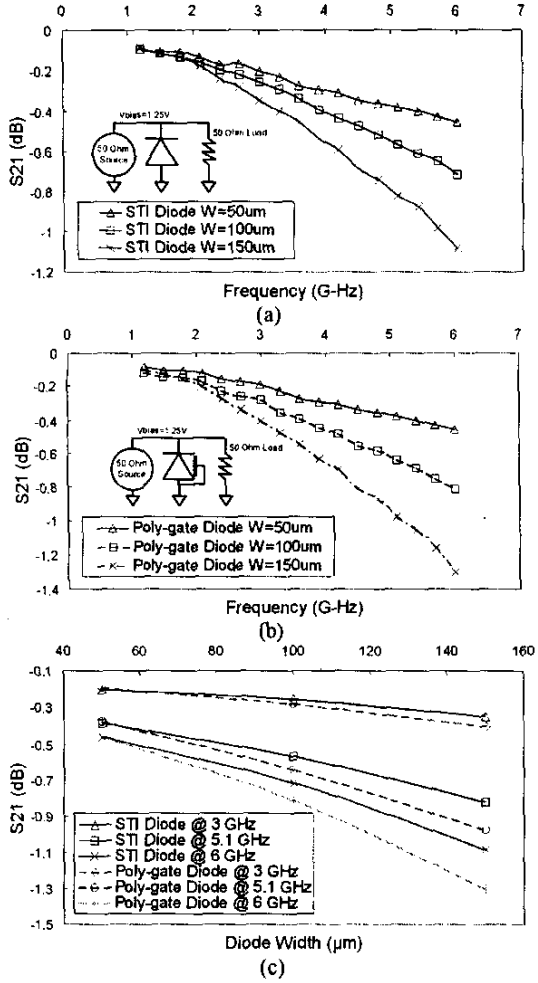


**Fig.5** (a) The S21 vs. frequency in different layout area of STI diodes as ESD devices. (b) The S21 vs. frequency in different layout area of poly-gated diodes as ESD devices. (c) The comparison on power gains S21 of STI diode and poly-gate diode at different operating frequency in different layout area.

The S21 vs. frequency of STI diodes in different layout area is shown in Fig. 5(a). The power gain S21 is decreased by STI diode in the same layout area when the operating frequency increases. The power gain S21 decreases drastically by STI diode with a larger layout area at a higher operating frequency. The difference of power gain S21 loss of the STI diodes with different layout area becomes larger at higher frequency. The larger parasitic capacitance of STI diode wastes more RF signal to ground and causes the power gain loss. The S21 vs. frequency of poly-gated diodes with different layout area is shown in Fig. 5(b). The variation on power gain S21 of the poly-gated diode is similar to that of STI diode. The comparison on power gain S21 at different operating frequency (3GHz, 5.1GHz, and 6GHz) among the STI diodes and poly-gated diodes with different layout area is shown in Fig. 5(c). The performance of poly-gated diode is worse than that of STI diode. The parasitic capacitance of poly-gated diode is more than that of STI diode because of the poly-gated oxide capacitance.

In order to further confirm the influence from ESD devices on RF circuits. A common-source NMOS amplifier with W/L=50μm/0.25μm is drawn with or without the ESD device to investigate the power gain S21. The measured power gain S21 of CS NMOS with different ESD devices is shown in Fig. 6. The gate and drain of NMOS are biased at 1.25V to make sure that CS NMOS operated in saturation region. At the 6GHz frequency, the CS NMOS has a power gain S21 of 3dB. After adding a single STI diode with width of 50μm, the power gain S21 is lowered to 2.44dB. After adding a single poly-gated diode with width of 50μm, the power gain S21 is lowered to 2.3dB. The power gain S21 is lower when the NMOS has ESD device. The poly-gated diode causes more power gain loss than the STI diode.

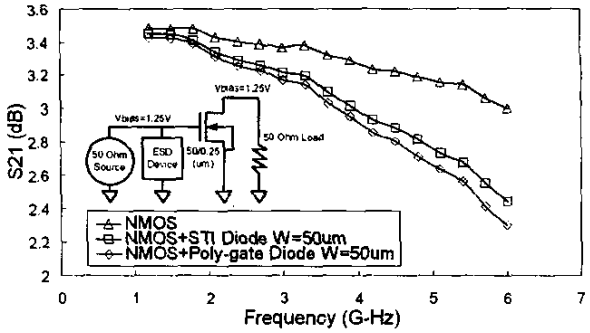


**Fig.6** The power gain S21 of CS NMOS with different ESD devices.

### *B. Noise Figure*

The high frequency noise parameter measurement system is used to measure the noise figure of the fabricated STI diodes and poly-gated diodes under different device dimensions. The noise figure in this work is measured from 1.2GHz to 6GHz with a step of 300MHz on the fabricated STI diodes and poly-gated diodes. The comparison of noise figure at different operating frequency (3GHz, 5.1GHz, and 6GHz) of the STI diodes and poly-gated diodes in different layout area is shown in Fig. 7. With the noise from measurement environment, the difference is hard to be figured out between poly-gated diode and STI diode. However, the noise performance of poly-gated diode is worse than that of STI diode. First reason is the parasitic capacitance of poly-gated diode is more than that of STI diode, because of the poly-gated oxide capacitance. Secondly, the parasitic resistance of

poly-gated diode is smaller than STI diode, because of using the poly gate to isolate N+ diffusion from the P+ diffusion in the diode structure. Two parasitic effects would increase the noise figure of the poly-gated diode.

### *C. ESD Robustness*

The *Zapmaster* ESD tester is used to evaluate the ESD robustness of the fabricated STI diodes and poly-gated diodes under different diode widths. The HBM (Human Body Model) ESD voltages from the ESD tester are controlled from 1000V to 8000V with a step of 200V. The MM (Machine Model) ESD voltages from the ESD tester are controlled from 50V to 425V with a step of 25V. The failure criterion for ESD level of the ESD diode is defined as the voltage of 1uA current shifting 30%. The HBM and MM ESD test results are summarized in Fig. 8. The poly-gated diodes can possess higher ESD level than STI diodes either in HBM or MM ESD stress.

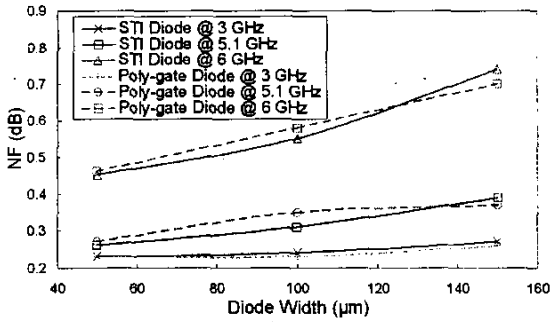


**Fig.7** The noise figure comparison of STI diode and poly-gated diode at different operating frequency in different layout area.

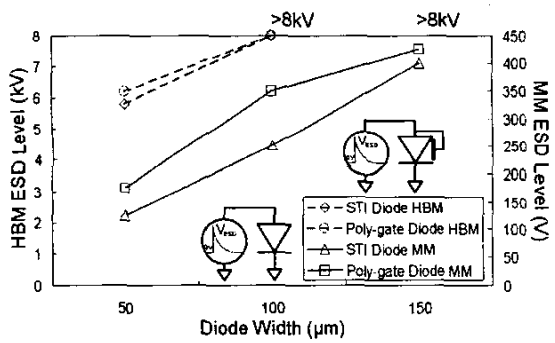


**Fig.8** The HBM and MM ESD level of forward STI diode and poly-gated diode.

### *D. Optimization on ESD and RF Performances*

Both of the STI diode and poly-gated diode have the advantages and disadvantages on RF performance and ESD robustness. In order to decide the most suitable diode structure for RF ESD application, the comparison between the STI diode and poly-gated diode on power gain S21 and MM ESD level is shown in Fig. 9. The basic requirement of MM ESD robustness is 200V at least. At the 200V MM ESD level, the power gain S21 of poly-gated diode is –0.51dB and that of STI diode is –0.61dB. The poly-gated diode has higher power gain S21 if the ESD requirement is fixed at some ESD specification (such as 200V MM ESD level). The comparison between STI and poly-gated diodes under the requirement of 200V MM ESD level is shown in Table I.

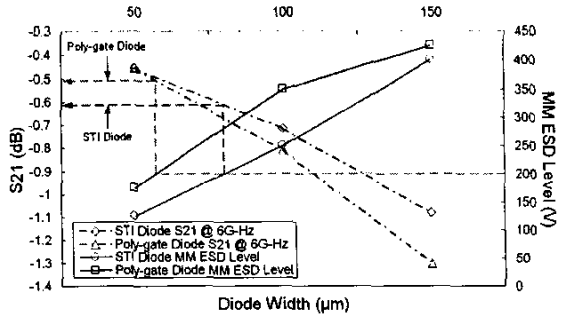


**Fig.9** The power gains S21 optimization of STI diode and poly-gated diode in 200V MM ESD level.

**Table I**

| *For 200V MM* | Width | S21 | Comparison |
|---|---|---|---|
| STI diode | 85 um | -0.61 dB | Bad |
| Poly-gate diode | 65 um | -0.51 dB | Better |

## VI. CONCLUSION

Two kinds of diode structures suitable for RF application have been practically investigated in a 0.25-μm CMOS process. By using the two-port GSG measurement, the power gain S21 and noise figure devoted by ESD devices had been extracted. The power gain S21 is degraded by ESD device with larger layout area and more serious at higher operating frequency. The noise figure is increased by ESD device with larger layout area and also is more serious at higher frequency. The ESD level and It2 both indicate that poly-gated diode has higher ESD level than that of STI diode under the same layout dimension. The poly-gated diode is more suitable as the ESD protection device for RF application.

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