Active Device under Bond Pad to Save I/O Layout for High-pin-count SOC

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Abstract

To save layout area for electrostatic discharge (ESD) protection design in the SOC era, test chip with large size NMOS devices placed under bond pads has been fabricated in 0.35-μm one-poly-four-metal (1P4M) 3.3V CMOS process for verification. The bond pads had been drawn with different layout patterns on the inter-layer metals to investigate the effect of bonding stress on the active devices under the pads. Threshold voltage, off-state drain current, and gate leakage current of these devices under bond pads have been measured. After assembled in wire bond package, the measurement results show that there are only little variations between devices under bond pads and devices beside bond pads. This result can be applied on saving layout area for on-chip ESD protection devices or I/O devices of IC products, especially for the high-pin-count system-on-a-chip (SOC).

1. Introduction

Design of bond pads has been ignored in IC design flow in the past because the chip design was not pushed to its limitation when using the conventional bond pad structure. As device feature sizes of IC technologies are shrunk more rapidly than the size of bond pad, and the number of I/O pins increases for more complex interfaces, the layout area occupied by bond pads in a silicon chip is getting larger. The increasing I/O pins and their layout area lead to more complex interconnection and increasing die cost. If the active devices of a chip can be placed under bond pads, the die cost would be reduced obviously, and the design flexibility would be also improved.

In general chip designs, active devices would not be placed under bond pads because circuit designers cannot make sure whether the device characteristics are still acceptable, or not, after the stress of packaging process. To make sure whether devices placed under bond pads are all right or not, there are some researches done in the past [1]-[3]. In those researches, studies of the gate leakage current [1], failure percentage after reliability tests [2], and second breakdown voltages [3] of devices placed under bond pads had been investigated. Besides, bond pads had been designed with some change from the conventional bond pad structure. To improve the bonding reliability, the metal layer beneath the most top metal layer of bond pad is suggested to be patterned [4]. To reduce the parasitic effect for high-speed I/O circuits, the low-capacitance bond pad structure had been reported with different layout patterns [5].

In this paper, the active devices under such low-capacitance bond pad structures to save layout area for high-pin-count IC's is studied and experimentally tested in a 0.35-μm CMOS process.

2. Test Chip Design to verify Devices under Bond Pads

To investigate whether the NMOS transistor placed under bond pad would be damaged by the wire bonding process or not, a set of device designs with NMOS transistors has been fabricated in a 0.35-μm 1P4M 3.3V CMOS process. Bond pads used in this experiment are all with a passivation window size of 86μm×86μm and a top metal size of 96μm×96μm. Besides, bond pad pitch in the silicon test chip is 116μm. All the NMOS transistors in the silicon test chip are drawn with the same feature size and layout style. The NMOS has total channel width of 2016μm and channel length of 0.5μm. The layout of the NMOS transistor is drawn in 21 fingers with each unit finger width of 96μm. The drain, gate, source, and bulk of NMOS are all connected to a standalone bond pad for each terminal in the silicon test chip.

The first device design, called as "Device-1", is constructed by four bond pads in line and a NMOS transistor between two of these bond pads. This traditional NMOS device, which is placed beside bond pads instead of under bond pad, is used as a reference device of the test chip. Experimental results from this reference device can be used as a set of basic reference data. The corresponding layout pattern of the bond pad in this device and its cross-sectional view are shown in Fig. 1(a) and Fig. 1(b), respectively. The dark area in center of Fig. 1(a) is shaped by a dozen of via plugs. From Fig. 1(b), it is clear that there is no any active device under the bond pad structure.

The "Device-2" design is constructed by four bond pads in line for the four terminals of a NMOS transistor, and a NMOS transistor placed directly under one of these bond pads. The layout view of the bond pad with a NMOS device under it in "Device-2" is shown in Fig. 2(a). The NMOS device symbol in Fig. 2(a) indicates that there is a NMOS device beneath the Metal-2 layer of this bond pad. Its corresponding cross-sectional view is

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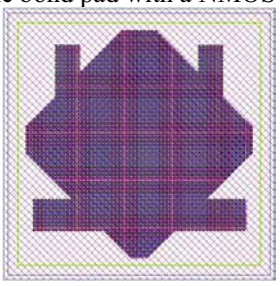
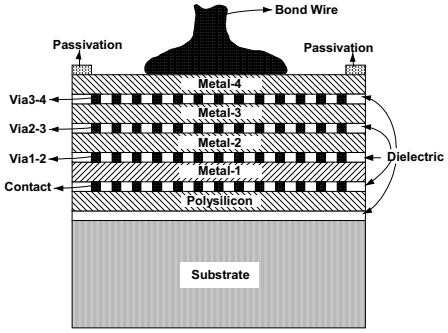
shown in Fig. 2(b). In Device-2, the layout drawings of Metal-2 and Metal-3 layers are kept as flat planes (or not patterned) for the bond pad with a NMOS device under it.



(a) Layout view of bond pad used in Device-1

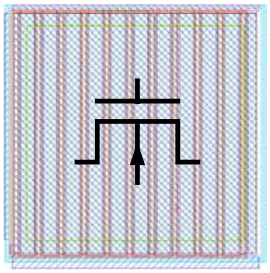


(b) Cross-sectional view of (a)

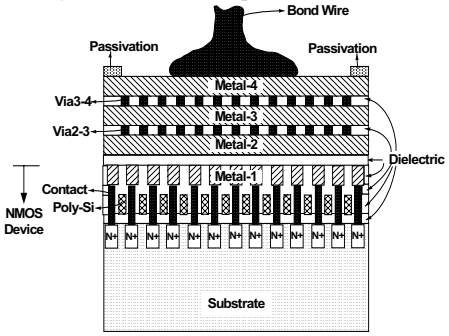
Fig. 1 (a) Layout pattern of the conventional bond pad used in Device-1, which is beside a NMOS transistor, and (b) the corresponding cross-sectional bond pad structure of (a).

The third design of the device group, which includes "Device-3", "Device-5", and "Device-7" designs, is constructed by four bond pads in line for the four terminals of a NMOS transistor, and a NMOS transistor placed directly under one of these bond pads. Fig. 3(a) shows the cross-sectional structure of the third design. The bond pad with a NMOS transistor placed under it is constructed by a NMOS transistor, which is placed under Metal-2 layer and a patterned Metal-3 layer. Metal-2 and Metal-4 layers of this designed bond pad are both in a large area of un-patterned plate. The corresponding layout views of the bond pads with a NMOS transistor under each of them in Device-3, Device-5, and Device-7 are shown in Fig. 3(b), Fig. 3(c), and Fig. 3(d), respectively. In Figs. 3(b)-(d), the NMOS device symbols on the bond pad layout patterns indicate that there is a NMOS transistor under the patterned metal layer(s) for each of these bond pads.

The fourth design of device group, which includes "Device-4", "Device-6", and "Device-8" designs, is also constructed by four bond pads in line for the four terminals of a NMOS transistor, and a NMOS transistor placed directly under one of these bond pads. In the fourth design, the bond pad with a NMOS transistor placed under it is composed of a NMOS transistor beneath Metal-2 layer and the metal layers, Metal-2 and Metal-3, with different layout patterns for each device. Metal-4 layer of the designed bond pad is in a large area of un-patterned plate for wiring bond.

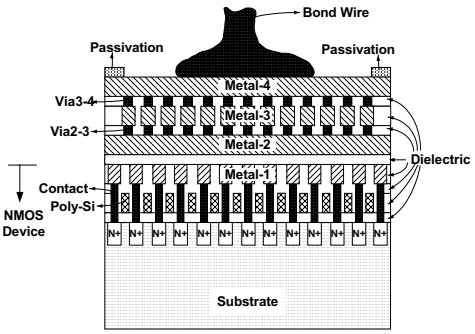


(a) Layout view of bond pad used in Device-2



(b) Cross-sectional view of (a)

Fig. 2 (a) Layout pattern of the bond pad with a NMOS transistor under Metal-2 in "Device-2", and (b) the corresponding cross-sectional bond pad structure of (a). The NMOS device symbol in (a) indicates that there is a NMOS device beneath the Metal-2 layer of this bond pad.

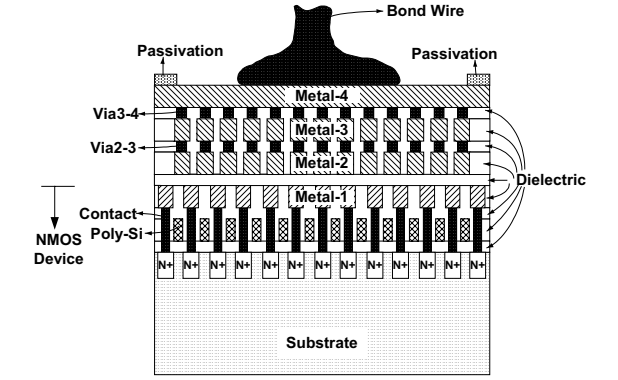


(a) Metal-3 patterned bond pad

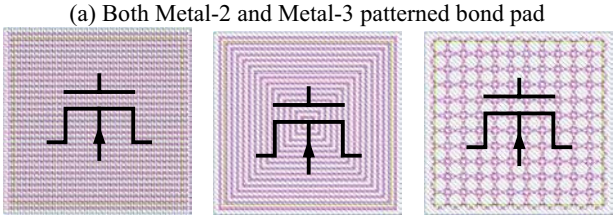
(b) Device-3 (c) Device-5 (d) Device-7

Fig. 3 Layout designs of bond pads with NMOS devices placed under Metal-2. (a) Cross-sectional bond pad structure of Metal-3 patterned devices, (b)-(d) show the patterned Metal-3 layer layouts of Device-3, Device-5, and Device-7, respectively. The NMOS device symbols on the bond pad layout patterns indicate that there is a NMOS transistor under the patterned metal layer(s) for each bond pad.

Cross-sectional view of the designed bond pad structure is shown in Fig. 4(a). The corresponding layout views of the bond pads with a NMOS transistor under each of them in Device-4, Device-6, and Device-8 are shown in Fig. 4(b), Fig. 4(c), and Fig. 4(d), respectively. In Figs. 4(b)-(d), the NMOS device symbols on the bond pad layout patterns indicate that there is a NMOS transistor under the patterned metal layer(s) for each of these bond pads.



(a) Both Metal-2 and Metal-3 patterned bond pad



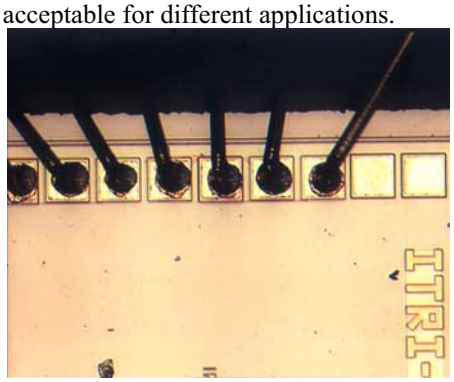
(b) Device-4 (c) Device-6 (d) Device-8

Fig. 4 Layout designs of bond pads with NMOS devices placed under Metal-2. (a) Cross-sectional bond pad structure of Metal-2 and Metal-3 patterned devices, (b)-(d) show the patterned Metal-2 and Metal-3 layouts of Device-4, Device-6, and Device-8, respectively. The NMOS device symbols on the bond pad layout patterns indicate that there is a NMOS transistor under the patterned metal layer(s) for each bond pad.

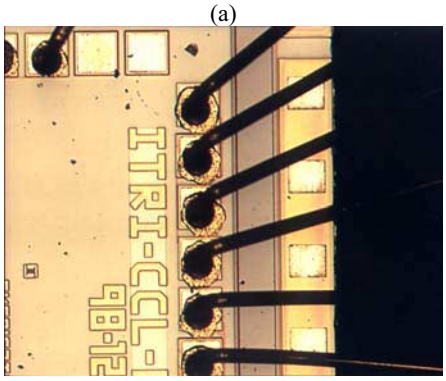
The designed patterns applied on Metal-2 and Metal-3 layers of the fourth design group are the same with the patterns applied on the Metal-3 layers of the third design group. In other words, the layout patterns of Metal-2 and Metal-3 layers in Device-4, Device-6, and Device-8 are the same with the layout patterns of Metal-3 layer in Device-3, Device-5, and Device-7, respectively. These designed layout patterns on metal layers, Metal-2 and Metal-3, and the active device region of bond pads are modified from the prior report on low-capacitance bond pad for high-frequency applications [5]. Therefore, except saving layout area of a silicon chip, the parasitic capacitance of the proposed bond pad design can be lowered when comparing with that of a conventional bond pad.

3. Experimental Results

The purpose of the proposed bond pad design is to make sure whether the NMOS transistor placed under bond pads with different Metal-2 and Metal-3 layout patterns would be damaged by the assembly process steps or not. First step of the verification work is to measure the wafer-level DC characteristics of the NMOS transistor in the designed devices. By probing the four terminals of each NMOS transistor on the wafer, the NMOS DC characteristics before wire bonding can be measured by HP4155 semiconductor parameter analyzer. The threshold voltage (Vt) of all the NMOS transistors on the test chips should be within the range listed on the process control management (PCM) specification released by foundry [6]. The off state drain current (Ioff) with drain voltage (VD) biased at VDD level of 3.3V and the gate leakage current (IG) with gate voltage (VG) biased at VDD level should be both acceptable for different applications.



(a)



(b)

Fig. 5 The bond ball sizes are (a) not dispersed by 1× of normalized bonding force (50g), and (b) dispersed obviously by 1.75× of normalized bonding force (87.5g). Adjacent bond pads might be connected together by the dispersed bond balls caused by a larger bonding force.

After the wafer-level measurements, assembly of the test chip samples is then taken in two different types of package : side-brazed dual-in-line (DIP) package and plastic DIP package. The side-brazed package is a kind of package with its leadframe uncovered by plastic molding compound. Thermal stress of the compound molding process and the mismatch of coefficients of thermal expansion (CTE) after compound molded could cause device performance degradation of the NMOS transistors placed under bond pads. Consequently, the purpose of

performing these two types of packages is to verify whether the performance of NMOS transistors would be further degraded by the compound molding process or not. The wire bonders for side-brazed package and plastic package are Panasonic HW22U-H and ESEC 3008, respectively.

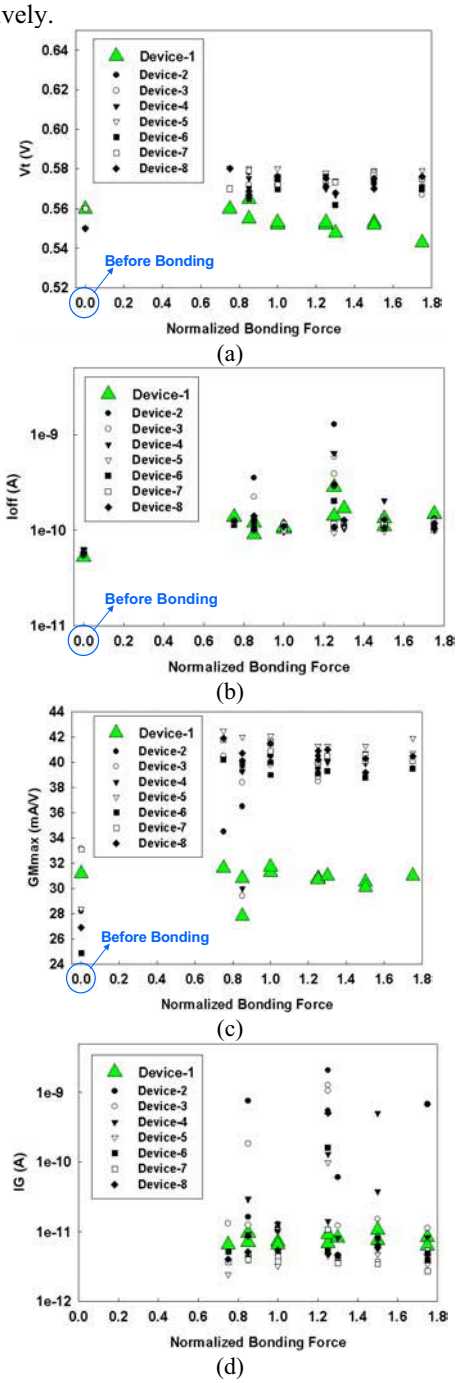


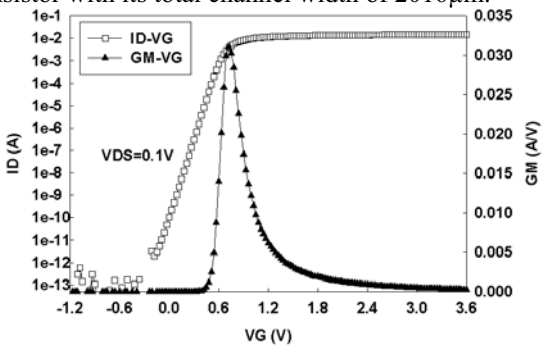
Fig. 6 The impacts of wire bonding force on device DC characteristics of (a) threshold voltage (Vt), (b) off-state drain current (Ioff), (c) maximum gm (GMmax), and (d) gate leakage current (IG) of NMOS transistors beside bond pads (Device-1) or beneath patterned metal layers of bonding pads (Device-2 ~ Device-8).

The DC I-V characteristics of NMOS transistors after assembly for both types of packaged IC's were measured. While comparing with the wafer-level measurement data, if the gate leakage current (IG), off state drain current (Ioff), or the threshold voltage (Vt) of NMOS transistor in the test chip are shifted obviously after assembly process steps, it is known that the device performance is affected by the wire bonding process or the compound molding process.

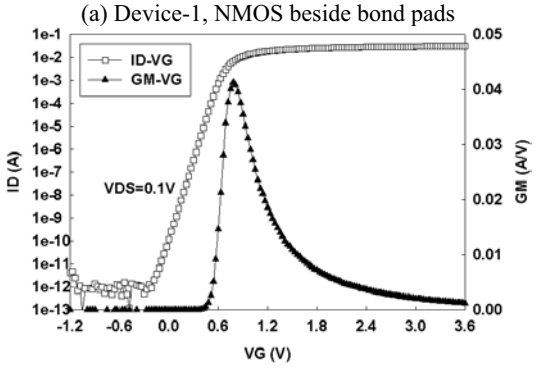
For the samples with side-brazed DIP package, normal bonding force of the corresponding wire bonder, Panasonic HW22U-H, is 50g and normal treated bonding power is 80mW. The applied bond ball diameter is 100μm (or 4mil) and the taken bond wire diameter is 25.4μm (or 1mil) in the experiments. To make sure whether the device performance of the NMOS transistor placed under bond pad would be affected by the wire bonding force or not, the applied wire bonding force was controlled and split into several conditions. The split conditions of wire bonding force are 0.75×, 0.85×, 1×, 1.25×, 1.3×, 1.5×, and 1.75× of normal wire bonding force of 50g. In other words, the applied wire bonding forces are 37.5g, 42.5g, 50g, 62.5g, 65g, 75g, and 87.5g for each split condition. When the wire bonding force is increased, the bond ball on the bond pad would be spread into a more unexpected shape with a larger occupied area. For wire bonding force larger than 87.5g, the shape of bond ball would be spread into an unacceptable larger area, which could lead to the short circuit phenomenon of bond balls on adjacent bond pads. Fig. 5 shows the optical microscope (OM) photos of bond balls on bond pads applied with different wire bonding forces. For the samples with plastic DIP package, normal bonding force of the corresponding wire bonder, ESEC 3008, is 51g and normal treated bonding power is 850mW. The applied bond ball diameter is about 80μm (or 3.1mil) and the taken bond wire diameter is 30.5μm (or 1.2mil) for the experiments. The molding process temperature for these samples is 175°C, which is a conventional temperature degree for compound molding process.

Fig. 6 shows the impacts of wire bonding force on the DC characteristics of NMOS transistors for different designed devices in the test chip. Results in Fig. 6 are from the samples assembled by side-brazed packages, which are not treated by the compound molding process. In Fig. 6, measurement results of Device-1 design, which is known as a NMOS transistor beside bond pads, are highlighted by relatively larger size triangle symbols as a reference level. The x-axes of Fig. 6 are the normalized bonding forces, which are the actually applied wire bonding forces normalized by a normal bonding force of 50g. In other words, 1× of normalized bonding force equals to applied wire bonding force of 50g; 0× of normalized bonding force means device characteristics before applying wire bonding force (the wafer-level measurement results). Fig. 6(a) shows the relationship between threshold voltage (Vt) and normalized wire bonding force. It is clear that the variation range of NMOS threshold voltage (Vt) is only from 0.54V to

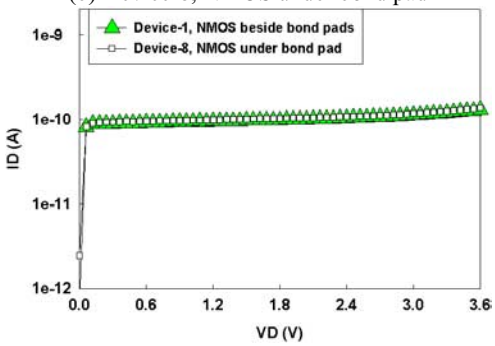
0.58V after different levels of wire bonding force. Fig. 6(b) shows the relationship between off state drain current (Ioff) and normalized wire bonding force. Although there is a larger range of variation for the results of applying 1.25× of normalized wire bonding force (62.5g), the off state drain current (Ioff) is still in the order of 1nA, which is reasonable for a large NMOS transistor with its total channel width of 2016μm.



(a) Device-1, NMOS beside bond pads



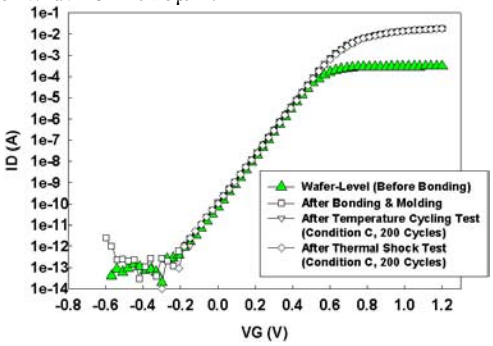
(b) Device-8, NMOS under bond pad



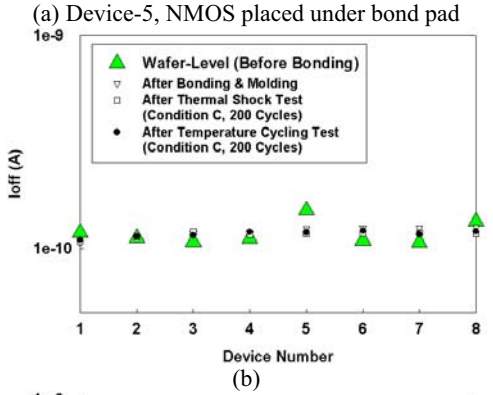
(c) ID-VD curves

Fig. 7 Comparison of device DC characteristics after compound molding. (a) ID-VG curve of Device-1, (b) ID-VG curve of Device-8, and (c) ID-VD curves of Device-1 and Device-8.

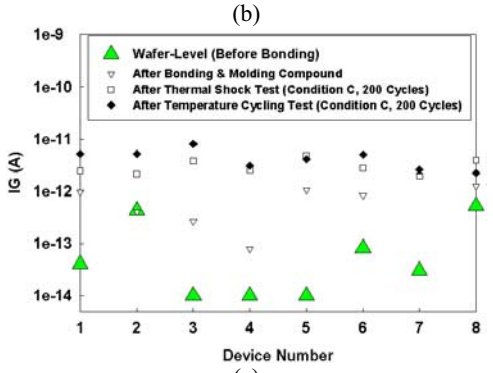
Fig. 6(c) shows the relationship between maximum transconductance (GMmax) and normalized wire bonding force. When comparing with the Device-1 design, results of other devices in Fig. 6(c) are shifted about 50%. Fig. 6(d) shows the relationship between gate leakage current (IG) and normalized wire bonding force. Although the results in Fig. 6(d) varies from the order of 10pA to the order of 1nA when comparing with the Device-1 design, it is still very small for a NMOS transistor with large channel width of 2016μm.



(a) Device-5, NMOS placed under bond pad



(b)



(c)

Fig. 8 The dependencies of device DC characteristics on assembly process steps. (a) Drain current (ID) versus gate biased voltage (VG) of NMOS device placed under bond pad, (b) off-state drain current (Ioff) versus varied designed devices after specific assembly process step, and (c) gate leakage current (IG) versus varied designed devices after specific assembly process step.

Fig. 7 shows the measurement data from plastic DIP packaged samples. The drain current (ID) and transconductance (GM) with drain-source voltage (VDS) biased at 0.1V versus gate biased voltage (VG) after compound molding for Device-1 and Device-8 are shown in Fig. 7(a) and Fig. 7(b), respectively. For Fig. 7(a) and Fig. 7(b), the x-axis and left hand y-axis are the gate biased voltage (VG) and the measured drain current (ID) of the NMOS transistor, respectively. The right hand y-axis is the transconductance (GM) of NMOS transistor. Although the drain current (ID) with gate voltage (VG)

biased at –1.0V is changed from 0.1pA of Fig. 7(a) to several pA of Fig. 7(b), the variation is very small for the NMOS transistor with large channel width of 2016μm. Besides, the VG value at maximum transconductance (GM) value are almost the same for both Fig. 7(a) and Fig. 7(b). This indicates that the threshold voltage of the NMOS transistor is not shifted obviously for NMOS transistors placed beside or under bond pads. The drain current (ID) versus drain biased voltage (VD) of Device-1 and Device-8 NMOS with other terminals (gate, source, and bulk) shorted to ground after compound molding are shown in Fig. 7(c). The x-axis and y-axis of Fig. 7(c) are the drain biased voltage (VD) and the drain current (ID) of the NMOS transistor, respectively. From Fig. 7(c), the curve with triangle symbols is from Device-1 with NMOS transistor beside bond pads, and the curve with rectangular symbols is from Device-8 with NMOS transistor under bond pad. So, it can be concluded that the off state drain current (Ioff), which is defined as the drain current amplitude while drain voltage biased at VDD level of 3.3V and the other terminals connected to ground level of 0V, is kept in the same order of 100pA for NMOS placed beside and under bond pads after compound molding process.

Fig. 8 compares the measurement results from the wafer-level NMOS transistors and the plastic DIP packaged samples. After assembly processes applied on these samples, both thermal shock and temperature cycling tests were applied onto the samples. Both thermal tests were applied with 200 cycles for each in condition C (-65°C ~ 150°C) of US military standard MIL-STD-883E [7]-[8]. Fig. 8(a) shows the relationship between the drain current (ID) and the gate biased voltage (VG) in the subthreshold region with 0.1V drain biased voltage for Device-5 with NMOS transistor placed under the bond pad. There are four curves in Fig. 8(a), which were measured from the samples at different conditions. These four curves are almost overlapped into one curve in the subthreshold region of the NMOS transistors. This indicates that the switching speeds of the NMOS transistors were neither degraded by the assembly process steps, nor by the thermal tests applied on the samples.

Fig. 8(b) shows the relationship between the off state drain current (Ioff) and different devices in the test chip. It indicates that there is no difference on Ioff among different devices for varied split conditions. In other words, the off state drain currents (Ioff) of the NMOS transistors on the samples of designed test chip were not affected by the assembly process steps or the applied thermal tests.

Fig. 8(c) shows the relationship between the gate leakage current (IG) and different devices in the test chip. From Fig. 8(c), the gate leakage current (IG) after the assembly process steps was increased by 1~2 orders when comparing with the wafer-level measurement data. The gate leakage current (IG) after the thermal tests was increased by 2~3 orders when comparing with the wafer-level measurement data. Although the gate leakage currents are increased, they are still below 10pA for a NMOS transistor with its channel width of 2016μm.

4. Conclusion

The NMOS transistor placed under bond pad has been verified in a 0.35-μm 1P4M 3.3V CMOS process. DC characteristics of test-chip samples were measured for 4 major steps of assembly, which are known as wafer-level probing, after wire bonding (side-brazed DIP package), after compound molding (plastic DIP package), and after life time thermal tests (thermal shock and temperature cycling tests). By a series of experimental investigations (changing wire bonding force applied on bond pads, additional compound molding process, and thermal reliability tests) and DC characteristics measurements, the device performances of NMOS transistors placed under bond pads have been proved to be with only little variation. These results are still acceptable for general digital CMOS IC products to save chip layout area. Therefore, not only ESD protection devices or I/O devices can be placed under bond pads for different applications, but also the parasitic capacitance of bond pad can be reduced by the patterned metal layers and the N+ diffusion region beneath the bond pad. Without any extra process steps, the devices under bond pads make the chip layout placement more flexible and have the advantage of cost reduction for high-pin-count IC products.

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