Novel Electrostatic Discharge Protection Design for Nanoelectronics in Nanoscale CMOS Technology

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Abstract—**A novel electrostatic discharge (ESD) protection concept by using the *already-on* device is proposed to effectively protect CMOS integrated circuits (IC) in nanoscale CMOS processes against ESD stress. Such an already-on NMOS device is designed to have a threshold voltage of ~0V, or even negative. When the IC is under the ESD zapping conditions, such already-on NMOS in CMOS IC are initially standing in the turn-on state and ready to discharge ESD current during any ESD zapping. So, such already-on NMOS has the fastest turn-on speed and the lowest trigger-on voltage to effectively protect the internal circuits with a much thinner gate oxide (~15Å) in future sub-100nm CMOS technology. To keep such already-on devices off when the IC is under normal circuit operating condition, an on-chip negative voltage generator realized by the diodes and capacitors is used to bias the gates of such already-on devices. The proposed already-on device and the on-chip negative voltage generator are fully process-compatible to the general sub-100nm CMOS processes.**

Keywords-Electrostatic Discharge (ESD); already-on device; threshold voltage; gate oxide; negative voltage generator.

I. INTRODUCTION

ESD damage has become the main reliability issue for CMOS IC products fabricated in the sub-quarter-micron CMOS processes. In the past, the on-chip ESD protection devices in CMOS ICs were realized by the NMOS/PMOS, field-oxide device (FOD), diode, parasitic BJT, or even the SCR devices. Such traditional ESD protection devices are initially kept off in CMOS ICs under ESD zapping condition. The applied overstress ESD voltage causes the junction breakdown to trigger on such traditional ESD protection devices, and then the ESD current is discharged through them. Among these traditional ESD protection devices, they have a relatively higher breakdown voltage or a higher trigger-on voltage. To effectively protect the thinner gate oxide in deep-submicron CMOS processes, the gate-coupled [1]-[3] or the substrate-triggered [4]-[7] circuit techniques had been used to reduce the trigger-on voltage and to enhance the turn-on speed of the traditional ESD protection devices. However, in the sub-100nm CMOS process, the gate oxide will be scaled down to only ~15Å. To protect such much thinner gate oxide, the trigger-on speed of on-chip ESD protection devices must be further enhanced, or the trigger-on voltage of ESD protection devices must be reduced lower enough, to clamp the overstress ESD voltage. It has become a big challenge to effectively protect such much thinner gate oxide in the future sub-100nm CMOS IC products.

In this paper, a novel ESD protection methodology by using the already-on devices as the on-chip ESD protection devices is proposed to effectively protect CMOS IC products in the future sub-100nm CMOS processes. Such already-on NMOS devices are designed to have a ~0V, or even negative, threshold voltage. When the IC is floating without any power bias, such already-on NMOS devices in CMOS IC are initially in the turn-on state to discharge any ESD-stress current. When the CMOS IC is under normal circuit operating condition, such already-on NMOS devices are turned off by a negative gate voltage. The on-chip negative voltage generator can be realized by using the polysilicon diodes [8] and the capacitors, which are all isolated from the common p-type substrate. In this work, the proposed ESD protection design has been successfully verified in a 130-nm CMOS process. The already-on NMOS device and the on-chip negative voltage generator can be fully process-compatible to general nanoscale CMOS processes.

II. THE ALREADY-ON (NATIVE) DEVICE

A. Device Structure

As the device scaling down, the twin-well technology is necessary to balance the device characteristics of NMOS and PMOS devices. The normal NMOS and PMOS devices in the sub-quarter-micron process have been formed in the P-well and N-well, respectively. The already-on device proposed in this paper for ESD protection design is built neither in the P-well nor in the N-well, but it is directly in the p-substrate, as those shown in Fig. 1. The p-substrate region is the reverse tone of both P-well and N-well regions, which can be generated by the logic operation in layout tool. The device is established in the native p-substrate region, so it is also called as "native device".

The detail device structures with different doping profiles of the normal NMOS device and the proposed already-on device in a standard twin-well CMOS process are compared in Figs. 2(a) and 2(b). The main difference between these two devices is that the normal device has the normal impurity doses, which include the P-well implant, the anti-punchthrough implant, the pocket implant, and the channel implant. These implants for normal NMOS are all with p-type impurity doses, and they are realized by using the same P-well mask in present sub-130nm CMOS process for cost reduction. But, the already-on device, which is realized without using the P-well mask, only has the p-type pocket implant in the channel region and the n-type LDD implant. In lack of the normal three p-type

impurity doses, the already-on device has a very low threshold voltage (~0V) and high electron mobility in its channel region.

Such already-on device can be fully process-compatible to general sub-quarter-micron CMOS processes, which have the separated N-well and P-well masking layers during wafer fabrication. Of course, if an extra threshold implant is included into the CMOS process, the NMOS device in P-well region can be also adjusted to have a ~0V (or even negative) threshold voltage. But, this needs an extra mask layer and increases the fabrication cost.
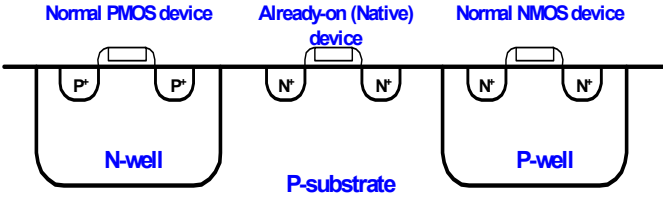

Fig. 1 The device cross-sectional views of the normal NMOS, normal PMOS, and the proposed already-on (native) NMOS device in a p-substrate twin-well CMOS technology.
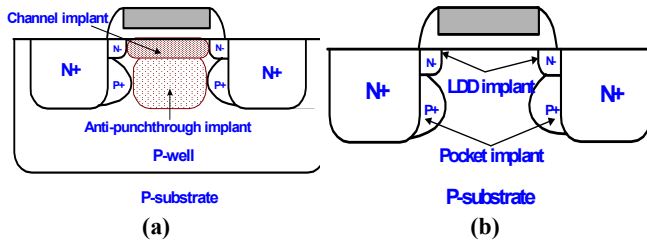

Fig. 2 The detailed device structures of (a) the normal NMOS device, and (b) the proposed already-on (native) NMOS device, in a p-substrate twin-well CMOS technology.

B. DC Characteristics of the Already-on (Native) Device

To use the already-on device as effective ESD protection device in CMOS ICs, the DC I-V characteristics must be investigated first. The proposed already-on NMOS in Fig. 2(b) had been fabricated in a 130-nm STI CMOS process without using any extra mask layer in wafer fabrication. The Ids-Vgs characteristics of the fabricated already-on device and the normal NMOS under Vds of 0.1V are measured by hp4155 and shown in Fig. 3. The threshold voltage is extracted by the standard maximum Gm method. The already-on NMOS device with a channel length of 0.2μm has a threshold voltage of ~0.22V, but the normal NMOS with the same channel length has a threshold voltage of 0.41V. Under 0-V gate bias, the already-on device (the normal NMOS) with W/L of 360μm/0.2μm has a leakage current about ~6μA (~13nA). With more negative gate bias (-0.3V), the leakage current of the already-on device can be reduced to ~ 0.3nA. However, the leakage current of the already-on device is still larger than that of the normal NMOS. The reason is that the already-on device without anti-punchthrough implant in its channel region has a DIBL (Drain Induced Barrier Lowering) effect that could not be turned off easily only by a negative gate bias. With a much lower threshold voltage, such already-on devices in on-chip ESD protection circuits can be quickly turned on to discharge ESD current without involving any junction breakdown.
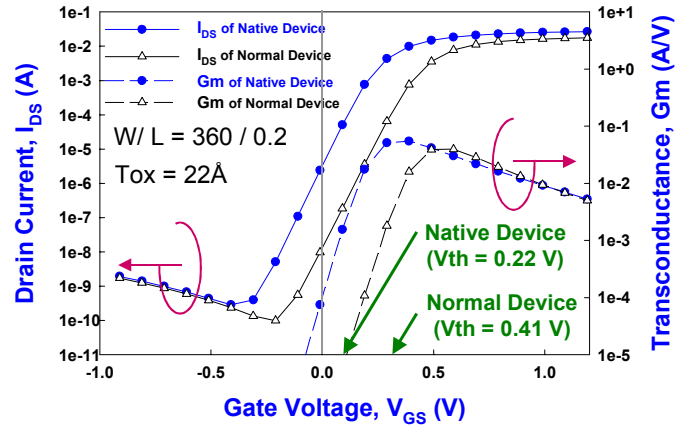

Fig. 3 The measured DC I-V curves and the Gm curves of the fabricated already-on (native) device and the normal NMOS. The threshold voltage (Vth) is extracted by the maximum Gm method.

C. TLP Characteristics of the Already-on (Native) Devices

The TLP-measured I-V curves of the fabricated already-on device and the normal NMOS with different channel lengths are shown in Fig. 4. The already-on device has obvious punchthrough I-V characteristics, but the normal device has snapback I-V characteristics due to the different conducted mechanism among the two devices. The It2 (second breakdown current) of already-on device with the same channel length is higher than that of normal device. Moreover, the Vt2 (second breakdown voltage) of the already-on device under the same current level is small enough to avoid oxide breakdown.
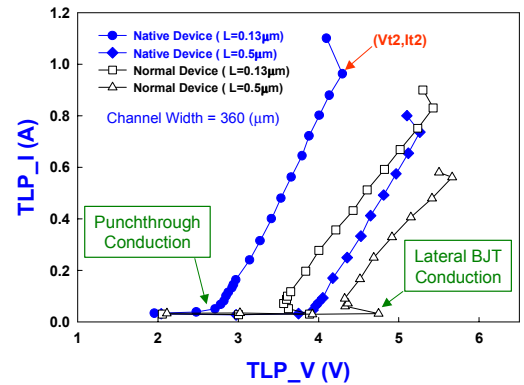

Fig. 4 The TLP-measured I-V curves of the already-on (native) device and the normal device under different channel lengths.

The ESD turn-on characteristics, including holding voltage (V_hold) and trigger-on voltage (Vt1), of the already-on device and the normal NMOS under different channel lengths are measured by transmission line pulsing (TLP) system and shown in Fig. 5. Only the V_hold of already-on device is shown in the figure due to the Vt1 is equal to the V_hold. This is because the punchthrough current conducts in the surface channel. The V_hold of already-on device with a short channel is lower than that with a long channel length due to the DIBL effect (one of the short channel effect) is serious in shorter channel length. On the other way, the Vt1 of the normal device depends on the breakdown of p-n junction. So, the Vt1 of the normal device is

almost constant. Moreover, the V_{hold} of normal device decreases with the channel length shrinking due to the efficiency of lateral BJT becomes high in a shorter base region. With the superiority of lower Vt1 and V_{hold}, the already-on device has the fastest turn-on speed and higher ESD robustness.
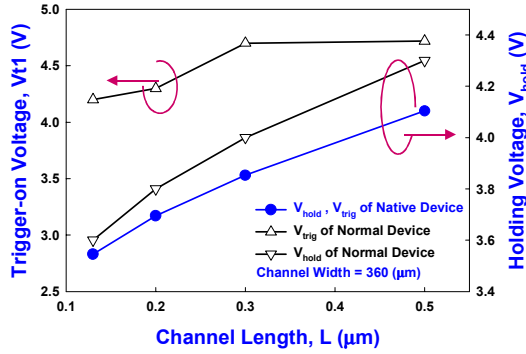

Fig. 5 The dependences of the trigger-on voltage (Vt1) and the snapback holding voltage (Vhold) of the already-on (native) device and the normal NMOS on the channel lengths.

The dependences of It2 and turn-on resistance (R_{on}) of the already-on device and the normal device on different channel lengths are compared in Fig. 6. The It2 of already-on device is linearly increased as the channel length is shrunk, which can be explained to reduce R_{on} in a shorter channel device. The turn-on resistance of the already-on device is lower about 1Ω than that of normal device with the same channel length. Therefore, the already-on device with a lower V_{hold} and smaller R_{on} has higher It2 (ESD robustness) than that of normal device on the same channel length.
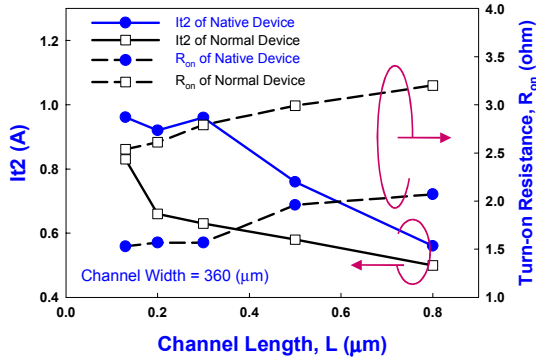

Fig. 6 The dependences of the It2 and turn-on resistance of the already-on (native) device and the normal NMOS on different channel lengths.

III. ESD PROTECTION WITH ALREADY-ON (NATIVE) DEVICES

A. ESD Clamp Cells with Already-on (Native) Devices

With the superiority of the low trigger-on voltage and high ESD robustness, the already-on device can be used stand alone as the ESD clamp device in Fig. 7(a) for on-chip ESD protection. It can be also used as a control device to quickly trigger on other ESD clamp devices to discharge ESD current. In Fig. 7(b), the ESD clamp device is realized by a field-oxide device (FOD) which is controlled by the already-on device

through its substrate. The TLP-measured I-V curves of the combined ESD clamp cell and stand-alone FOD device are compared in Fig. 8. Although the It2 of the combined ESD clamp cell is a little smaller than that of the stand-alone FOD, the Vt1 of this combined ESD clamp cell has a ~ 7V reduction from that of the stand-alone FOD. With a lower Vt1, it can provide much better protection for the internal circuits with thinner gate oxide. To turn off such ESD clamp cells with already-on devices, a negative voltage (~ -0.3V) is applied to the gate of every already-on device during the normal circuit operating condition. This can be achieved by suitable circuit design.
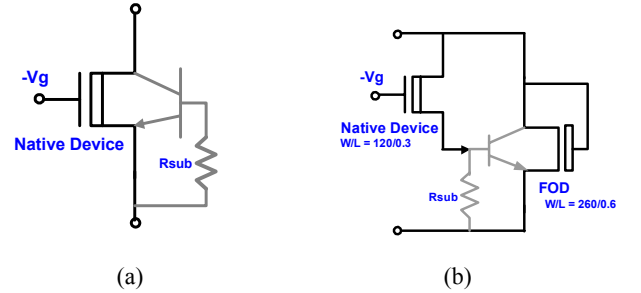

(a)   (b)

Fig. 7 The ESD clamp cells realized by (a) the already-on (native) device, and (b) a field-oxide device controlled by the already-on (native) device.
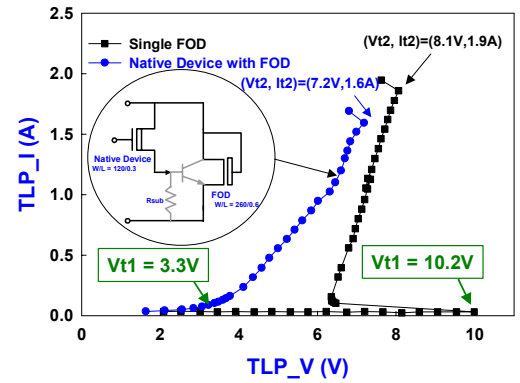

Fig. 8 The TLP-measured I-V curves of the combined ESD clamp cell and a stand-alone FOD device.

B. Whole-Chip ESD Protection Scheme

With the initial turn-on characteristics of the already-on device, the ESD clamp cells in Fig. 7 have the fastest turn-on speed to discharge ESD current, when the ESD voltage is zapped to the pad. One of the whole-chip ESD protection designs with the ESD clamp cells of already-on devices is shown in Fig. 9. In Fig. 9, the ESD clamp cell is connected between every pad and the common ESD path. The gates of already-on devices in all ESD clamp cells are biased by a negative bias line. This negative bias is generated from an on-chip negative voltage generator. When the IC is under normal circuit operating condition with power supplies, the negative voltage generator can automatically generate a negative voltage from the normal power supplies [9]. When the IC is floating without any power supplies, there is no output voltage generated from the negative voltage generator to the negative bias line. Therefore, under ESD zapping condition (the IC is initially floating), the ESD clamp cells in the whole-chip ESD

protection scheme without negative bias are initially standing in their turn-on states to discharge the positive or negative ESD voltages under any pin combination (I/O pin to I/O pin, I/O pin to power pin, and VDD pin to VSS pin) of ESD test. Such ESD protection design with the already-on devices is quite different to the traditional ESD protection circuits.
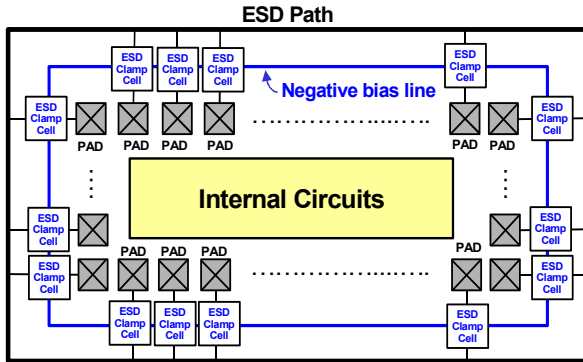

Fig. 9 The whole-chip ESD protection design with the ESD clamp cells of already-on (native) devices connected between every pad and the common ESD path in the CMOS IC.

C. *Negative Voltage Generator with Polysilicon Diodes*

To turn off the already-on devices under normal circuit operating condition, an on-chip negative voltage generator [9] is built into the CMOS chip. The traditional negative pump circuit realized by MOS or diodes cannot be directly used in this situation, because of the grounded common p-substrate. The polysilicon diodes [8] with fully isolated junction from the common p-substrate can be use to realize the negative voltage generator. The junction-isolated negative voltage generator is shown in Fig. 10, where all the diodes are realized by the polysilicon diodes. With a 0-to-2.5V clock voltage (it can be generated from an on-chip ring oscillator) as the input source Vs, this negative voltage generator can generate a negative voltage which is stored on the capacitor C2. By adjusting the number of stacked diodes in the diode string (PD1 ~ PDn), the output voltage (Vout) can be clamped to different negative voltage levels.
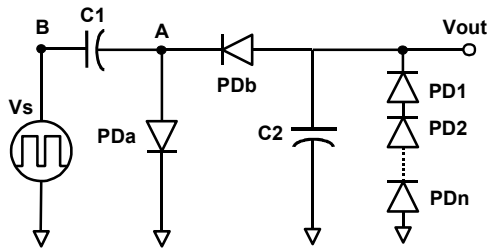

Fig. 10 The on-chip negative voltage generator realized by the polysilicon diodes and capacitors.

The measured output voltage level of the negative voltage generator with a 0-to-2.5V 1-MHz clock input (Vs) is shown in Fig. 11. With only a polysilicon diode in the diode string, Vout is clamped to -0.62V. When two polysilicon diodes are used in the diode string, Vout is clamped to -1.24V. This has successfully verified the effectiveness of the proposed negative voltage generator to turn off all already-on devices in the on-

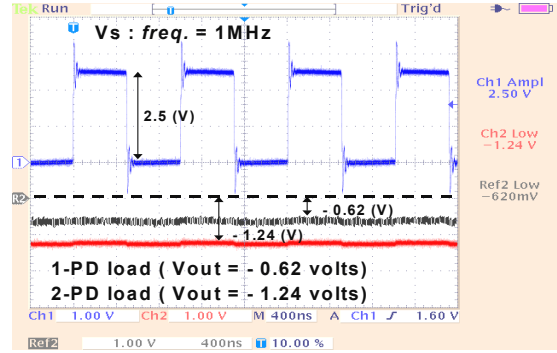chip ESD protection circuits under normal circuit operating condition.

Fig. 11 The measured output voltage levels of the negative voltage generator under a 0-to-2.5V clock input with different numbers of stacked polysilicon diodes in the diode string.

IV. CONCLUSION

A novel ESD protection design concept with the *already-on* (native) device is quite different to the traditional ESD protection circuits. With this novel ESD protection concept, the much thinner gate oxide in sub-100nm CMOS process or the future nanoscale CMOS technology can be still safely protected against ESD damage. The already-on (native) device has been investigated in a 0.13μm CMOS process. Moreover, not only the on-chip negative voltage generator for leakage consideration but also the whole-chip ESD protection with this already-on (native) device has been successfully demonstrated in this work.

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