A Novel LC-Tank ESD Protection Design for Giga-Hz RF Circuits

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Abstract — **To further decrease the power gain loss and noise figure of RF LNA circuit from the on-chip ESD protection circuit. A novel LC-tank RF ESD protection circuits is proposed in this paper and has been successfully verified in a 0.25-μm CMOS process with top thick metal. With the resonance of LC-tank, the LC-tank RF ESD protection circuit can reduce the power gain loss and noise figure at the operation frequency from ESD device. From the experimental results, the 4.5 circles inductor of LC-tank is the best choice for the requirement of 2kV HBM ESD level. The proposed LC-tank ESD protection circuit will be one of the most effective ESD protection solutions for RF circuits in higher frequency band (>10GHz).**

I. Introduction

The parasitic effects of on-chip ESD clamp devices on the I/O pad often degrade power gain S21 and increase the noise figure in RF circuit, especially the LNA input stage. There are some requests on ESD clamp devices in giga-Hz RF circuits: low parasitic capacitance, insensitive to substrate coupling noise, and good enough ESD robustness [1]. The traditional input ESD clamp device is gate-grounded NMOS (GGNMOS). But, the GGNMOS with a larger device dimension and a wider drain diffusion junction contributes a larger parasitic drain capacitance to the input pad, which is not suitable for RF ESD application. A typical request on maximum loading capacitance for RF ESD protection device was specified as ~200fF [2]. In order to fulfill such a tight specification, diodes are commonly used for ESD protection in RF LNA. Moreover, by adding a turn-on efficient ESD clamp circuit across the power rails of ESD protection circuit formed by double diodes, the overall ESD level of RF input pin had been significantly improved [3].

In this paper, a novel on-chip ESD protection design with LC-tank to tune out the parasitic effects from the ESD clamp devices for giga-Hz RF applications is first reported in the literature. The LC-tank is designed to resonant at the operation center frequency of RF circuits. So, the RF input port will see infinite impedance through ESD clamp devices with the LC-tank. The proposed LC-tank ESD protection circuits with different combinations of L and C values, but all resonating at 2.7 GHz, have been designed and verified in a 0.25-μm CMOS process.

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II. Impact of ESD Devices on RF Performance

For an input pin, there are four ESD-stress modes [1], in which the positive or negative ESD pulse is applied to an input pin with the VDD or VSS pins relatively grounded. To provide comprehensive protection against such four-modes ESD stress, the typical ESD protection design for RF circuits is shown in Fig. 1, which had been successfully verified in a 900-MHz RF receiver with HBM ESD level of greater than 8kV [3]. The power-rail ESD clamp circuit was designed to help the ESD protection diodes for discharging ESD current in forward-biased condition during the four-modes ESD stresses. Diode operating in forward-biased condition can sustain much higher ESD level, so the ESD protection diode can be drawn with a very small device dimension to minimize the parasitic effect to RF circuits.

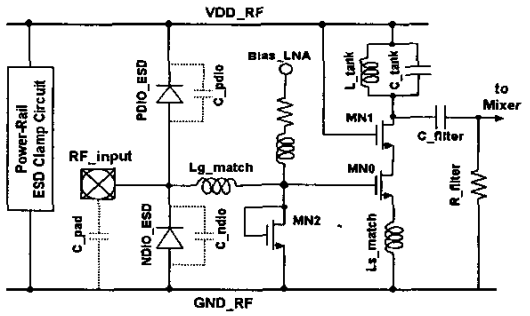

Fig. 1. The typical ESD protection design with double diodes and active power-rail ESD clamp circuit for LNA RF input pin.

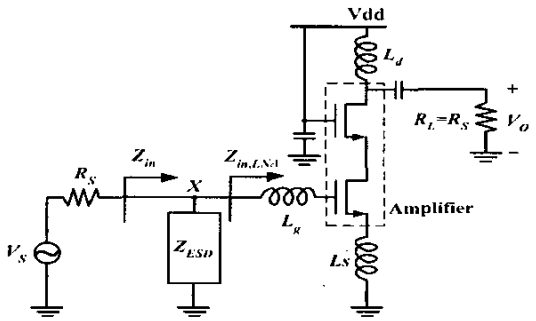

Fig. 2. The equivalent small-signal circuit of a RF LNA with on-chip ESD protection device for calculating the overall power gain and noise figure.

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However, when the operating frequency of RF circuits is further increased, such parasitic effect from the small-dimension ESD protection diodes can still degrade RF performance. To find the impact of such ESD protection diodes on the circuit performance of giga-Hz RF LNA, the noise figure and power gain of a RF LNA with on-chip ESD protection device has been calculated from its small-signal equivalent circuit, as that shown in Fig. 2.

A simple expression to the input impedance at resonance of the inductive degenerate LNA is [4]

$$Z_{in,LNA} = s(L_s + L_g) + \frac{1}{sC_{gs}} + (\frac{gm}{C_{gs}})L_s \approx \omega_T L_s = R_s \cdot \quad (1)$$

The overall input impedance of the RF LNA with ESD protection device (Z_{ESD}) is

$$Z_{in} = Z_{ESD} \| Z_{in,LNA} \approx Z_{ESD} \| R_s \cdot \quad (2)$$

So, overall transconductance (G_m) of this LNA stage is

$$G_m = \frac{Z_{ESD}}{Z_{ESD}+R_s}\frac{\omega_T}{s(R_s+Z_{in})} = \frac{\omega_T}{sR_s}\frac{Z_{ESD}}{R_s+2Z_{ESD}} = \frac{\omega_T}{sR_s}\frac{1}{2+\frac{R_s}{Z_{ESD}}} \cdot \quad (3)$$

To analyze the overall power gain of the LNA, we neglect the feedback capacitor C_{gd} of the MOS device first and assume that at input and output are conjugately matched to get a simpler expression of the power gain. The transducer power gain G_T (corresponding to S21) is

$$G_T = \frac{P_L}{P_{avs}} = \frac{\frac{1}{8}|V_s G_m|^2 (R_o \| R_s)}{\frac{1}{8}|V_s|^2 / R_s} = |G_m|^2 R_s (R_o \| R_s) = \left(\frac{\omega_T}{\omega_0}\right)^2 \frac{(R_o \| R_s)}{R_s} \left| \frac{1}{2+\frac{R_s}{Z_{ESD}}} \right|^2 \quad (4)$$

In (4), P_L is the power delivered to the load, P_{avs} is the power available from the source, and R_o is the output impedance of the amplifier.

As $Z_{ESD}=R_{ESD}+jX_{ESD}$, through some derivation, we can get the overall noise factor (NF) of the LNA with on-chip ESD protection device as

$$NF = 1 + \frac{S_{a,M_1}(\omega_0) + S_{a,Resd}(\omega_0)}{S_{a,src}(\omega_0)} = 1 + \gamma\chi' g_{d0} R_S \left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{R_S R_{ESD}}{4\left|R_{ESD} + jX_{ESD} + \frac{R_S}{2}\right|^2}, \quad (5)$$

where $$\chi' = 1 + 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1+Q_s'^2), \quad (6)$$

$$Q_s' = \left|\frac{\omega_0(L_s+L_g)}{(Z_{ESD}\|R_s)}\right| = \left|\frac{1}{\omega_0(Z_{ESD}\|R_s)C_{gs}}\right| = \frac{1}{\omega_0 C_{gs}}\left|\frac{1}{R_s}+\frac{1}{Z_{ESD}}\right|. \quad (7)$$

The g_{d0} is the zero-bias drain conductance of MOS device, γ is a bias-dependent factor, δ is the coefficient of gate noise, $\alpha = g_m/g_{d0}$, and c is the complex correlation coefficient between the gate noise and the drain noise.

From above equations, if the impedance of the ESD protection device (Z_{ESD}) can be approaching to infinite, the power gain (G_T) and noise figure (NF) of the RF LNA with ESD protection device can be converged to those of a pure RF LNA without ESD protection device. However, even though ESD protection diodes, operated in forward-biased condition to discharge ESD current with the help of power-rail ESD clamp circuit, still have to be drawn with somewhat device size for sustaining the desired ESD level. The parasitic capacitance and resistance from ESD protection diodes still generate Z_{ESD} into above equations. When the RF circuit is operating in a higher frequency (~10GHz), Z_{ESD} of ESD protection devices seen from the RF input port to ground will be reduced. So, the impedance Z_{ESD} was not approaching to infinite in actual RF LNA with any ESD protection circuit. This implies that the on-chip ESD protection circuit will seriously degrade circuit performance of RF LNA, especially in much higher frequency.

III. ESD Protection Design with LC-Tank

The RF power gain loss and noise figure contributed by ESD devices are strongly dependent on the parasitic capacitance and parasitic resistance of input port ESD devices. If the parasitic effect of input ESD devices can be blocked during the RF circuit operates, the RF power gain would not be degraded anymore. To provide nearly infinite impedance from the on-chip ESD protection devices, a novel ESD protection design with LC-tank to tune out the parasitic effects from the ESD devices for giga-Hz RF applications is shown in Fig. 3. The LC-tank is designed to resonant at the operation center frequency of RF circuits. So, the RF input port will see infinite impedance through ESD clamp devices with the LC-tank, which resonating at RF operation frequency. In order to stack the LC-tank and the N+ diode, the deep N-well is used to isolate the P substrate and the N+ diode. The inductance and capacitance in the LC-tank can be decided from the resonating frequency of

$$\omega_0 = \frac{1}{\sqrt{LC}} \cdot \quad (8)$$

With consideration on the parasitic effect of inductor and capacitor realized in real silicon chip, the values of inductance and capacitance of LC-tank under the same resonating frequency (demonstrated at 2.7 GHz in this work) are modified in a pair to investigate the overall circuit performance. The LC-tanks with the same resonating frequency at 2.7GHz, but realized by different inductance and capacitance are listed in Table I, which have been designed and fabricated in a 0.25-μm CMOS process with thick top-layer metal to realize inductors.

To avoid the ESD diodes operating in the breakdown condition during the PS-mode and ND-mode ESD stresses to cause a much lower ESD level, a turn on efficient RC-based ESD clamp circuit between the power-rails is constructed into the ESD protection circuit. When the RF pad was zapped in the PS-mode or ND-mode ESD stress [1], the Dp1 and Dn1 would operate under forward-biased condition, and through inductor and power-rail ESD clamp circuit to discharge ESD current. Because the ESD current is discharged through forward-biased Dp1 (Dn1), thick metal inductor, and the large-dimension MNESD between power rails under the PS-mode (ND-mode) ESD stress. The ESD level can still sustain high enough to protect the internal RF circuits.

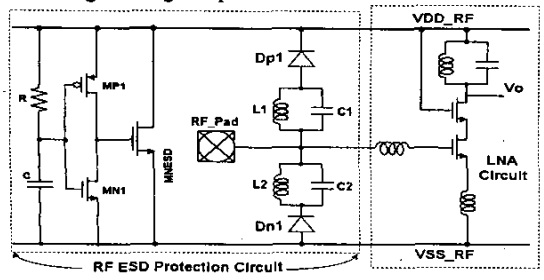

Fig. 3. The proposed RF ESD protection circuit with LC-tank.

TABLE I
DIMENSIONS OF INDUCTOR AND CAPACITOR IN LC TANK

fo=2.7GHz	1	2	3	4	5
Inductance (top thick metal)	12.12nH (6.5 Circles)	8.64nH (5.5 Circles)	5.88nH (4.5 Circles)	3.74nH (3.5 Circles)	2.17nH (2.5 Circles)
Capacitance (MIM)	219fF (14.8umx14.9um)	361fF (19umx19um)	596fF (24.4umx24.4um)	999fF (31.6umx31.6um)	1731fF (41.6umx41.6um)

IV. EXPERIMENTAL RESULTS

The proposed LC-tank ESD protection circuits with different combinations of L and C values have been designed and verified in a 0.25-μm CMOS process. The RF circuit performance of noise figure and power gain on the fabricated LC-tank ESD protection circuits have been investigated by two-port GSG measurement with the S-parameter measurement system HP 85122A. The experimental setup to measure power gain and noise figure is shown in Fig. 4. ESD robustness of the fabricated LC-tank ESD protection circuits has been verified by ESD Zapmaster in both human-body-model (HBM) and machine-model (MM) ESD stresses.

A. Power Gain

The power gain S21 vs. frequency of the LC-tank RF ESD protection circuit with different inductance is shown in Fig. 5 during the frequency range of 2.4 ~3 GHz: The line shown with L=0 nH (0 circle) means that the ESD protection diodes were not blocked with the LC-tank, which is the traditional ESD protection design of Fig. 1 for comparison reference. The diodes (Dn1 and Dp1) in Fig. 5 have a parasitic capacitance of 300 fF. In Fig. 5, the measured results show that the power gain loss become smaller when the inductance is larger. At 2.7 GHz, the RF power gain S21 is increased from −1.05 dB (without LC tank) to −0.6 dB (with LC tank, L=12.12 nH). When ESD diodes are drawn with larger device sizes, comparisons on the power gain loss (at 2.7 GHz) between the proposed RF ESD protection design (in Fig. 3 with LC tank) and the prior-art ESD protection design (in Fig. 1 without LC tank) are shown in Fig. 6. This has proven that the LC-tank technique can successfully block the most parasitic effect from ESD diodes to RF circuits, especially when the ESD diodes are drawn with larger device dimensions.

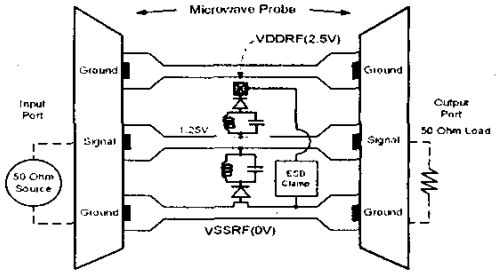

Fig. 4. The experimental setup to measure the power gain and noise figure of the fabricated RF ESD protection circuit with LC-tank.

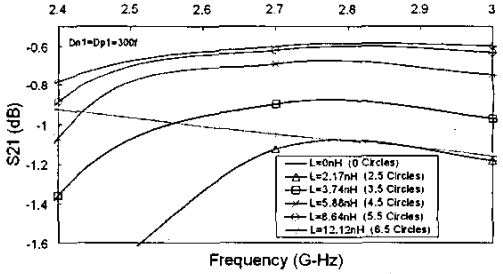

Fig. 5. The measured power gain loss of the proposed RF ESD protection circuit from 2.4 to 3 GHz under different inductances in the LC-tanks.

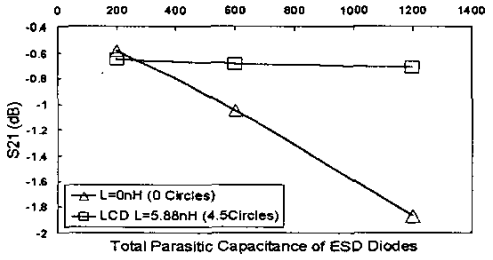

Fig. 6. Comparisons on the power gain loss between the proposed RF ESD protection design with LC tank and the prior-art design without LC tank at 2.7 GHz.

B. Noise Figure

The noise figures in the frequency range, between 2.4 GHz to 3 GHz, among the fabricated RF ESD protection circuits with different inductance in the LC-tank are compared in Fig. 7. The line shown with L=0 nH (0 circle) is the prior-art ESD protection design of Fig. 1 as a reference. The noise figure of the proposed RF ESD circuit with LC-tank is smaller than that of the traditional ESD protection circuits without LC-tank. All the ESD diodes (Dn1 and Dp1) are drawn with the same device size in the verified ESD protection circuits, which are all with a parasitic capacitance of 300 fF. At 2.7 GHz, the overall noise figure of the RF ESD protection circuit is decreased from 0.83 dB (without LC-tank) to 0.54 dB (with LC-tank, L=12.12 nH). The comparisons on the increase of noise figure (at 2.7 GHz) between the proposed RF ESD protection design with LC tank and the prior-art ESD design without LC tank are shown in Fig. 8, under different ESD diodes dimension. This has verified the effectiveness of LC-tank using in RF ESD protection circuit.

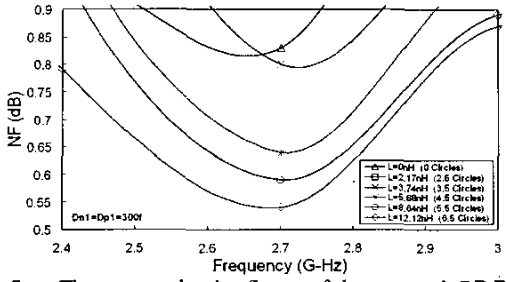

Fig. 7. The measured noise figure of the proposed RF ESD protection circuit from 2.4 to 3 GHz under different inductances in the LC-tanks.

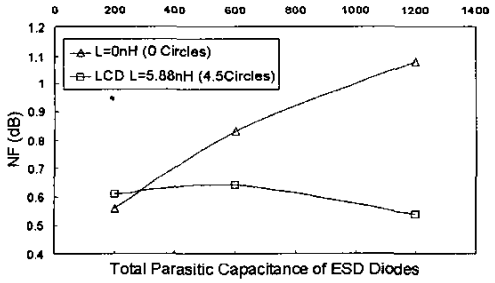

Fig. 8. Comparisons on the increase of noise figure between the proposed RF ESD protection design with LC tank and the prior-art design without LC tank at 2.7 GHz.

C. ESD Robustness

The four-modes HBM and MM ESD test results on the fabricated RF ESD protection circuits with LC-tanks under different inductor circles are summarized Table II. All the LC-tanks have the same resonating frequency at 2.7 GHz. The total parasitic capacitance (Cdiodes) generated from the ESD diodes (Dn1 and Dp1) is also varied as 600 fF, 200 fF, and 1200 fF, to verify the corresponding ESD robustness. From the measured results, the more inductor circles in RF ESD protection circuits lead to the lower HBM and MM ESD levels, under the same device size (600 fF) of ESD diodes. When the inductor in LC-tank is kept as 4.5 circles in layout, the HBM and MM ESD levels of the proposed RF ESD protection circuit can be increased by the increase of the device size of ESD diodes, which are indicated as the Cdiodes in Table II.

TABLE II
ESD LEVEL OF FABRICATED ESD PROTECTION CIRCUITS

LCD RF ESD Protection circuit			PD-mode		NS-mode		PS-mode		ND-mode	
Cdiodes	L	C	HBM(V)	MM(V)	HBM(V)	MM(V)	HBM(V)	MM(V)	HBM(V)	MM(V)
600fF	2.5 Circles	1731fF	5700	425	7100	775	3200	275	7200	400
600fF	3.5 Circles	996fF	4000	400	6800	700	2500	225	6000	350
600fF	4.5 Circles	596fF	3400	375	6600	650	2000	200	5200	275
600fF	5.5 Circles	361fF	3200	300	6400	650	1600	175	4600	225
600fF	6.5 Circles	219fF	2900	300	6000	625	1400	150	3900	200
200fF	4.5 Circles	596fF	3000	300	4300	500	1600	125	3000	200
1200fF	4.5 Circles	596fF	3800	325	8000	775	2700	200	6300	325

V. CONCLUSION

A novel on-chip ESD protection design with LC-tank to tune out the parasitic effects from the ESD devices for giga-Hz RF applications has been successfully verified in a 0.25-μm CMOS process. The LC-tank is designed to resonant at the operation center frequency of RF circuits, and to generate infinite impedance through ESD clamp devices with the LC-tank. To meet the requests of 2-kV HBM and 200-V MM ESD protection, ESD diodes (drawn with capacitance of Dn1=Dp1=300 fF) and LC-tank (L=5.88 nH drawn in 4.5 circles) in the proposed RF ESD protection circuit can be optimized to have a better RF performance of power gain loss of only –0.69 dB and noise figure increase of only 0.63 dB, under 2.7 GHz operating frequency.

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