

## 51.3: Successful Electrostatic Discharge Protection Design for LTPS Circuits Integrated on Panel

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### Abstract

A successful electrostatic discharge (ESD) protection design for 2.2-inch TFT-OLED product has been proposed and demonstrated in this paper. The panel-B with this successful ESD protection design has shown higher ESD robustness, as comparing to the panel-A with old-version ESD protection method. The VDD-to-VSS ESD clamp circuits have been inserted in I/O region of panel-B to effectively protect the internal circuits. Moreover, the turn-on behavior in time domain of VDD-to-VSS ESD clamp circuits has been verified to clamp the overstress ESD pulse. The I-V curve shifting and failure analysis with hot-spot pictures after ESD zapping are also shown in this paper.

### 1. Introduction

As the time of system-on-panel (SOP) is approaching, ESD reliability issue on the driver circuits or control circuits integrated with TFT-LCD or TFT-OLED panels is not only an oncoming problem but also an extremely worth-concern issue for production. Recently, some papers related to ESD robustness of LTPS TFTs have been reported [1]-[4]. Moreover, the transmission-line-pulsing (TLP) measured secondary breakdown current ( $I_{t2}$ ) of LTPS TFTs with gate-driven and substrate-triggered techniques has been investigated in [5]-[6]. Until now, none paper reported the ESD robustness of TFT product with circuit-on-panel. How to design the efficient ESD protection for circuit-on-panel has become an emergent challenge.

In this paper, the new panel-B with successful ESD protection design has been compared to the panel-A with old-version ESD protection method. The turn-on-efficient VDD-to-VSS ESD clamp circuit [7] of panel-B plays an important role to discharge ESD energy, and its turn-on behavior has been verified in time-domain measurement. According to the measurement results, the panel-B with successful ESD protection design has been proved to gain higher ESD robustness for high-yield mass production.

### 2. ESD Protection of 2.2-inch TFT-OLED Panel

#### 2.1 LTPS Process

TFT devices were fabricated on buffer oxide, which is above the glass substrate. After a  $\alpha$ -Si:H films deposited on buffer oxide by PECVD system, the XeCl excimer laser was used to crystallize  $\alpha$ -Si:H film, and then the poly-Si film was patterned. Subsequently, gate insulator was deposited by PECVD. After the source and drain regions impurities doping, the interlayer was deposited by

PECVD. Then, doping activation and hydrogenation were done to get better electrical characteristics. Finally, contact holes etching and source/drain metal patterning were formed.

#### 2.2 Protection Circuits of Panel-A and Panel-B

The 2.2-inch TFT-OLED panel-A with old-version ESD protection design is shown in Fig. 1. The ESD protection circuit in I/O circuit of panel-A is with Gate-VDD LTPS PMOS (GDPMOS) and Gate-Ground LTPS NMOS (GGNMOS) as ESD protection devices. The dimensions of GGNMOS and GDPMOS are drawn as  $800\text{ }\mu\text{m}/6\text{ }\mu\text{m}$  and  $1200\text{ }\mu\text{m}/6\text{ }\mu\text{m}$ , respectively. When the input pin of panel-A is under positive ESD zapping related to VSS (PS mode ESD zapping), the ESD current is discharged by only one path, as shown by dashed line in Fig. 1. The ESD energy will be released from input pin to VSS as soon as the drain junction breakdown of GGNMOS. By the breakdown mechanism to discharge ESD energy, both ESD robustness and turn-on speed of device are poor. It deserved to be mentioned that, no designed ESD discharge paths from VDD to VSS is highly dangerous to have ESD damages in the internal circuits.

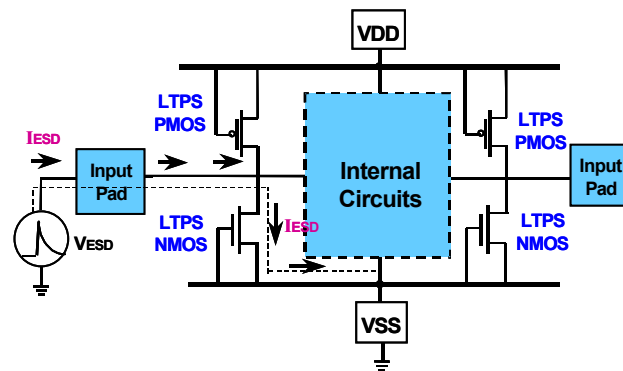


Figure 1 The ESD protection design for old-version panel-A in 2.2-inch TFT-OLED display.

In panel-B, not only GDPMOS ( $W/L = 1295\text{ }\mu\text{m}/4\text{ }\mu\text{m}$ ) and GGNMOS ( $W/L = 1246\text{ }\mu\text{m}/4\text{ }\mu\text{m}$ ) but also VDD-to-VSS ESD clamp circuits in I/O circuits constitute the whole-panel ESD protection scheme, as that shown in Fig. 2. With the VDD-to-VSS ESD clamp circuits, the panel-B has a designed ESD protection path from VDD to VSS to avoid ESD damages in internal circuits.

Moreover, this kind of ESD protection design creates more discharging paths to bypass ESD current. For example, when PS mode ESD occurs at input pin, the main ESD current will flow through forward-biased GDPMOS and discharge through the VDD-to-VSS ESD clamp circuits (bold dashed line). The other ESD current (thin dash line) will be discharged by breakdown of GGNMOS. The essence of the whole-panel ESD protection design provides more ESD discharging paths when ESD occurs.

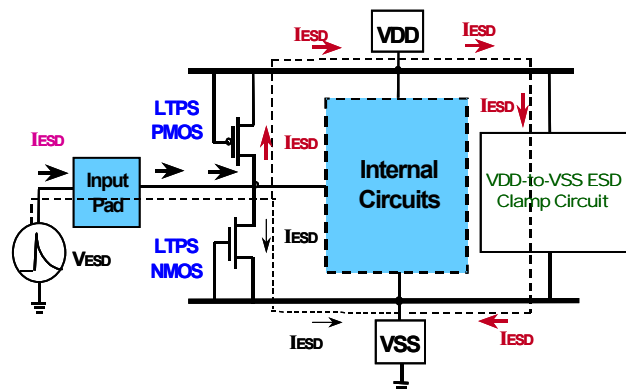


Figure 2 The ESD protection design for new panel-B with whole-panel ESD protection solution.

### 2.3. Concept of the Efficient VDD-to-VSS ESD Clamp Circuit

The VDD-to-VSS ESD clamp circuit consists of ESD detection circuit and ESD clamping device ( $M_{ESD}$ ), as that shown in Fig. 3. Before ESD zapping, the nodes  $V_X$  and  $V_G$  have the voltage levels the same as the VSS level initially because the IC is in the floating condition without power supplies. The ESD voltage across the VDD and VSS power line will charge the capacitor C to rise up the voltage level of  $V_X$ . The ESD voltage has a rise time about  $\sim 10$  ns. The voltage level of  $V_X$  is increased much slower than the voltage level on the VDD power line, because the RC circuit has a time constant in the order of microsecond ( $\mu$ s). Due to the delay of the voltage increase on the node  $V_X$ , the  $M_p$  device is biased by ESD voltage and conducts a voltage into the node  $V_G$  to turn on  $M_{ESD}$ . The turned-on  $M_{ESD}$ , which provides a low-impedance path between the VDD and VSS power lines, can clamp ESD voltage across the VDD and VSS power lines. So, the internal circuits can be effectively protected without ESD damage. When the panel is in the normal operating condition with the power supplies, the  $M_{ESD}$  device has to be kept off to avoid power loss from VDD to VSS.

### 2.4 Realization of the VDD-to-VSS ESD Clamp Circuit

The practical top-view layout of VDD-to-VSS ESD clamp circuit with specified components in TFT panel is shown in Fig. 4. The VDD-to-VSS ESD clamp circuit is designed to be turned on when ESD voltage appears across the VDD and VSS power lines. But, this ESD clamp circuit is kept off when the panel is under the normal power-on condition. To meet these requirements, the RC time constant in the VDD-to-VSS ESD clamp circuit is designed about  $0.1 \sim 1 \mu$ s to achieve the desired operations. Moreover, the VDD-to-VSS ESD clamp circuit is inserted around the whole-

panel layout, as that shown in Fig. 5. The distance between two VDD-to-VSS ESD clamp circuits is about  $5500 \sim 7000 \mu$ m due to the limitation of layout area for IO design.

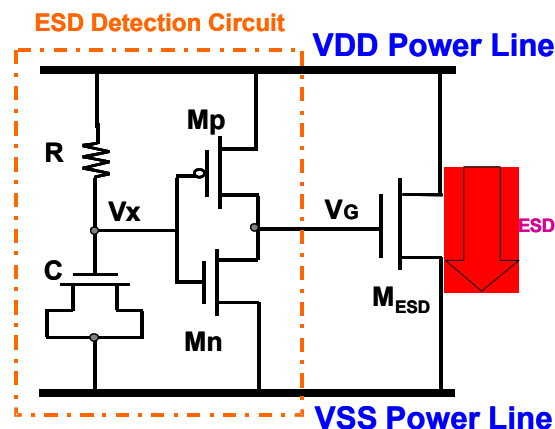


Figure 3 The circuit diagram of VDD-to-VSS ESD clamp circuit in panel-B.

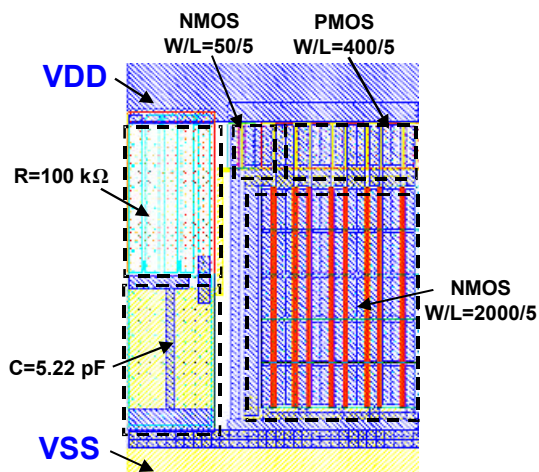


Figure 4 The layout view and specified device parameters of VDD-to-VSS ESD clamp circuit in panel-B.

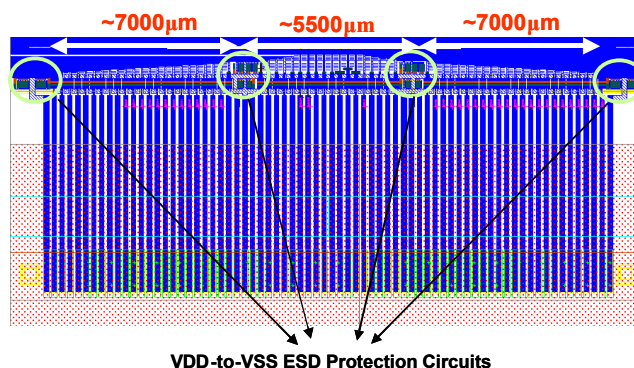


Figure 5 The location of VDD-to-VSS ESD clamp circuit in panel-B layout.

### 3. Experimental Results

#### 3.1 Turn-on Verification of VDD-to-VSS ESD Clamp Circuit

To verify the turn-on behavior of VDD-to-VSS ESD clamp circuit, an ESD-like voltage pulse generated by HP 8110 was applied between VDD and VSS. The 12V ESD-like pulse has a rise time of 10ns and a pulse width of 500ns. In panel-A, the output waveform is nearly the same as the input ESD-like pulse due to no extra ESD discharging path from VDD to VSS, as that shown in Fig. 6. For panel-B, as shown in Fig. 7, the pulse height has been clamped to 5.1V when the 12V ESD-like pulse is applied. This has verified that the VDD-to-VSS ESD clamp circuit in panel-B can effectively clamp the overstress ESD voltage under ESD stress condition, so it can provide more efficient ESD protection to the circuits on panel.

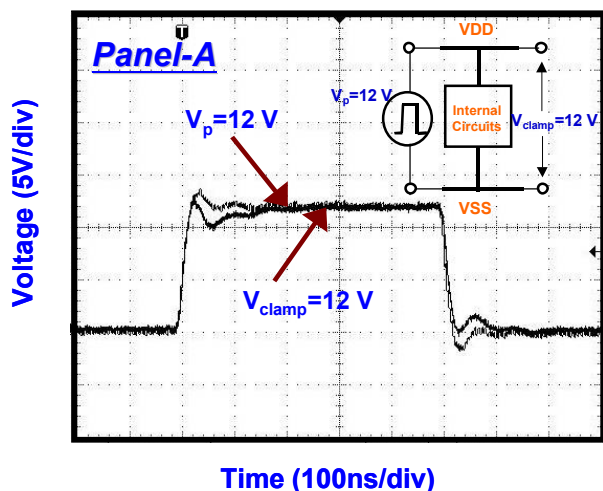


Figure 6 The turn-on verification from VDD to VSS in the panel-A under 12V ESD-like voltage pulse triggering.

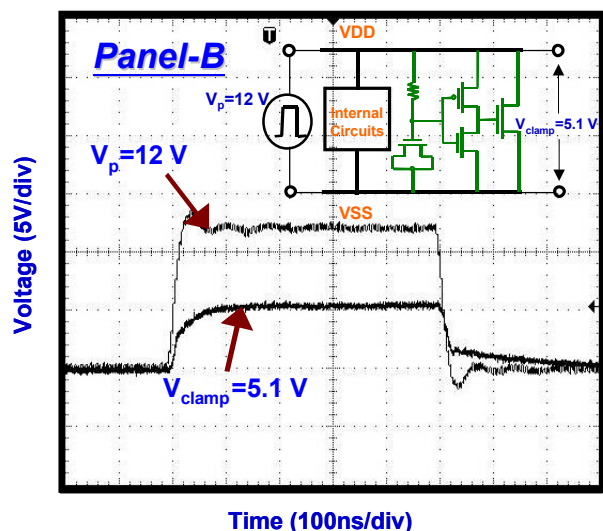


Figure 7 The turn-on verification of VDD-to-VSS ESD clamp circuit from VDD to VSS in the panel-B under 12V ESD-like voltage pulse triggering.

#### 3.2 Failure Behavior

The failure behavior of TFT devices is great different from that of CMOS device. When the device is damaged by ESD stress, it was burned out to short and then with an increase on leakage current. Due to the unstable grain boundary traps, the TFT device under ESD stress is not easy to define whether the device is damaged or not. Therefore, the definition of failure criteria in this work is: (1) the voltage shifts 30% under 40uA, or (2) the top view of device has obvious failure spots. In Fig. 8, the measured I-V curve shifting of input pin of panel-B is less than 30% after positive-to-VDD (PD) mode Machine Model (MM) ESD stress of 550V. But the obviously failure spots are located not only in GDPMOS device but also in GGNMOS device, as shown in Fig. 9. This is due to the ESD current has extra current path from GGNMOS to VDD-to-VSS ESD clamp circuit under PD mode ESD stress. So, even through the I-V curve shifts below 30%, the failure criteria 2 decided the failure of device. In Fig. 10, the I-V curve shifts above 30% after negative-to-VSS (NS) mode human body model (HBM) ESD stress of 2kV. But the top-view of TFT device has no failure spot, as shown in Fig.11. The failure is due to the latent damages of GGNMOS device under NS mode ESD zapping.

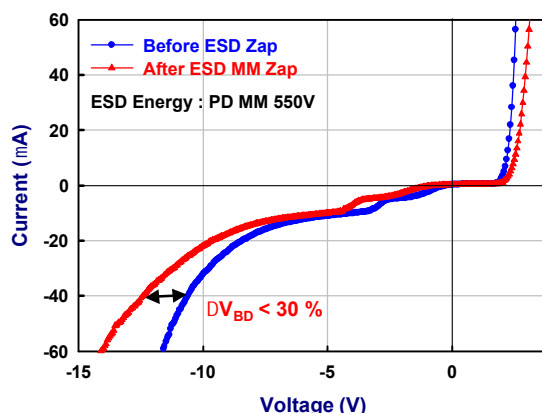


Figure 8 The I-V curve shift of p-channel TFT device before and after machine-model ESD stress of 550V.

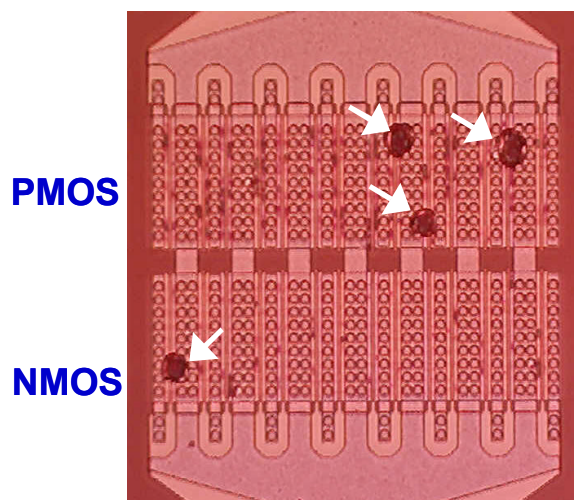


Figure 9 The failure spots on both p-channel and n-channel TFT devices after the machine-model ESD stress of 550V in PD mode zapping.



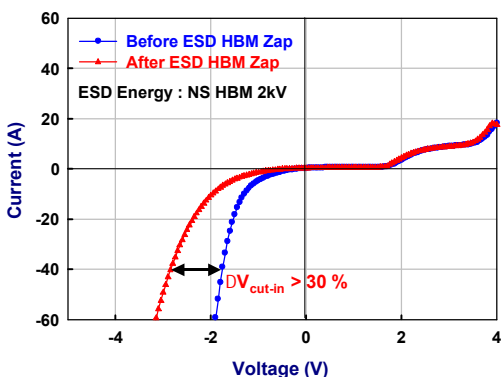


Figure 10 The I-V curve shift of n-channel TFT device before and after the HBM ESD stress of 2kV.

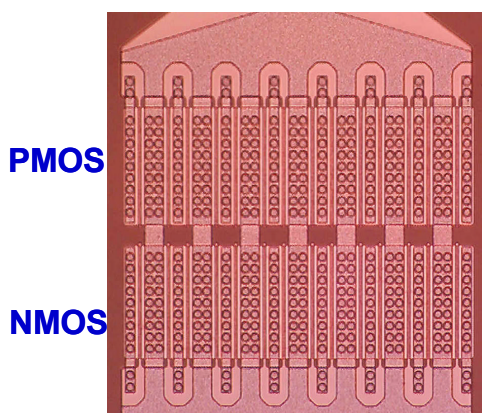


Figure 11 No failure spot on both p-channel and n-channel TFT devices after the HBM ESD stress of 2kV in NS mode zapping.

### 3.3 Comparison on ESD Robustness between Panel-B and Panel-A

Since the ESD stress may have positive or negative voltage on an input (or output) pin with the VDD or VSS pins respectively ground, there are four ESD-stress modes (PD, ND, PS, and NS modes) on an input (or output) pin [7], as shown in Fig. 12. By measurement with ESD tester, the HBM and MM results of panel-A and panel-B under four ESD-stress modes are listed in Table 1. The panel-B with VDD-to-VSS ESD clamp circuits is more robust than panel-A with the same I/O circuit. The HBM level of panel-B is 1.75kV, which is higher than that of panel-A, 1.25kV. The NS mode is worst among the four modes of ESD stress. It is due to large hot-carrier injection in GGNMOS device structure in the LTPS process. The ESD stress under PD and ND modes related to GDPMOS is more robust than that under PS and NS modes related to GGNMOS. That is a evidence that the ESD characteristic of GDPMOS is more reliable than that of GGNMOS. Not only the ESD characteristic but also the DC characteristic including variation of threshold voltage of NMOS TFT device is poor. Therefore, the ESD performance of GGNMOS could be improved on layout structure or on the circuit design scheme. The GDPMOS can be used to replace the GGNMOS as the ESD protection device between input pin and VSS power line for better ESD robustness of TFT panel.

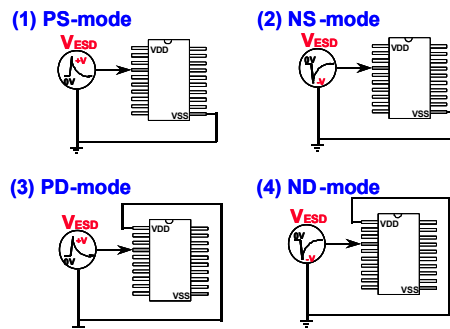


Figure 12 Four modes of ESD stress on an input (or output) pin with respect to the grounded VDD or VSS pins.

Table 1 Comparison of ESD robustness between panel-B and panel-A under various modes of ESD stress.

	PD	ND	PS	NS
HBM Panel-A	2.25kV	2.25kV	2.25kV	1.25kV
HBM Panel-B	3.25kV	2.75kV	3.0kV	1.75kV
MM Panel-A	425V	325V	225V	100V
MM Panel-B	525V	375V	275V	125V

## 4. Conclusion

Successful whole-panel ESD protection design for 2.2-inch TFT OLED display has been proposed in this paper. The architecture of panel-B with whole-panel ESD protection scheme, as comparing to that of panel-A, has shown obvious improvement on ESD protection. The VDD-to-VSS ESD clamp circuit in panel-B plays an important role to create more ESD current discharging paths. The ESD result of NS mode is the weakest among four modes ESD stress, which is due to latent damages in GGNMOS device. However, it can be further improved by layout structure of GGNMOS device, replaced by GDPMOS, or other circuit techniques.

## 5. References

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