ESD Protection Design for Mixed-Voltage-Tolerant I/O Buffers with Substrate-Triggered Technique

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ABSTRACT

A substrate-triggered technique is proposed to improve ESD protection efficiency of the stacked-NMOS device in the mixed-voltage I/O circuit. The substrate-triggered technique can further lower the trigger voltage of the stacked-NMOS device to ensure effective ESD protection for the mixed-voltage I/O circuit. The proposed ESD protection circuit with the substrate-triggered technique for 2.5V/3.3V tolerant mixed-voltage I/O circuit has been fabricated and verified in a 0.25-μm salicided CMOS process. Experimental results have confirmed that the HBM ESD robustness of the mixed-voltage I/O circuit can be increased ~60% by this substrate-triggered design.

I. INTRODUCTION

In the mixed-voltage IC with single power supply, only a low VDD power supply is provided for internal circuits. Therefore, the I/O circuits are designed to be tolerant of, and protected from, high-voltage input signals. Typically, a chip, which operates with I/O signals ranging from 0V to 3.3V, may have an internal supply voltage of only 2.5V or 1.8V. The chip-to-chip interface I/O circuits must be designed to avoid electrical overstress on the gate oxide and to prevent undesirable current leakage paths between the chips [1], [2]. The ESD protection circuit also has to meet these constraints for providing robust ESD protection in such mixed-voltage application. In advanced deep submicron CMOS technology, some fabrication processes provide both high-voltage and low-voltage transistors. In such processes, the high-voltage transistors which have thicker gate oxides can be used for the protection circuits. However, some processes with only single gate-oxide thickness do not have this capability. Thus, there is a need for an ESD protection circuit designed by only using the thin-oxide MOS devices, which have the same oxide thickness as those used in the interior of chip.

To solve the gate-oxide reliability issue without using the additional thick gate-oxide process (or called as dual gate oxide in some CMOS processes), the stacked-NMOS structure had been widely used in the mixed-voltage I/O buffer [2], [3]. The typical 3V/5V-tolerant mixed-voltage I/O circuit is shown in Fig. 1 [2]. The pull-up PMOS, connected from the I/O pad to VDD power line, has the gate tracking circuits for tracking the gate voltage and the N-well self-biased circuits for tracking N-well voltage, which are designed to ensure that the pull-up PMOS does not conduct current when the 5-V input signals enter the I/O pad. Due to the limitation of placing a diode from the pad to VDD, such mixed-voltage I/O circuits with stacked-NMOS often have much lower ESD level, as compared to the buffer with single NMOS [4].

An NMOS device with higher local substrate potential had been confirmed to provide better ESD robustness [5], [6]. In this paper, a new substrate-triggered design is proposed to reduce the trigger voltage of the lateral npn BJT in the stacked-NMOS device, and to enhance the ESD robustness of the mixed-voltage I/O circuits.

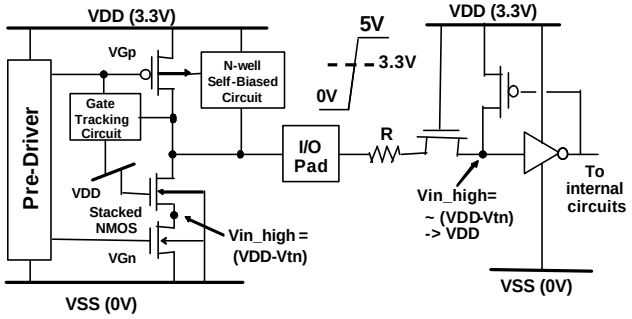

Fig. 1 The typical mixed-voltage I/O circuit with the stacked NMOS and the self-biased-well PMOS to avoid the leakage current path and the gate oxide reliability issue.

II. SUBSTRATE-TRIGGERED STACKED NMOS

A. Stacked-NMOS Device

Fig. 2(a) and (b) show the finger-type layout pattern and the corresponding cross-sectional view of the stacked-NMOS structure for mixed-voltage I/O circuit, which includes one pair of NMOS transistors connected in a stack configuration. The stacked-NMOS device is often used as both of the pull-down stage and the ESD protection device for the I/O circuit. This NMOS transistor pair includes a first transistor (top NMOS transistor), having a drain connected to an I/O pad, and a gate (Vg1) connected to the VDD power supply. A second NMOS transistor (bottom NMOS transistor) of the NMOS transistor pair is merged into the same active area of the first transistor, having a gate (Vg2) connected to the pre-driver of mixed-voltage I/O circuit. The drain of the bottom NMOS and the source of the top NMOS are constructed together by sharing the common N+ diffusion region.

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The voltage (Vg1) of the top NMOS is biased at the low VDD voltage (e.g. 2.5V in a 2.5V/3.3V interface). The voltage (Vg2) of the bottom NMOS is at VSS provided by the pre-driver to avoid leakage current through the stacked-NMOS structure, when the I/O circuit has a high-voltage input signal. With a high-voltage input signal at the pad (e.g. 3.3V in a 2.5V/3.3V interface), the shared common diffusion region has approximately a voltage level of VDD-Vth (~2.7V). The Vth (~0.6V) is the threshold voltage of NMOS device. Therefore, the stacked NMOS can be operated within the safe range for both dielectric and hot carrier reliability limitations.

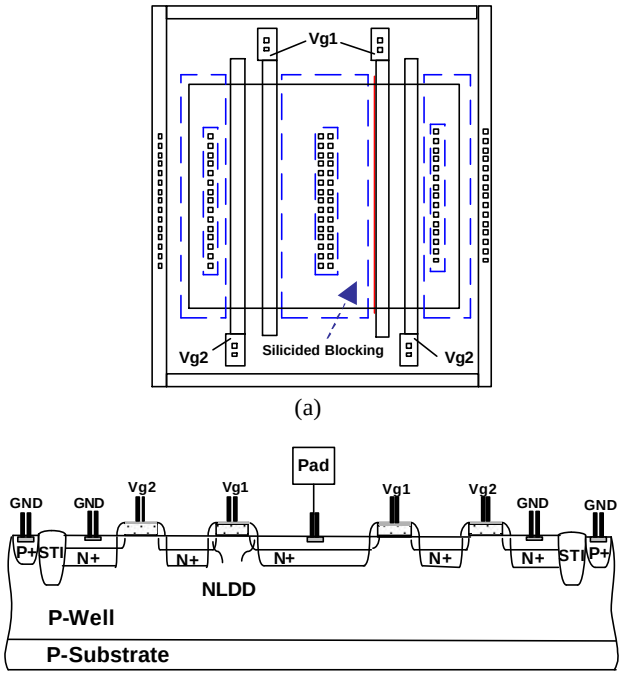

Fig. 2 (a) The finger-type layout pattern, and (b) the corresponding cross-sectional view, of the stacked-NMOS device in a P-substrate CMOS process.

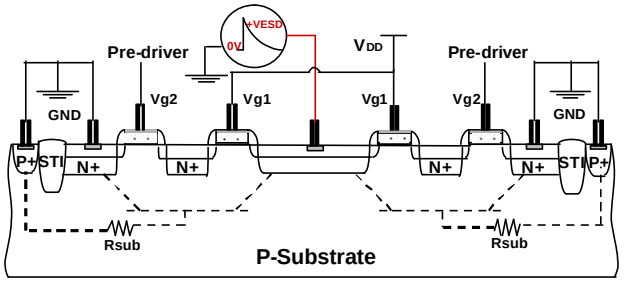

Fig. 3 The cross-sectional view of the stacked-NMOS device indicating the bipolar effect during the positive-to-VSS ESD-stress condition.

Under the positive-to-VSS ESD-stress condition (with VSS grounded but VDD floating), the stacked-NMOS device operates in snapback breakdown, with the bipolar effect taking place between the drain of the top NMOS and the source of the bottom NMOS. Fig. 3 shows a device cross-sectional view of a stacked-NMOS device indicating the bipolar effect during the positive-to-VSS ESD-stress condition. These two diffusions act as bipolar emitter and collector, respectively. Their spacing determines the base width and turn-on efficiency of the lateral bipolar transistor.

The snapback mechanism of stacked-NMOS device for conducting large amount of ESD current involves both avalanche breakdown and turn-on of the parasitic lateral npn bipolar transistor. The hole current (Isub) generated from drain avalanche breakdown, drifting through the effective substrate resistance (Rsub) to ground, may elevate the substrate potential locally to the emitter-base junction of npn shown in Fig. 3. The voltage level, which the local substrate potential is elevated, depends on the relative proximity to the avalanching junction. When the emitter-base junction of npn begins to weakly forward bias due to the increase of local substrate potential, additional electron current through the bipolar device acts as "seed current" to drive a significant increase in the multiplication rate and avalanche current generation at the collector-base junction of the lateral npn BJT. Therefore, a "snapback" is seen, and the lateral npn BJT enters strong bipolar conduction.

B. Substrate-Triggered Stacked-NMOS Device

As shown in Fig. 3, the snapback operation of stacked-NMOS device depends on the substrate current (Isub), which is created at the reversed-biased drain/p-substrate junction, to forward bias the substrate/source junction.

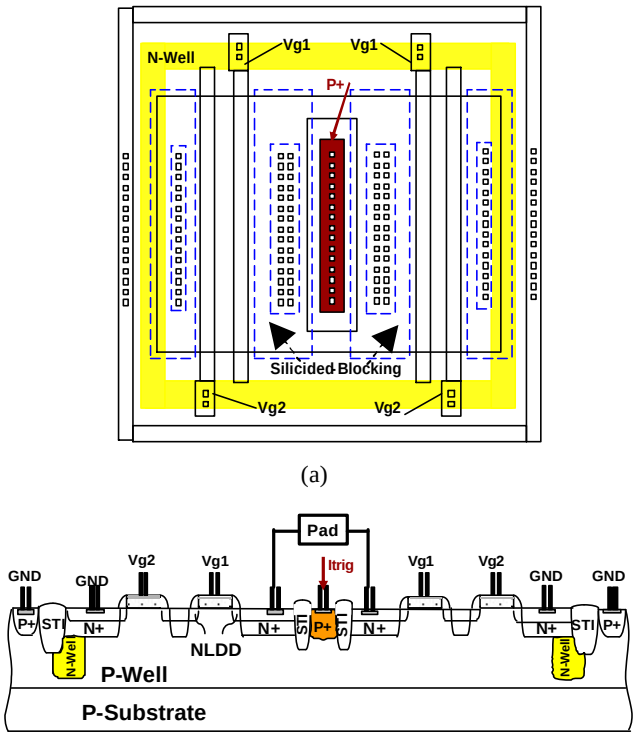

Fig. 4 (a) The finger-type layout pattern, and (b) the corresponding cross-sectional view, of the substrate-triggered stacked-NMOS device in a P-substrate CMOS process.

Hence, the substrate resistance (Rsub) and substrate current (Isub) are the important design parameters for ESD protection [7]. The substrate-triggered circuit technique can be used to generate the substrate current. With the substrate-triggered current, the trigger voltage (Vt1) of the stacked-NMOS device in mixed-voltage I/O circuits can be reduced for more effective ESD protection.

The substrate-triggered technique has an obvious improve on ESD level of the large-dimension NMOS devices [6]. In this work, the substrate-triggered stacked-NMOS device that combines the substrate-triggered technique into the stacked-NOMS device is proposed.

The finger-type layout pattern and the corresponding cross-sectional view of the new proposed substrate-triggered stacked-NMOS device are shown in Fig. 4(a) and (b), respectively. In Fig. 4(b), the P+ diffusion is inserted into the center region of the stacked-NMOS device as the substrate-triggered point. The trigger current (Itrig) is provided by the special ESD detection circuit. An N-well structure is further diffused under the source region of this device to form a higher equivalent substrate resistance to improve turn-on efficiency of the lateral npn BJT in the stacked-NMOS device.

III. ESD PROTECTION CIRCUIT DESIGN

The ESD protection design including the substrate-triggered stacked-NMOS device, the substrate-triggered circuit, and the corresponding cross-sectional view are shown in Figs. 5 and 6, respectively. The substrate-triggered circuit is composed of the PMOS (Mp1) and NMOS (Mn1), to provide the substrate current for triggering on the parasitic lateral npn bipolar junction transistor contained in the stacked-NMOS device while the ESD voltage is zapping on the I/O pad.

The drain of Mn1 and the capacitance C in the substrate-triggered circuit and the collector of the parasitic npn BJT in the stacked-NMOS device are connected to the I/O pad. The gates of PMOS (Mp1 and Mp2) are connected together to the VDD power line through a resistor, which is an N+ diffusion resistance with a parasitic N+/P-sub diode used as an antenna diode to solve the antenna effect during the fabrication process.

Fig. 6 shows the cross-sectional view of the stacked-NMOS device with substrate-triggered circuit for protecting the mixed-voltage I/O circuits. In the normal circuit operating condition, the substrate-triggered circuit should remain in a non-conductive state, so that it does not interfere with the voltage levels on I/O pad. For the 2.5V/3.3V mixed-voltage IC application, 3.3V tolerance was desired for normal circuit operation with a 2.5V VDD supply in the chip. The gates of Mp1 and Mp2 are biased with 2.5V VDD supply in the substrate triggered circuit, so these two PMOS are kept OFF during the normal circuit operating condition. So, the substrate triggered circuit is in the non-conductive state. No current is conducted into the base of the npn BJT in the stacked-NMOS device.

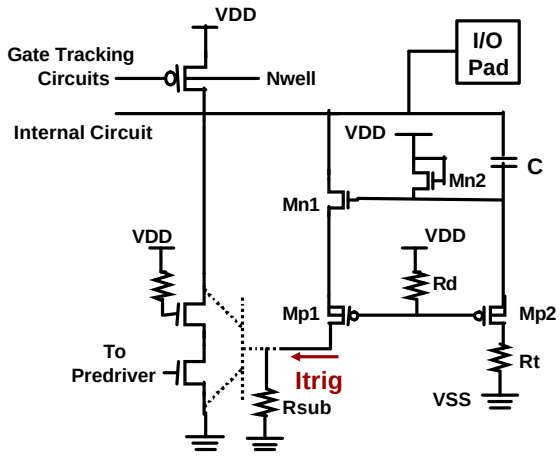

Fig. 5 The proposed on-chip ESD protection design for mixed-voltage I/O circuit with the substrate-triggered stacked-NMOS device.

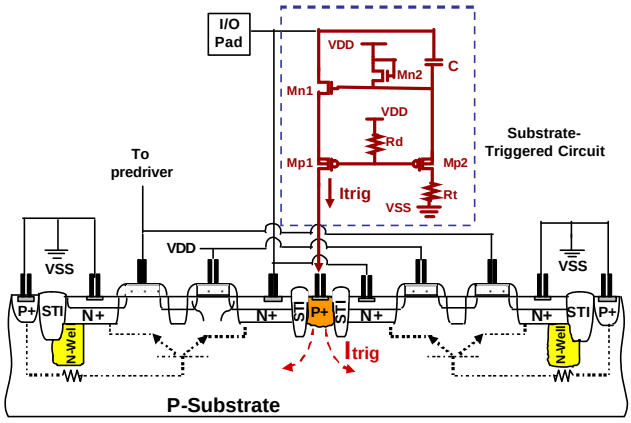

Fig. 6 The cross-sectional view of the stacked-NMOS device with the proposed substrate-triggered circuit.

Under the positive-to-VSS ESD-stress condition, the gates of PMOS (Mp1 and Mp2) have an initial voltage level of ~0V, while the VSS pin is grounded but the VDD pin is floating. Moreover, the ESD transient voltage on the pad is coupled through the capacitance C to bias the gate of Mn1. In this situation, both of the Mn1 and Mp1 are operated in the turn-on state. So, the substrate-triggered circuit will provide the trigger current flowing through the Mn1 and Mp1 path into the p-substrate. For a given Rsub, the substrate-triggered circuit must supply an enough trigger current (Itrig) to raise up the substrate potential, so that VBE (= Isub x Rsub) can become greater than 0.6V to trigger on the lateral npn BJT in the stacked-NMOS device. Once the parasitic lateral npn BJT is turned on, the ESD current is mainly discharged from the I/O pad through the npn BJT to the grounded VSS. The trigger current (Itrig) provided by the substrate-triggered circuit is determined by the size of Mn1, Mp1, and the capacitance C. With an appropriate Itrig, the substrate potential is raised up high enough to trigger on the lateral npn BJT and to reduce the trigger voltage of the ESD clamp circuit. Therefore, ESD robustness of the mixed-voltage I/O circuits with the stacked-NMOS devices can be effectively improved.

IV. EXPERIMENTAL RESULTS

The stacked NMOS and substrate-triggered design for mixed-voltage I/O circuit have been fabricated in a 0.25-μm CMOS process with silicided-blocking mask. The I-V characteristics of the stacked-NMOS devices with different substrate-triggered currents are measured by the curve tracer (*Tek370A*). The ESD simulator (*ZapMaster*) is used to evaluate the ESD robustness of the devices with the failure criterion of 1-μA current leakage under a 3.3-V bias.

A. Characteristics of the Substrate-Triggered Stacked-NMOS Device

The measured I-V characteristics of the stacked-NMOS device under different substrate-triggered currents are shown in Fig. 7. The trigger voltage of the stacked-NMOS device decreases when the substrate-triggered current increases. The trigger voltage reduces to only ~3.1V, when the Itrig is 7mA. Based on above experimental results, the effective ESD protection can be achieved by the special substrate-triggered circuit to generate the substrate current to further increase ESD robustness of the stacked-NMOS device in the mixed-voltage I/O buffer.

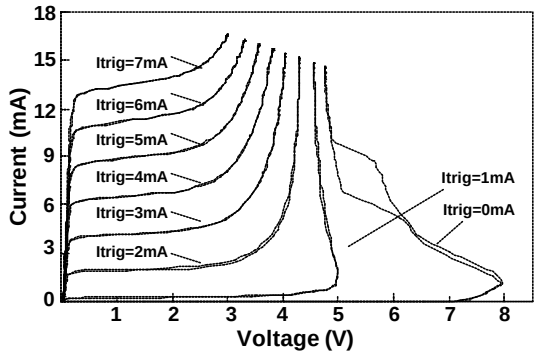

Fig. 7 The measured I-V characteristics of the stacked-NMOS device under different substrate-triggered currents.

B. ESD Robustness

The original mixed-voltage I/O buffers with different stacked-NMOS channel widths are also fabricated in the same test chip and tested as a reference. All stacked-NMOS devices with different channel widths have the same channel length of 0.5μm for both top and bottom NMOS, and the N+ diffusion layout spacing between the two poly gates in the stacked-NMOS device is fixed as 0.4μm. The HBM ESD levels of the mixed-voltage I/O circuits with or without the proposed substrate-triggered ESD protection design are compared in Fig. 8. For the stacked-NMOS with a channel width of 240μm, it can sustain the HBM ESD level of 3500V. But, if such a stacked-NMOS is designed with the proposed substrate-triggered circuit, its ESD level can be increased up to 5500V. It has a ~60% improvement from its origin value by this substrate-triggered design. This has verified the effectiveness of the proposed substrate-triggered design to improve ESD level of mixed-voltage I/O circuits.

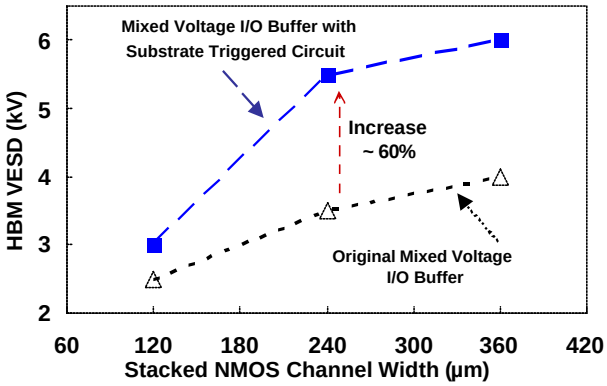

Fig. 8 The positive-to-VSS HBM ESD levels of the mixed-voltage I/O buffers with or without the substrate-triggered circuit in a 0.25-μm CMOS process.

V. CONCLUSION

To improve ESD robustness of the stacked-NMOS devices in mixed-voltage I/O circuits, a new ESD protection circuit has been designed and successfully verified in a 0.25-μm CMOS process. The HBM ESD level of the mixed-voltage I/O circuit with a stacked-NMOS device of 240-μm channel width can be improved from the original 3.5 kV up to 5.5 kV (increase of ~60%) by the proposed substrate-triggered design. Without using the thick gate oxide, this new proposed ESD protection circuit is fully process compatible with general sub-quarter-micron CMOS processes for effectively protecting the mixed-voltage interface circuits on the input and output pins. This design can be also applied to the I/O interfaces of 1.8V/3.3V, 1.8V/2.5V, or between other different voltage levels.

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