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Dynamic Holding Voltage SCR (DHVSCR) Device for ESD Protection with high Latch-up Immunity

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1. Introduction

On-chip ESD protection is a necessary for the advanced deep submicron integrated circuits (ICs). SCR device is an attractive choice, since it offers the maximum ESD performance, while occupying the smallest layout area. But SCR device is susceptible to latch-up during normal operations due to noise such as a power surge or spike. This phenomenon will lead to IC working failure or even destruction. Two methods had been reported to solve this problem [1]. One way is to increase the SCR's holding voltage to be larger than the supply voltage, and the other way is to increase the SCR's trigger current. Besides, the High-Holding Current SCR (HHI-SCR) device had been also reported [2], which employed an SCR with an increased holding current above certain minimum latch-up triggered current to prevent latch-up during normal operation. In this work, a Dynamic Holding Voltage SCR device (DHVSCR) is proposed to fine-tune a high holding voltage and holding current to prevent latch-up during normal operation condition. Under ESD stress condition, the DHVSCR will drop its holding voltage and holding current to discharge ESD current.

2. Device Structure

Figures 1 and 2 show the cross-sectional views for devices with the traditional PMOS-LVTSCR and the new proposed DHVSCR, respectively. Compared with the PMOS-LVTSCR, an NMOS transistor (NM2) is embedded in the DHVSCR structure. The PMOS-LVTSCR and DHVSCR devices are fabricated in a 0.25-μm/2.5V silicided CMOS process. The extra resistor between terminal R and GND is used to investigate the holding voltage and holding current of the new proposed DHVSCR device. The NM2 and PM2 embedded in the DHVSCR are used to adjust its holding voltage and holding current for effective ESD protection purpose during the ESD zapping condition, as well as, for high latch-up immunity under normal circuit operating condition.

3. Experiment and Results

The I-V curves of PMOS-LVTSCR under normal operation and ESD protection conditions are shown in Figs. 3(a) and 3(b), respectively. The holding voltage (V_h) of PMOS- LVTSCR device always keeps on 1.3V. In other words, the IC will be damaged or functional fail when SCR turn on during normal circuit operating condition. The I-V curves of DHVSCR under normal circuit operating and ESD protection conditions are showed in Figs. 4(a) and 4(b), respectively. Both gate voltages of the PMOS (PM2) and the NMOS (NM2) are tied to 2.5V or 0V, with the R terminal floating, to represent device operated under normal or ESD protection condition. In Fig. 4(a), DHVSCR's holding voltage (V_h) is about 2.8V, which is higher than V_{dd} supply voltage of 2.5V. In addition, its holding current (I_h) also rises up to 172mA. Thus, DHVSCR will not keep in the latch-up state, and high latch-up immunity for normal circuit operating can be achieved. In Fig. 4(b), DHVSCR's holding voltage (V_h) reduces to 2.2V and holding current (I_h) also drops to 91mA, when the gate of PM2 and NM2 is grounded. So, holding voltage and current can be adjusted by controlling gate voltage of PM2 and NM2. Such gate bias can be achieved by suitable ESD-detection circuit design.

Table I shows the holding voltage and the holding current of DHVSCR with different device widths. The holding voltage of these devices can be adjusted between 2.1V and 2.8V by the gate voltage of PMOS (PM2) and embedded NMOS (NM2). In addition, the holding currents of these devices can also be adjusted by the gate voltage of PMOS (PM2) and embedded NMOS (NM2). The ESD levels of DHVSCR and PMOS-LVTSCR are compared in Table II. The HBM and MM ESD level of the DHVSCR device are 5.6kV and 200V, which are slightly less than those of PMOS-LVTSCR. But, it is still high enough for ESD protection with a device width of only 50μm.

To investigate the holding voltage and holding current of DHVSCR during normal circuit operation with different shunt resistance, the embedded NMOS (NM2) is turned off and a variable resistor will be coupled between the R and GND terminals, whereas the gate voltage of PMOS (PM2) will be 2.5V. The measurement results are shown in Figs. 5 and 6. In Fig. 5, the DHVSCR's holding voltage will be increased higher than V_{dd} supply voltage when the shunt resistance is less than 100ohm. In Fig. 6, the holding current of DVHSCR will also be raised when the shunt resistance is tuned to low. This investigation on the shunt resistance has verified the effectiveness of the NM2 in DHVSCR structure, which is used to increase the holding voltage and current of the DHVSCR to avoid latch-up issue in the normal circuit operating condition.

4. Conclusions

The DHVSCR has tunable holding voltage and holding current. Its holding voltage can be increased above 2.5V supply voltage, and holding current will be raised to avoid latch-up during normal circuit operation. Under ESD protection condition, its holding voltage and current can be reduced to perform better ESD robustness. Besides, it can provide efficient ESD robustness with a small layout area.

References

[1] M.-D. Ker and H.-H. Chang, in *Proc. of EOS/ESD Symp.*, 1998, pp. 72-85.

[2] M. Markus *et al.*, in *Proc. of EOS/ESD Symp.*, 2002, pp. 10-17.

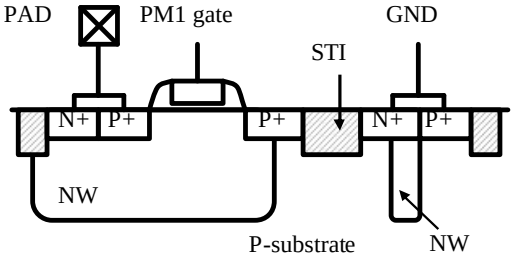


Fig. 1 The cross-sectional view of traditional PMOS-LVTSCR.

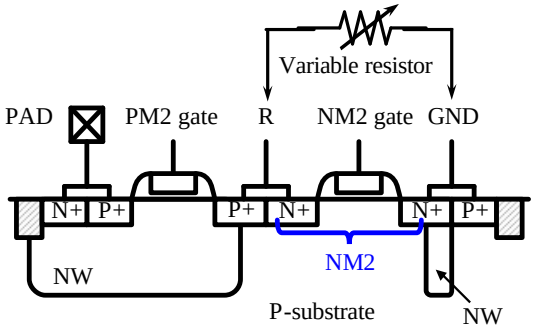
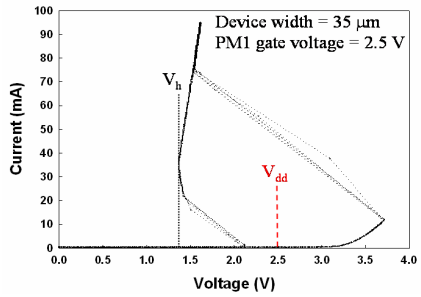
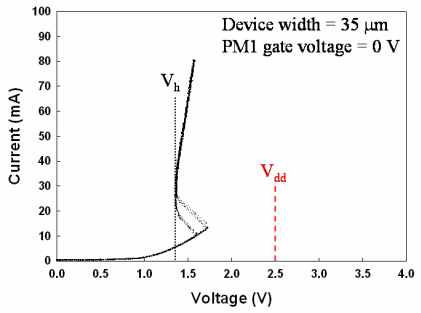


Fig. 2 The cross-sectional view of the new proposed DHVSCR.



(a)

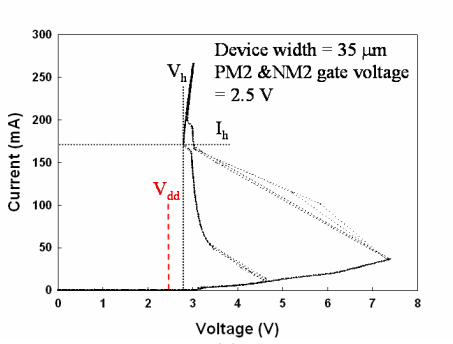


(b)

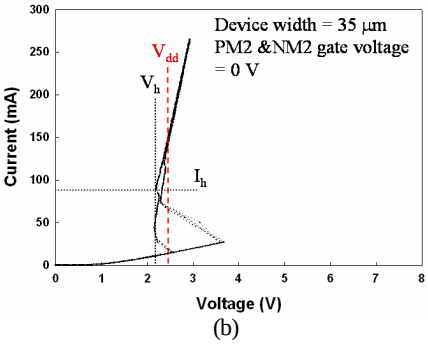
Fig. 3 The I-V curves of PMOS-LVTSCR under (a) normal circuit operating condition, and (b) ESD protection condition.

Table I
The holding voltage/holding current with different width of DHVSCR devices.

Device width	NM2 and PM2 gate voltage = 0 V	NM2 and PM2 gate voltage = 2.5 V
35 μm	2.21 V / 91.0 mA	2.80 V / 172.0 mA
50 μm	2.10 V / 127.0 mA	2.71 V / 227.0 mA



(a)



(b)

Fig. 4 The I-V curves of DHVSCR under (a) normal circuit operating condition, and (b) ESD protection condition.

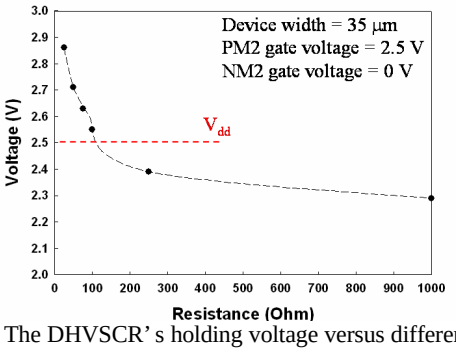


Fig. 5 The DHVSCR's holding voltage versus different shunt resistance during normal circuit operation condition.

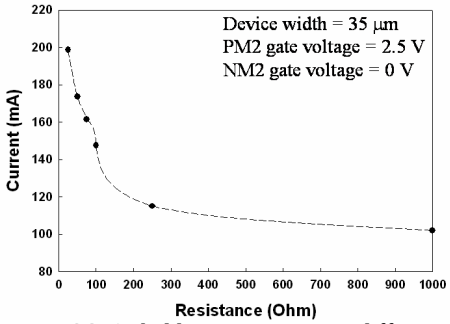


Fig. 6 The DHVSCR's holding current versus different shunt resistance during normal circuit operating condition.

Table II
HBM/MM ESD level of the DHVSCR and the PMOS-LVTSCR.

ESD model	DHVSCR	PMOS-LVTSCR
HBM	5.6 kV	6.2 kV
MM	200 V	250 V

*Device width is 50 μm.