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Improvement on Turn-on Speed of Substrate-Triggered SCR Device by Using Dummy-Gate Structure for On-Chip ESD Protection

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1. Introduction

An excellent ESD protection device must have high enough ESD robustness and faster turn-on speed to effectively protect the gate oxide of input stage from ESD overstress. With the best area efficiency, SCR can sustain highest ESD level in a smallest layout area, as comparing to other ESD protection devices. So, SCR had been used as on-chip ESD protection for a long time [1]. But, SCR still has a higher switching voltage (~20V) in CMOS technology, which is generally greater than the gate-oxide breakdown voltage of the input stage. Some reports had presented the solutions to overcome this issue [2], including the ST_SCR device [3].

In this work, a novel dummy-gate structure is used to block the shallow trench isolation (STI) region in SCR device and to further enhance its turn-on speed. With suitable ESD-detection circuit [3], the ST_SCR with dummy-gate structure is designed to be kept off during the normal circuit operating conditions, and to be quickly triggered on during the ESD-zapping conditions. Therefore, the ultra-thin gate oxide in deep submicron CMOS processes can be effectively protected by the ST_SCR with dummy-gate structure.

2. SCR Device With Dummy-Gate Structure

In deep submicron CMOS processes, the diffusion regions are isolated by STI. With the dummy-gate structures, the STI regions between the diffusions in SCR device are blocked. The ST_SCR device with STI is shown in Fig. 1(a), whereas the proposed ST_SCR device with dummy-gate structure is shown in Fig. 1(b). In a typical 0.25-µm CMOS process, the depth of STI is about ~0.4µm, but the junction depth of P+ / N+ diffusion is only about ~0.18µm. The deeper STI region in SCR device causes a longer current path from the anode to the cathode, which also leads to a slower turn-on speed. The ESD current path in the ST_SCR with dummy-gate structure indicated by the dashed line in Fig. 1(b) is shorter than that in ST_SCR with STI in Fig. 1(a), because the dummy-gate structure is used to block the STI region in SCR device. The inserted P+ diffusions are connected out as the p-trigger node of the ST_SCR. When a trigger current is applied into the trigger node, the ST_SCR can be triggered on into its latching state. For ESD protection purpose, the corresponding ESD-detection circuit has to be designed to control the turn-on of this ST_SCR.

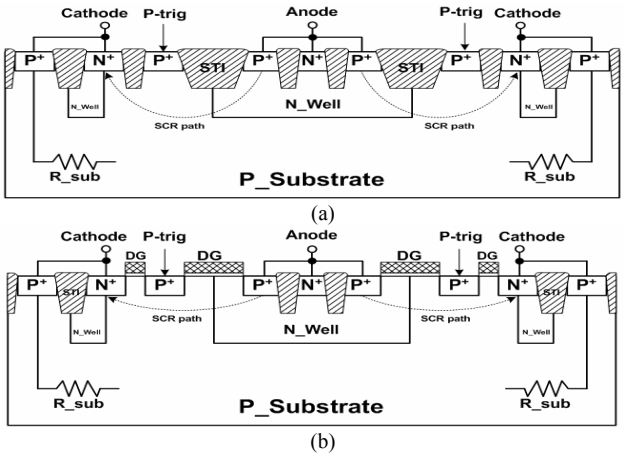

Fig. 1 Device structures of the substrate-triggered SCR (ST_SCR) with (a) STI structure and (b) dummy-gate structure.

3. Experimental Results

Device Characteristics

The two ST_SCR devices with STI and dummy-gate structures have been fabricated with the same layout area in a fully-silicided 0.25-µm CMOS process. The dependences of switching voltages (Vt1) of ST_SCRs with STI and dummy-gate structures on the substrate-triggered current are compared in Fig. 2 and the inset of Fig. 2 is the DC I-V curves of ST_SCR with dummy-gate structure under different substrate-triggered currents. When the substrate-triggered current at the p-trigger node is increased from 0mA to 6mA, the Vt1 of ST_SCR with STI is reduced from ~22V to ~7V, whereas the Vt1 of ST_SCR with dummy-gate structure is reduced from ~18V to ~3V. If the trigger current is continually increased, the Vt1 of both ST_SCRs will be nearly reduced to their holding voltages (~1.3V). This result has proven that the Vt1 of both ST_SCRs with STI and dummy-gate structure can be significantly reduced by the substrate-triggered technique. Moreover, the Vt1 of ST_SCR with dummy-gate structure can be further reduced lower than that of ST_SCR with STI under the same trigger current. This is related to the current gain (β) of parasitic bipolar transistor in SCR structure,

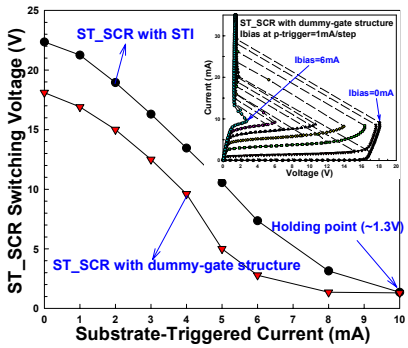

Fig. 2 The dependences of switching voltages of ST_SCR devices with STI and dummy-gate structure on the substrate-triggered current. The inset is the DC I-V curves of ST_SCR with dummy-gate structure under different substrate-triggered currents.

which will be discussed later. The SCR device with lower Vt1 can clamp ESD overstress more quickly to effectively protect the thinner gate oxide of input circuits.

Turn-on Speed

The turn-on time of ST_SCR is defined as the time for ST_SCR entering into its latching state. The measured turn-on times for ST_SCRs with STI and dummy-gate structure are shown in Figs. 3(a) and 3(b), respectively. The inset of Fig. 3(a) is the measurement setup. From Fig. 3(a), the turn-on time of ST_SCR with STI is reduced from 35ns, 20ns, to 11.2ns, while the ST_SCR is triggering by the voltage pulse of 1.5V, 2V, and 4V with 10-ns rise time into the trigger node. Moreover, from Fig. 3(b), the turn-on time of ST_SCR with dummy-gate structure is further reduced from 25.4ns, 13.6ns, to 9.8ns under the same measurement conditions as that of Fig. 3(a). The relations between the turn-on time and the triggering pulse voltage of ST_SCRs with STI and dummy-gate structure are compared in Fig. 4. The turn-on time of ST_SCR with dummy-gate structure can be effectively shortened, as comparing to the ST_SCR with STI. For CMOS IC applications with ultra-thin gate oxide, the ST_SCR with dummy-gate structure can be designed to protect the core circuits from latent damages or

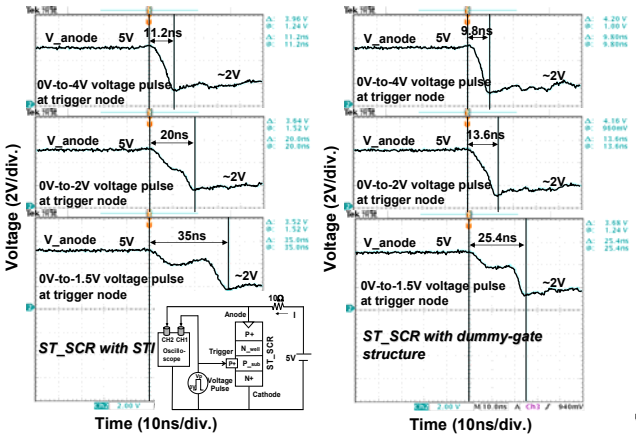

Fig. 3 Measurement on the turn-on time of ST_SCR under different voltage pulses. The measured voltage waveforms on the anode of the ST_SCR with (a) STI, and (b) dummy-gate structure, while the ST_SCR is triggering by the voltage pulse of 1.5V, 2V, and 4V with 10-ns rise time into the trigger node. The inset in (a) is the measurement setup.

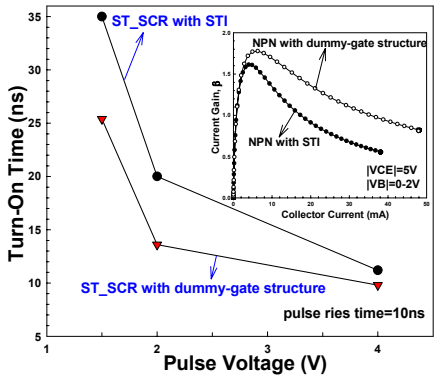

Fig. 4 The relations between the turn-on time and the triggering pulse voltage of ST_SCR with STI and dummy-gate structure. The inset is the dependence of current gains of the NPN bipolar transistors in the ST_SCR devices on its collector current.

failure more efficiently than the ST_SCR with STI. For analyzing the different characteristics of ST_SCRs, the dependence of current gains of NPN bipolar transistors in the ST_SCR with STI and dummy-gate structure on the collector current under the measured conditions of |VCE|=5V and |VB|=0-2V is shown in the inset of Fig. 4. In the inset of Fig. 4, the current gain of NPN in the ST_SCR with dummy-gate structure is higher than that of NPN in the ST_SCR with STI. The Vt1 of ST_SCR device is in inverse proportion to the current gain [4], so the ST_SCR with dummy-gate structure has the lower Vt1. In addition, substrate bias used to trigger the NPN transistor in the ST_SCR device has significant effect to further reduce Vt1 and turn-on time of ST_SCR with dummy-gate structure.

The dependence of turn-on time of ST_SCR with dummy-gate structure on rise time of voltage pulse under different substrate bias conditions is also measured and shown in Fig. 5. When a 4-V substrate pulse with rise time of 5ns is applied to the p-trigger node, the turn-on time of the ST_SCR can be shortened to 6.6ns. So, the turn-on speed of ST_SCR with dummy-gate structure can trace the rise time of ESD events to discharge the ESD current faster.

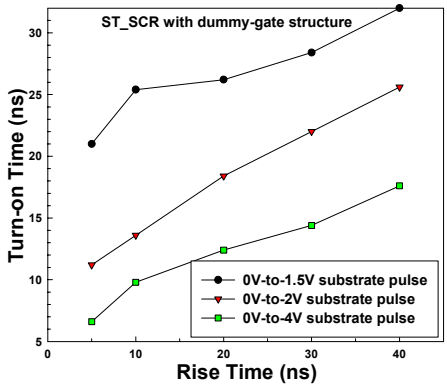

Fig. 5 The dependence of turn-on time of ST_SCR with dummy-gate structure on rise time of voltage pulse under different substrate bias conditions.

4. Conclusions

The novel dummy-gate structure in SCR device with substrate-triggered design has been successfully investigated in a 0.25-μm salicided CMOS process. The dummy-gate structure can indeed reduce the switching voltage and improve turn-on speed of ST_SCR device without increasing any cost, as comparing to the traditional SCR structure. With an improved turn-on speed, the proposed ST_SCR with dummy-gate structure can effectively protect the ultra-thin gate oxide against ESD damage in deep submicron CMOS integrated circuits.

References

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