Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 404-405

P1-3

Low-Voltage-Triggered PNP for ESD Protection in Mixed-Voltage I/O interface

Ming-Dou Ker, Wei-Jen Chang, and Wen-Yu Lo*

Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Taiwan.
*Mixed-Signal Product Division, Silicon Intergrated Systems (SiS) Corp., Hsinchu, Taiwan.

1. Introduction

With the mix of power supply voltages, chip-to-chip interface I/O circuits must be designed to avoid electrical overstress across the gate oxide, to avoid hot-carrier degradation on the output devices, and to prevent undesirable leakage current paths between the chips [1], [2].

Some mixed-voltage circuit applications, such as ADSL, which have input signals with voltage levels higher than VDD and lower than VSS, is shown in Fig. 1. The traditional ESD protection circuits shown in Fig. 2 are not suitable for these mixed-voltage interfaces. From Fig. 2(a), under the normal condition, the D_p diode will be forward biased when input signals are higher than VDD. The D_n diode will be forward biased when input signals are lower than VSS. The ESD protection circuit will cause the leakage current paths. For Fig. 2(b), it has the same leakage issue as that in Fig. 2(a). Moreover, in Fig. 2(b), it will even result in the gate-oxide reliability problem.

In this paper, a new ESD protection design with a new device, which is the low-voltage-triggered PNP (called as LVTPNP), is used for input signals with voltage level larger than VDD or less than VSS. The LVTPNP with a low breakdown voltage provides a current path between the emitter and collector when the PN or NP junction avalanche breakdown happens, therefore, it can effectively protect the internal circuits of such mixed-voltage I/O interface.

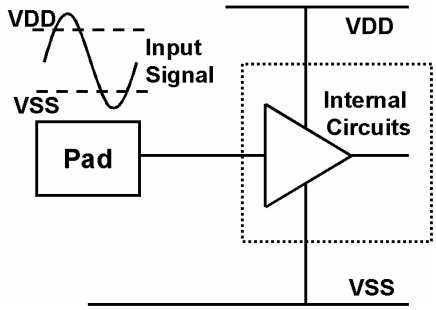

Fig. 1. The input signals with voltage levels higher than VDD and lower than VSS in some mixed-voltage I/O interface.

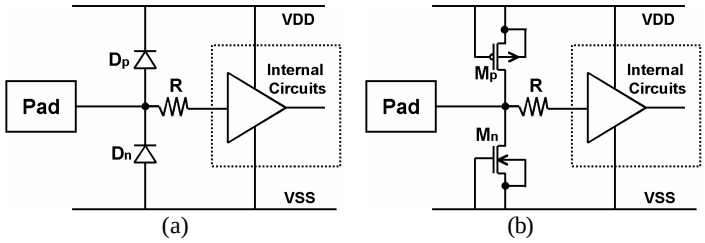

Fig. 2. The two traditional ESD protection circuits for input signals.

2. New ESD Protection Design with LVTPNP Devices

A new ESD protection design with LVTPNP device is shown in Fig. 3. The LVTPNP device is connected between input pad and VSS power line, which provides ESD protection for such mixed-voltage I/O interface.

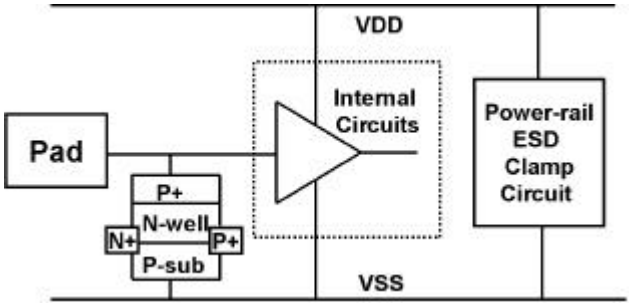

Fig. 3. A new ESD protection design with LVTPNP device.

LVTPNP Device Structure

The diagram of the traditional PNP is shown in Fig. 4(a). In Fig. 4(b), an n+ diffusion is inserted between the N-well and P-substrate, and the structure is similar to the traditional PNP but with a low breakdown voltage and a floating bulk, which is called as the type1 LVTPNP. The n+ diffusion, rather than being used as contact regions, is floated to avoid the leakage current paths from pad to VSS in such mixed-voltage I/O interface. That is to say, the base of the type1 LVTPNP is floating. Thus, only the PN or NP junction may be forward biased to eliminate leakage current in normal operation condition. Moreover, the junction between p+ diffusion and N-well has a low breakdown voltage since the p+ diffusion region is heavily doped, while the junction between N-well and P-substrate has high breakdown voltage since both of them are lightly doped. The junction between N-well and P-substrate with high breakdown voltage is disadvantageous to formation of the ESD current path. Fortunately, the n-type heavily doped regions compensate this disadvantage. The junction between n+ diffusion and P-substrate has a low breakdown voltage due to the heavily doped regions, which avalanches earlier than the junction between N-well and P-substrate when the ESD pulse is zapping the pad. Accordingly, the n-type heavily doped regions may be disposed in any location adjacent to the N-well and not limited to the location.

In Fig. 4(c), a p+ diffusion instead of n+ diffusion is inserted to become the type2 LVTPNP, and therefore the junction between p+ diffusion and N-well has a low breakdown voltage since the regions adjacent to the N-well and P-substrate are heavily doped.

Because of the floating base, the two separate p+ diffusion can be merged into one p+ diffusion to form the type3 LVTPNP, shown in Fig. 4(d). The p-type heavily

doped regions adjacent to the N-well and P-substrate are used as contact regions for P-substrate since regions only couple the P-substrate to another element or to receive a voltage level but keep N-well floated.

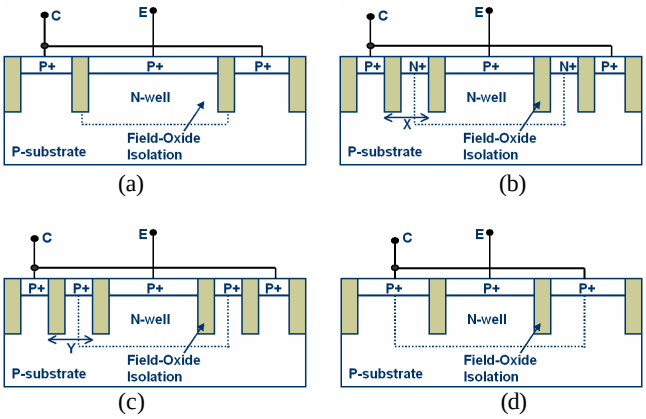

Fig. 4. The device structures of (a) the traditional PNP, and (b) the type1 LVTPNP, and (c) the type2 LVTPNP, and (d) the type3 LVTPNP.

3. Experimental Results

Device I-V Characteristics

The LVTPNP devices have been fabricated in 0.35-μm CMOS process. The measured I-V curves of the traditional PNP and LVTPNP are shown in Fig. 3. Comparing the traditional PNP with LVTPNP, the breakdown voltage is about 30V for the typical PNP, but that of LVTPNP is reduced to 8~10V.

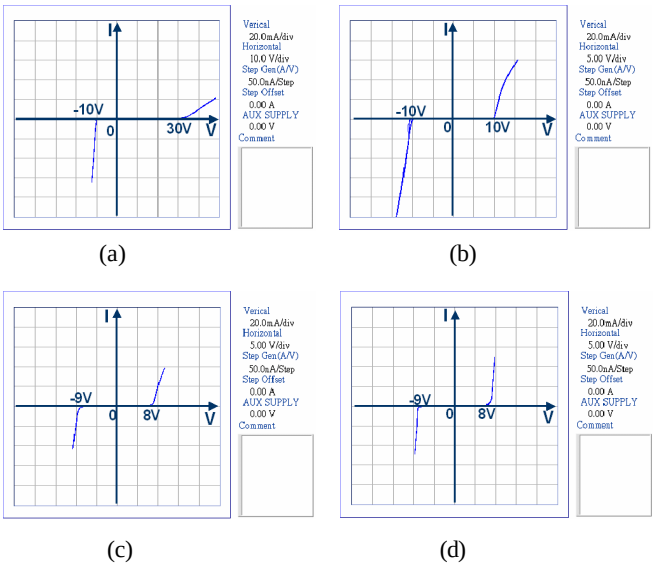

Fig. 5. The breakdown voltages of (a) the traditional PNP, and (b) the type1 LVTPNP, and (c) the type2 LVTPNP, and (d) the type3 LVTPNP.

ESD Level of LVTPNP

Here, we define the width of the ESD current path in the devices from the emitter to the collector. Under the positive-to-VSS ESD-stress condition, with the same size of 30μm×30μm (the width is defined as 30μm), the measured ESD levels of the traditional PNP and LVTPNP are shown in Fig. 6(a). The type1 LVTPNP with lower breakdown voltage has higher ESD level (~250V) than that of the lower breakdown voltage PNP (~150V). Usually, the doping concentration of N-well is heavier than P-substrate, so the junction between p+ diffusion and N-well of the type2 LVTPNP has slightly lower breakdown voltage (~8V) than the junction between n+ diffusion and P-substrate of the type1 LVTPNP (~10V). According to such results, the type2 LVTPNP has higher ESD level (about 400V) than that of the type1 LVTPNP. For the type2 LVTPNP and the type3 LVTPNP, both of them have the same breakdown voltage. However, from the structure, the ESD current path of the type2 LVTPNP is longer than that of the type3 LVTPNP. From the I-V curves, the turn-on resistance of the type2 LVTPNP is larger than that of the type3 LVTPNP. The power dissipation is I^2R, so the type3 LVTPNP has larger ESD level (about 550V) than that of the type2 LVTPNP due to higher power dissipation.

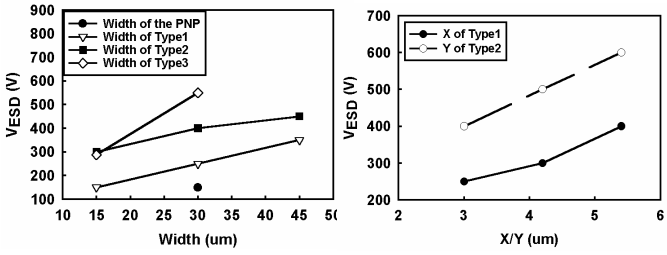

Fig. 6. (a) The ESD level v.s. device width, and (b) the ESD level v.s. the spacing X of the type1 LVTPNP in Fig. 4(b) or the spacing Y of type2 LVTPNP in Fig. 4(c), respectively.

From Fig. 6(a), as the width of the devices increase, the ESD level is improved. We can use multi-fingers of LVTPNP to increase the total current path from emitter to collector to improve ESD level to the desired ESD specification. From Fig. 6(b), as the spacing X of the type1 LVTPNP or the spacing Y of the type2 LVTPNP increase, the ESD level is also improved. From such results, we can increase these two spacings in LVTPNP to improve ESD robustness for such mixed-voltage I/O interfaces.

4. Conclusions

The LVTPNP devices have successfully lowered the breakdown voltage to have a good ESD protection to mixed-voltage I/O interface in 0.35-μm CMOS process. The LVTPNP devices indeed have the higher ESD level than that of the traditional PNP device. Among these three types of LVTPNP, the type3 LVTPNP with lowest trigger-on voltage and highest ESD robustness will be the best choice to be the ESD protection device for such mixed-voltage I/O interface.

References

[1] S. H. Voldman, "ESD protection in a mixed voltage interface and multi-rail disconnected power grid environment in 0.5- and 0.25-μm channel length CMOS technologies," in *Proc. of EOS/ESD Symp.*, 1994, pp. 125-134.

[2] S. Dabral and T. J. Maloney, *Basic ESD and I/O Design*, John Wiley & Sons, Inc., New York, 1998.