Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 426-427

P2-8

Novel ESD Protection Design for Nanoscale CMOS Integrated Circuits

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1. Introduction

Electrostatic discharge (ESD) damage has become the main reliability issue for IC products fabricated in nanoscale CMOS processes. The traditional ESD protection devices are initially kept off in CMOS ICs, they often have a relatively higher breakdown (or trigger-on) voltage and a slower turn-on speed. To effectively protect the thinner gate oxide in deep-submicron CMOS processes, the gate-coupled [1]-[2] or the substrate-triggered [3]-[4] circuit techniques had been used to reduce the turn-on voltage and to enhance the turn-on speed of traditional ESD protection devices. However, in nanoscale CMOS processes, the thin gate oxide (10~15Å) will be much weak under ESD stress. Still now, there is no effective solution to solve this serious reliability problem. It has become a big challenge to effectively protect such much thinner gate oxide in the future nanoscale CMOS ICs.

In this paper, a novel ESD protection design, that can successfully solve this problem, is first reported in the literature.

2. Already Turned-On Device

The already-on NMOS with a Vth of ~0V or even negative have been realized by the native device structure in the present 130-nm CMOS process without any extra process modification. The already-on NMOS for ESD protection design is built neither in the P-well nor in the N-well, but it is directly in the p-substrate, as those shown in Fig. 1. Such device is fully process-compatible to general sub-0.1μm CMOS processes.

The Ids-Vgs characteristics of the fabricated already-on (native) device and the normal NMOS under Vds of 0.1V is measured and shown in Fig. 2. With a much lower threshold voltage, such already-on (native) devices in on-chip ESD protection circuits can be quickly turned on to discharge ESD current without involving any junction breakdown.

The snapback I-V characteristics of already-on (native) device and normal NMOS under different channel lengths are measured by TLP (Transmission Line Pulsing) system and shown in Fig. 3. The dependences of trigger-on voltage (V_{trig}) and snapback holding voltage (V_{hold}) of already-on (native) device and normal NMOS on channel length are compared in Fig. 4. The already-on (native) device has no snapback characteristic because it conducts ESD current by punchthrough mechanism, not by parasitic lateral BJT. The dependences of It2 (second breakdown current) of the already-on (native) device and normal NMOS on different channel lengths are compared in Fig. 5. With a shorter channel length, the already-on (native) device has higher ESD robustness.

3. ESD Protection Design

With superiority of the lower threshold voltage and high ESD robustness, the already-on (native) device can be used stand-alone as the ESD clamp device in Fig. 6(a), or as the control device to quickly trigger on other ESD clamp devices in Fig. 6(b). The TLP-measured I-V curves of the combined ESD clamp cell and stand-alone FOD device are compared in Fig. 7. The V_{trig} of the combined ESD clamp cell is smaller than that of the stand-alone FOD.

The whole-chip ESD protection design with the ESD clamp cells of already-on devices is shown in Fig. 8. The gates of already-on devices in all ESD clamp cells are biased by a negative bias line in normal operating condition. The desired negative voltage to turn off the native device can be obtained from on-chip negative charge pumping circuit [5], which was a well-known circuit by IC designer.

4. Conclusions

A novel ESD protection design by using the already-on device is proposed to effectively protect CMOS ICs in nanoscale CMOS processes against ESD stress. Such an already-on device is designed to have a threshold voltage of ~0V, or even negative, which has been successfully verified in a 130-nm CMOS technology. When the IC is under the ESD zapping conditions, such already-on device are initially standing in the turn-on state and ready to discharge ESD current. So, such already-on device has the fastest turn-on speed and the lowest turn-on voltage to effectively protect the internal circuits with a much thinner gate oxide in nanoscale CMOS technology. Under the normal circuit operations, such already-on device is kept off by an on-chip-generated negative bias.

References

[1] C. Duvvury *et al*., in *Proc. of IRPS*, 1992, pp.141-150.
[2] M.-D. Ker *et a*l., *IEEE Trans. on VLSI Systems*, vol. 4, no. 3, pp. 307-321, 1996.
[3] C. Duvvury *et al*., in *Proc. of EOS/ESD Symp*., 2000, pp. 7-17.
[4] M.-D. Ker *et al*., in *Proc. of IEEE Int. Symp. on Circuits and Systems*, 2001, pp.754-757.
[5] M.-D. Ker, C.-Y. Chang, and H.-C. Jiang, "Design of negative charge pump circuit with polysilicon diodes in a 0.25-μm CMOS process," in *Proc. of IEEE AP-ASIC Conference*, 2002, pp. 145-148.

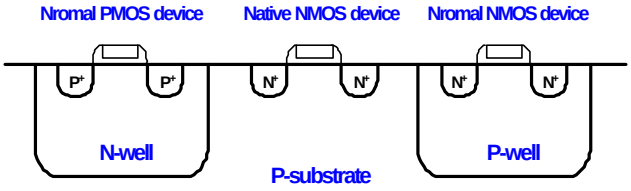

Fig. 1 The device cross-sectional views of the normal NMOS, normal PMOS, and the proposed already-turned-on (native) device in a p-substrate twin-well 130-nm CMOS technology.

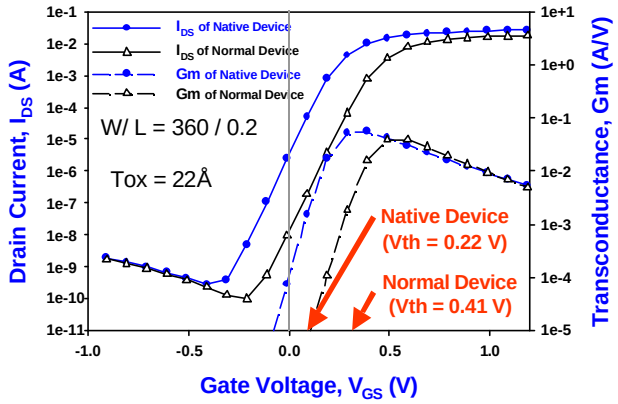

Fig. 2 The measured DC I-V curves and Gm curves of the fabricated already-on (native) device and the normal NMOS. The threshold voltage (Vth) is extracted by the maximum Gm method.

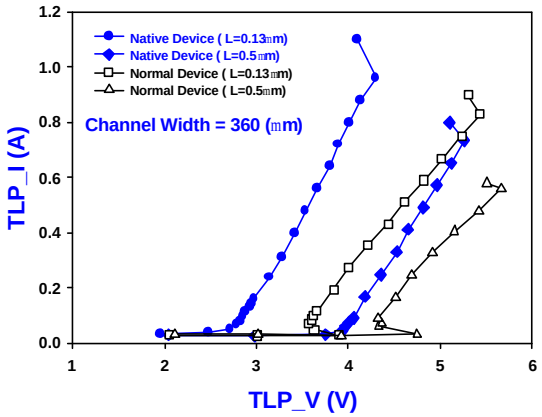

Fig. 3 The TLP-measured I-V curves of the already-on (native) device and the normal device under different channel lengths.

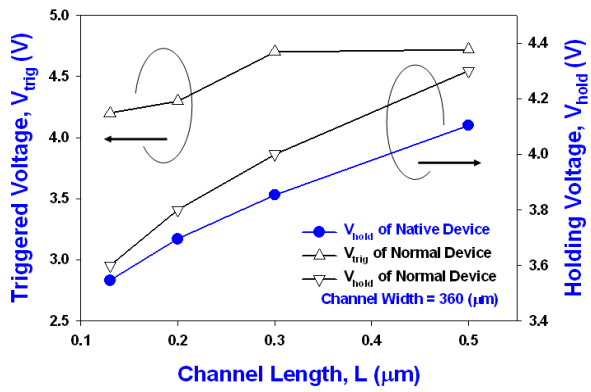

Fig. 4 The dependences of the trigger-on voltage (V_{trig}) and the snapback holding voltage (V_{hold}) of the already-on (native) device and the normal NMOS on the channel length.

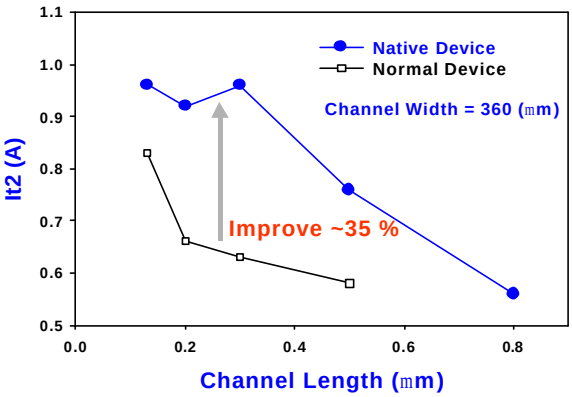

Fig. 5 The dependences of the It2 of the already-on (native) device and the normal NMOS on different channel lengths.

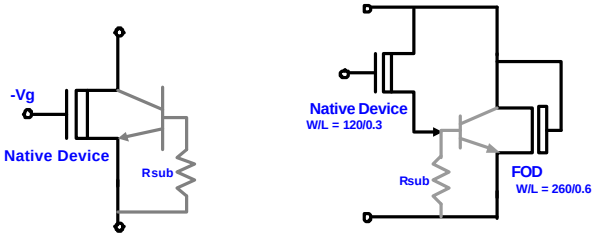

Fig. 6 The ESD clamp cells realized by (a) the already-on (native) device, and (b) a field-oxide device controlled by the already-on (native) device.

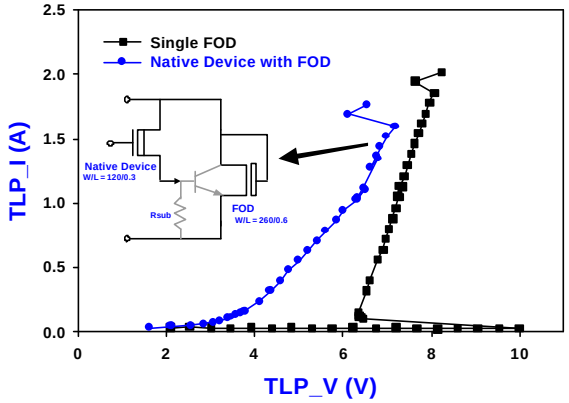

Fig. 7 The TLP-measured I-V curves of the combined ESD clamp cell and a stand-alone FOD device.

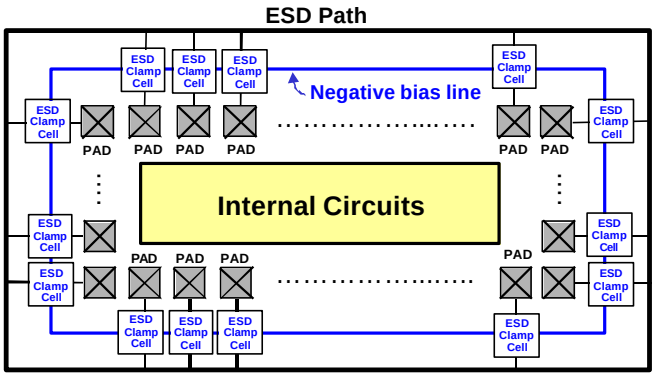

Fig. 8 The whole-chip ESD protection design with the ESD clamp cells of already-on (native) devices connected between every pad and the common ESD path in CMOS IC.