MOS-Bounded Diodes for On-Chip ESD Protection in a 0.15-μm Shallow-Trench-Isolation Salicided CMOS Process

Ming-Dou Ker, Kun-Hsien Lin, and Che-Hao Chuang*

Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics
National Chiao-Tung University, Taiwan

* ESD Protection Technology Department
SoC Technology Center
Industrial Technology Research Institute, Taiwan

ABSTRACT

Novel diode structures without the shallow trench isolation (STI) across the p/n junction for ESD protection in a 0.15-μm CMOS process are proposed. A NMOS (PMOS) is especially inserted into the diode structure to form the NMOS-bounded (PMOS-bounded) diode, which is used to block the STI isolation across the p/n junction in the diode structure. Without the STI boundary across the p/n junction of diode structure, the proposed PMOS-bounded and NMOS-bounded diodes can provide more effective protection to the internal circuits, as compared to the other diode structures under reverse-biased condition. Such PMOS-bounded and NMOS-bounded diodes are fully process-compatible to general CMOS processes without additional process modification or mask layers.

I. INTRODUCTION

With the scaled-down device dimension, shallower junction depth, thinner gate oxide, LDD (Lightly-Doped Drain) structure, and salicided process in sub-quarter-micron CMOS technology, the CMOS integrated circuits become more susceptible to electrostatic discharge (ESD) damage [1]-[2]. Therefore, on-chip ESD protection devices have to be added into the IC products to sustain a reasonable ESD stress (typically, ±2kV in the human-body-model ESD event [3]) for safe mass production. The typical ESD protection circuit with double diodes for a pad is shown in Fig. 1 [4], where the ESD clamp circuit between the VDD and VSS power rails are often added into the chip to avoid the ESD damages located in the internal circuit [5].

When the diodes stressed by the ESD pulses, the diffusion boundary to the STI is easily damaged by ESD and causes a very low ESD robustness [6]. The weakest point at the boundary between the STI field-oxide region and the diffusion edge of the diode structure is illustrated in Fig. 2, where the STI field-oxide region near to the P+ diffusion has a pull-down structure. When the p/n junction is reverse biased during ESD stress, the breakdown point is located at the boundary between the P+ diffusion and STI region. Due to the limit area of the boundary for heat dissipation, this pull-down structure on the STI boundary causes the P+ diffusion having a lower ESD robustness on its diffusion edge. If the CMOS process has the silicided diffusion, the silicide layer covered on the P+ diffusion causes a bend-down corner at the boundary between the P+ diffusion and STI region. This bend-down corner further causes the diode being more easily damaged by ESD. Thus, the ESD protection circuits formed by double diodes often have lower ESD robustness in the CMOS process with STI and silicided diffusion, even if the diodes have been drawn with larger silicon area. To overcome the ESD damage at the p-n junction diffusion to the STI boundary, the Poly/STI-bounded diode and Poly/Poly-bounded diode were reported [6].

* *This work was supported by the National Science Council, Taiwan; and partially supported by United Microelectronics Corporation (UMC), Hsinchu, Taiwan, on test chips fabrication.*

In this paper, the novel diode structures, called as NOMS-bounded diode and PMOS-bounded diode, are proposed to improve ESD robustness of CMOS IC's in sub-quarter-micron CMOS processes. ESD robustness and turn-on verification of the new proposed diode structures are investigated and compared to those of the normal diode, Poly/STI-bounded diode, and Poly/Poly-bounded diode in a 0.15-μm CMOS salicided process.

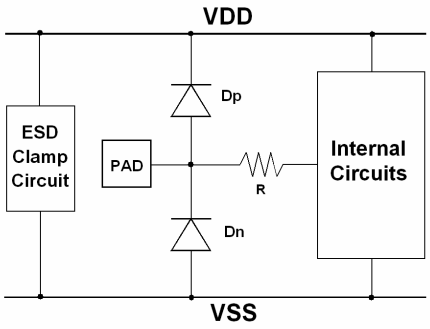


Fig. 1. The typical ESD protection design for an input pad with double diodes and the power-rail ESD clamp circuit.

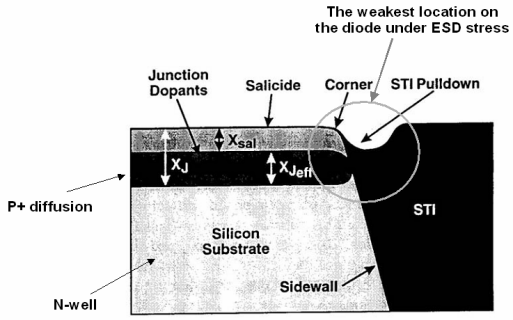
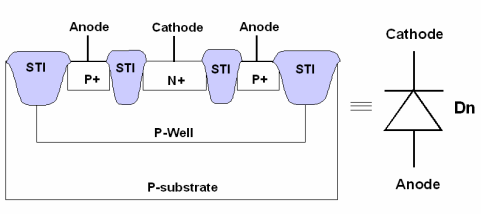


Fig. 2. The pull-down weakest point at the boundary between the shallow-trench isolation (STI) region and the diffusion edge of the diode structure.

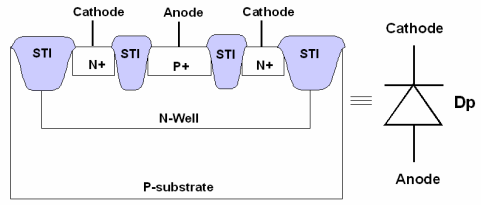
II. THE DIODE STRUCTURES

A. Normal N-type and P-type Diodes

The cross-sectional view of the normal N-type diode (Dn) and P-type diode (Dp) realized in the 0.15-μm CMOS process are shown in Figs. 3(a) and 3(b), respectively. For the normal N-type diode, N+ diffusion (as the cathode) is placed in a P-well in P-substrate to form the p/n junction of the diode. The anode of such an N-type diode is connected out by the P+ diffusion in the P-well (or p-substrate). For the normal P-type diode, P+ diffusion (as the anode) is placed in an N-well to form the p/n junction of the diode. The cathode of such a P-type diode is connected out by the N+ diffusion in the N-well. Such diodes had been fabricated in the testchips to verify its ESD robustness.

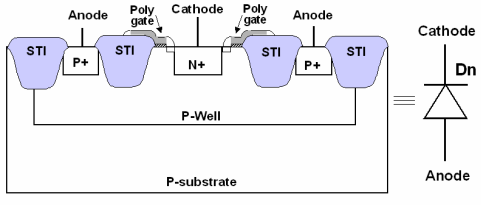


(a)

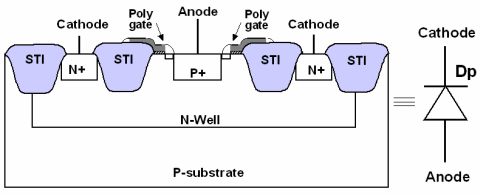


(b)

Fig. 3. The device cross-sectional views of (a) the normal N-type diode, and (b) the normal P-type diode, in CMOS process.



(a)



(b)

Fig. 4. The device cross-sectional views of (a) the Poly/STI-bounded N-type diode, and (b) the Poly/STI-bounded P-type diode, in CMOS process.

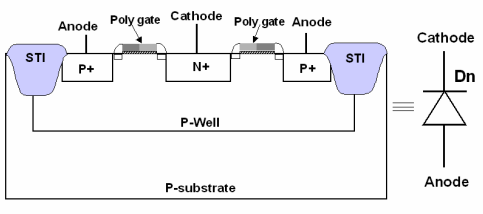
B. Poly/STI-Bounded N-type and P-type Diodes

To overcome the weakest ESD-damaged location at the p/n junction diffusion to the STI boundary, a modified diode structure with dummy gate [6], called as the Poly/STI-bounded N-type (P-type) diode, is shown in Figs. 4(a) and 4(b).

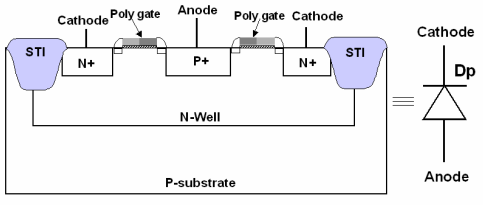
As comparing to Fig. 3, the STI regions between the P+ and N+ diffusions are removed away from the N+ (P+) diffusion of the normal N-type (P-type) diode and replaced by the dummy poly gates. The dummy poly gates are located half on the P-Well (N-Well) region and half on the STI region. Therefore, there is no STI boundary to the N+ (P+) diffusion edge of the Poly/STI-bounded N-type (P-type) diode. Without the STI boundary at the p/n junction of the diodes, the pull-down and bend-down corner in Fig. 2 to cause low ESD robustness can be overcome. Such diodes had been fabricated in the testchips to verify its ESD robustness.

C. Poly/Poly-Bounded N-type and P-type Diodes

Another modified diode structure has the same concept with the Poly/STI-bounded diode to avoid the weakest ESD-damaged location at the p/n junction diffusion to the STI boundary [6], called as the Poly/Poly-bounded N-type (P-type) diode, is shown in Figs. 5(a) and 5(b).

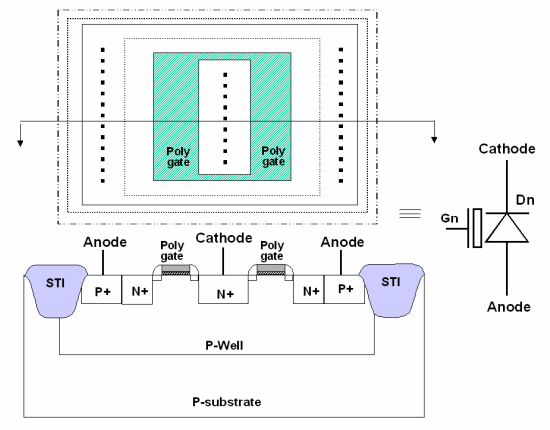


(a)

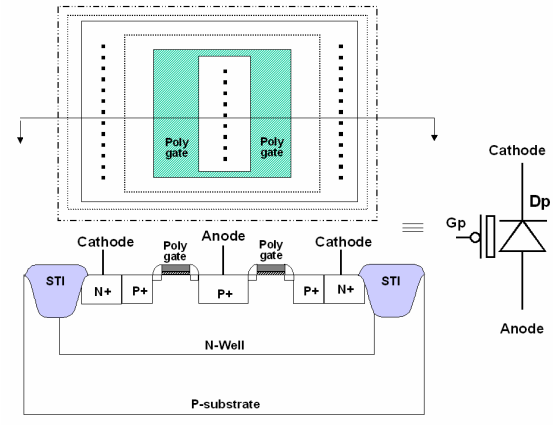


(b)

Fig. 5. The device cross-sectional views of (a) the Poly/Poly-bounded N-type diode, and (b) the Poly/Poly-bounded P-type diode, in CMOS process.



(a)



(b)

Fig. 6. The layout top views and the device cross-sectional views of (a) the NMOS-bounded diode, and (b) the PMOS-bounded diode, in a CMOS process.

Without STI regions between the P+ and N+ diffusions of the diode, the dummy poly gate fully replaces STI to isolate P+ and N+ diffusions of Poly/Poly-bounded diode. The dummy poly gate is half covered by the N+ implantation and half by the P+ implantation. Such diodes had been also fabricated in the testchips to verify its ESD robustness.

D. NMOS-Bounded and PMOS-Bounded Diodes

The layout top views and the device cross-sectional views of the proposed NMOS-bounded diode and PMOS-bounded diode are shown in Figs. 6(a) and 6(b), respectively. The N(P)MOS-bounded diode has a N(P)MOS structure inserted in the diode structure.

The NMOS-bounded diode has a cathode of N+ diffusion, which does not directly touch the P+ diffusion in the diode structure. The diode anode of P+ diffusion directly touches another N+ diffusion in the NMOS-bounded diode, but this N+ diffusion is floating in the device structure. The anode of the PMOS-bounded diode is the P+ diffusion in the center, which does not directly touch the N+ diffusion. The cathode of diode is the N+ diffusion, which directly touches another P+ diffusion in the structure, but this P+ diffusion is floating in the device structure. In this N(P)MOS-bounded diode, the poly gate is fully covered by the N+ (P+) implantation, therefore the gate can be successfully formed on the NMOS (PMOS) channel. If there is correct gate bias on the NMOS (PMOS) gate, the diode turn-on speed can be enhanced to fast discharge the ESD current. Therefore, it can provide more effective protection to the internal circuits. The poly gate in the layout top view shown in Fig. 6 has a close-loop ring to block the STI boundary from the cathode N+ diffusion (anode P+ diffusion) of the N(P)MOS-bounded diode structure. This proposed N(P)MOS-bounded diode is fully compatible to the general CMOS processes without any additional process step or extra mask layer. Such novel diodes had been also fabricated in the testchip in a 0.15-μm CMOS process to verify its ESD robustness, and to compare with the normal diode, Poly/STI-bounded diode, and Poly/Poly-bounded diode.

III. EXPERIMENTAL RESULTS

The proposed new diodes, the traditional normal diodes, Poly/STI-bounded diodes, and Poly/Poly-bounded diodes had been fabricated in a 0.15-μm STI salicided CMOS process

A. ESD Robustness

The second breakdown current (It2) of four kinds of diodes under reverse-biased condition, measured by the transmission line pulse generator (TLPG) [7] with pulse width of 100ns is used to verify their ESD robustness. Figs. 7(a) and 7(b) show the measured I-V characteristics of N-type diodes and P-type diodes with diode junction perimeter of 100μm under reverse-biased condition. The poly gate is connected to P+ anode (N+ cathode) for N-Type (P-Type) diodes during the pulse of TLPG. From the experimental results, the normal diode has the much higher turn-on voltage (junction breakdown voltage) of ~11V and larger turn-on resistance as compared to other diode structures. The normal diode and Poly/STI-bounded diode, with higher holding voltage and larger turn-on resistance due to the N+ and P+ diffusions in the diode blocked by STI, can't provide efficient ESD protection to the internal circuits in sub-quarter-micron CMOS technology with much thinner gate oxide thickness. The NMOS-bounded diode and PMOS-bounded diode have the smallest turn-on resistance, the lowest holding voltage, and comparable It2 level among four kinds of diodes. Fig. 8 shows the reverse-biased It2 level of NMOS-bounded diode, Poly/STI-bounded N-type diode, and Poly/Poly-bounded N-Type diode, measured by TLPG under different gate biases. The It2 level of NMOS-bounded diode can be improved higher than other diode structures under suitable gate bias (~1V) on the NMOS gate. Therefore, it can provide more effective protection to the internal circuits. Some on-chip ESD protection circuits can be therefore designed to generate the suitable voltage to the dummy gates of the NMOS-bounded and PMOS-bounded diodes during ESD zapping. Two typical on-chip ESD protection circuits for input pads realized with the proposed MOS-bounded diodes are shown in Figs. 9(a) and 9(b).

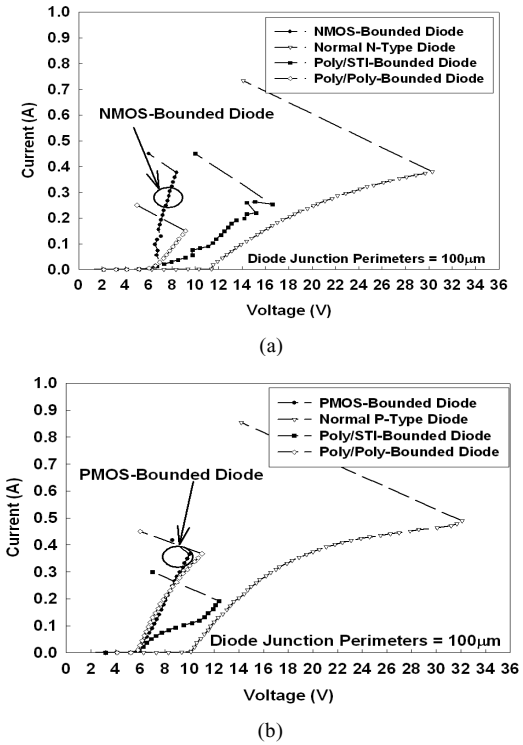


Fig. 7. The measured I-V characteristics of four kinds of (a) the N-type diodes, and (b) the P-type diodes, under reverse-biased condition by TLPG with a pulse width of 100ns.

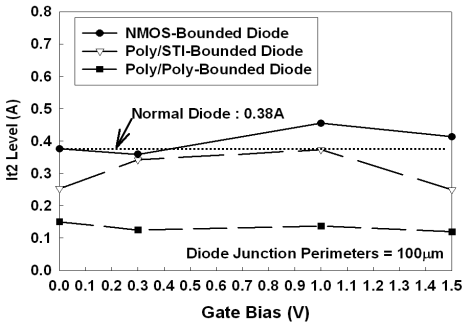


Fig. 8. The reverse-biased It2 level of NMOS-bounded diode, Poly/STI-bounded N-type diode, and Poly/Poly-bounded N-type diode, measured by TLPG under different gate biases.

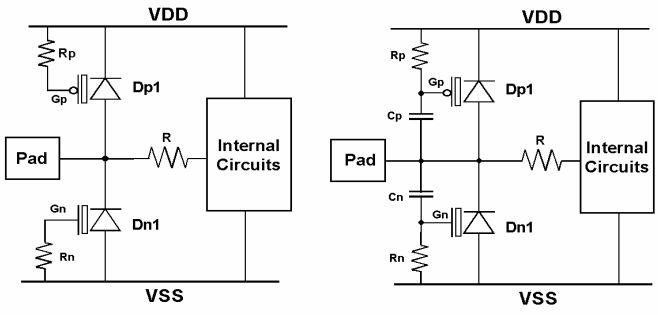


Fig. 9. The ESD protection circuits with the NMOS-bounded and PMOS-bounded diodes for the input pads, where (a) poly gate of the N(P)MOS-bounded diode is connected to VSS (VDD) through a resistor, and (b) gate-couple technique is applied.

B. Turn-On Verification

A voltage pulse generated from a pulse generator with a pulse height of 20 V and a rise time of ~ 10ns, as shown in Fig. 10, is used to simulate the rising edge of an ESD pulse. Such a voltage pulse is applied to the four kinds of diodes under reverse-biased condition to verify the turn-on behavior of the diodes. The voltage waveforms clamped by the N-type diodes and P-type diodes are shown in Fig. 11 and Fig. 12, respectively. The clamped voltage level of the diodes has the sequence of: normal diode > Poly/STI-bounded diode > Poly/Poly-bounded diode > MOS-bounded diode, which is consistent with the I-V characteristics measured by TLPG. The higher junction breakdown voltage and higher turn-on resistance cause higher clamped voltage level. The MOS-bounded diode has the lowest clamped voltage of 7~8V.

Therefore, the proposed NMOS-bounded and PMOS-bounded diodes are more suitable than the normal diodes, Poly/STI-bounded diodes, and Poly/Poly-bounded diodes for ESD protection design in sub-quarter-micron CMOS processes.

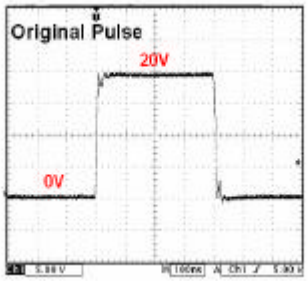


Fig. 10. The voltage waveform of the original 0-20-V voltage pulse generated from the pulse generator. (X-axis: 100ns/Div., and Y-axis: 5V/Div.)

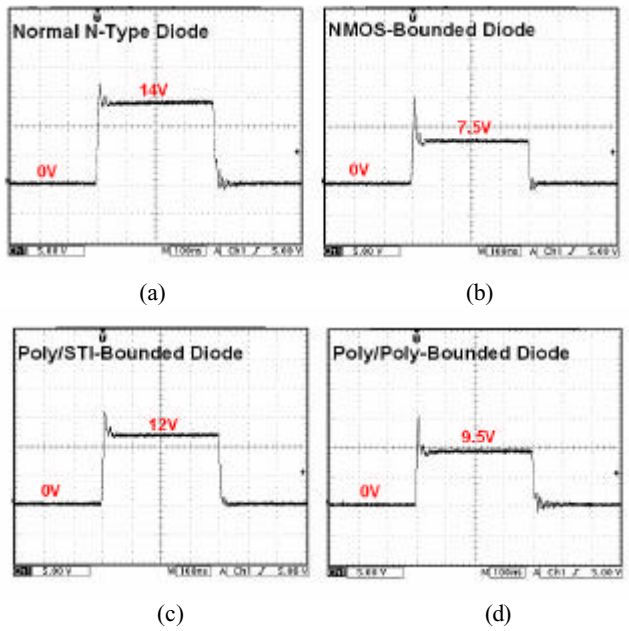


Fig. 11. The clamped voltage waveforms by (a) the normal N-type diode, (b) the NMOS-bounded diode, (c) the Poly/STI-bounded N-type diode, and (d) the Poly/Poly-bounded N-type diode, under reverse-biased condition. (X-axis: 100ns/Div., and Y-axis: 5V/Div.)

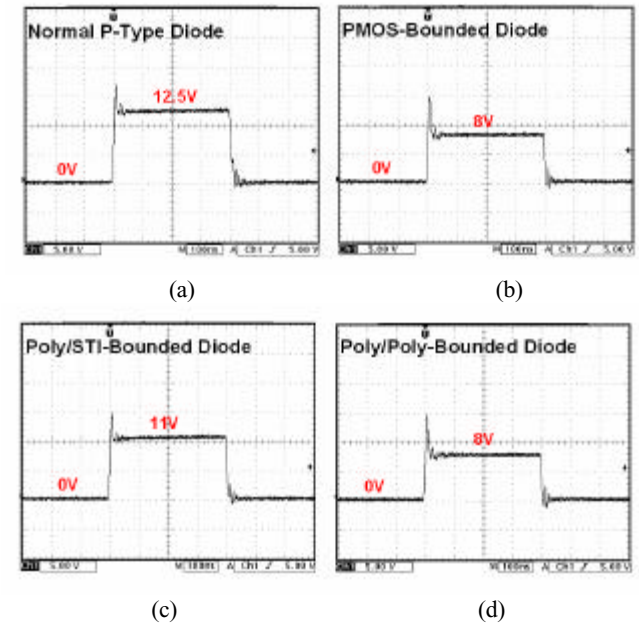


Fig. 12. The clamped voltage waveforms by (a) the normal P-type diode, (b) the PMOS-bounded diode, (c) the Poly/STI-bounded P-type diode, and (d) the Poly/Poly-bounded P-Type diode, under reverse-biased condition. (X-axis: 100ns/Div., and Y-axis: 5V/Div.)

IV. CONCLUSION

I-V characteristics, It2, and turn-on behaviors of N(P)MOS-bounded diode for ESD protection in a 0.15-μm CMOS process have been investigated and compared to that of normal N(P)-type diode, Poly/STI-bounded N(P)-type diode, and Poly/Poly-bounded N(P)-type diode. The experimental results have confirmed that the new proposed MOS-bounded diode structures are more suitable for on-chip ESD protection design among these diodes in a 0.15-μm STI salicided CMOS process.

REFERENCES

[1] A. Amerasekera and C. Duvvury, "The impact of technology scaling on ESD robustness and protection circuit design," in *Proc. of EOS/ESD Symp.*, 1994, pp. 237-245.

[2] G. Notermans, A. Heringa, M. Van Dort, S. Jansen, and F. Kuper, "The effect of silicide on ESD performance," in *Proc. of IEEE Int. Reliability Physics Symp.*, 1999, pp. 154-158.

[3] Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM), Test Method Standard STM5.1, ESD Association, USA, 1998.

[4] J. Bernier, G. Croft, and W. Young, "A process independent ESD design methodology," in *Proc. of IEEE Int. Symp. on Circuits and Systems*, 1999, pp. 218-221. M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. on Electron Devices*, vol. 46, pp. 173-183, 1999.

[6] S. Voldman, S. Geissler, J. Nakos, J. Pekarik, and R. Gauthier, "Semiconductor process and structural optimization of shallow trench isolation-defined and polysilicon-bound source/drain diodes for ESD networks," in *Proc. of EOS/ESD Symp.*, 1998, pp. 151-160.

[7] H. Hyatt, J. Harris, A. Alanzo, and P. Bellew, "TLP measurements for verification of ESD protection device response," in *Proc. of EOS/ESD Symp*., 2000, pp. 111-120.