# Evaluation on ESD Robustness of LTPS Diode and TFT Device by Transmission Line Pulsing (TLP) Technique

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## ABSTRACT

ESD robustness of Low Temperature Poly-Si (LTPS) diodes and TFT devices has been investigated in this paper. By using the Transmission Line Pulsing (TLP) techniques, the It2 (secondary breakdown current) of LTPS diodes and TFT devices were measured. To evaluate the ESD robustness of components for ESD protection, the shifts of breakdown voltage and cut-in voltage of LTPS diode and TFT devices after TLP stress are considered into failure threshold judgment. From the experimental results, It2 of LTPS diodes under forward-biased stress is better than that of LTPS TFT devices. Furthermore, the It2 of LTPS TFT devices under reverse-biased stress is more robust than it under forward-biased stress. Such investigation results can help us to design a successful ESD protection for the circuits on glass.

## INTRODUCTION

System on panel (SOP), combined with memory, controller, and driver circuits on a glass substrate, will be the most suitable applications for TFT-LCD or TFT-OLED panels in the near future [1]. As the time of SOP is approaching, ESD reliability issue of TFT-LCD system is not only an oncoming problem but also an extremely worth-concern problem. In the silicon base CMOS technologies, several advanced whole chip ESD protection schemes have been proposed [2]-[3]. For LTPS circuits, the whole chip protection scheme should be a promising solution. In order to evaluate the ESD robustness of LTPS circuits, the It2 (which represents the ESD robustness of a device) of LTPS device must be investigated first. Recently, there are some papers studied ESD robustness of LTPS TFT devices [4]-[8].

In this paper, the ESD characteristics of both LTPS diode and LTPS TFT devices have been evaluated under different layout parameters. Moreover, the reliability issue and its physical mechanism of LTPS diodes and TFT devices after TLP stress have been discussed in detail.

## TEST DEVICES

### *Device Fabrication*

The LTPS TFT devices were fabricated on the glass substrate. Firstly, buffer oxide and α-Si:H films were deposited on glass substrate by PECVD system. After XeCl excimer laser was used to crystallize α-Si:H film, the poly-Si film was patterned. Subsequently, gate insulator was deposited by PECVD. After source and drain regions impurities doping, the interlayer was deposited by PECVD. Finally, doping activation and hydrogenation were done to get better electrical characteristics.

### *Layout Structure*

Fig. 1 shows the layout top view of (a) LTPS diodes and (b) LTPS n-channel TFT devices. The diode structure shown in Fig. 1(a), is fully process-compatible to LTPS TFT processes without extra mask. For low leakage consideration, the LTPS diode was designed with p+-i-n+ structure. The intrinsic region "i" is formed under the metal gate, that is a mask to block n- LDD doping. The width of intrinsic poly region "s", the p+ contact to metal gate space "a", and the n+ contact to metal gate space "b" were key layout parameters for ESD consideration, which will be investigated in this paper. For the LTPS n-channel TFT in Fig. 1(b), the ESD related layout parameter "x" in the channel length, where channel length is 11μm+2x in the device, will be investigated.

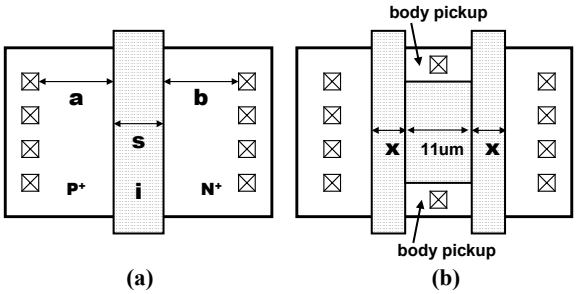


**Fig. 1** The layout top views of (a) LTPS diode, and (b) LTPS TFT device with body pickup.

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## EXPERIMENTAL RESULTS

### *It2 of LTPS Diodes*

The It2 of both LTPS diodes and TFT devices were measured by using Transmission Line Pulsing (TLP) system that generated high stress current of ESD-like pulse. The pulse width generated by TLP system is about 100ns with a rise time of 10ns. Moreover, the failure criteria for device under test is defined as TLP measured I-V curve showing obviously secondary breakdown with negative resistance. The It2 is defined as the current at the beginning of the secondary breakdown point with negative resistance. After the It2, the devices were permanently damaged.

The measured TLP I-V curves of LTPS diodes under forward-biased and reverse-biased stress are shown in Fig. 2. The It2 of LTPS diodes with a channel width of 400μm under forward-biased stress is 0.58A, which is much higher than that under reverse-biased stress, 0.12A. The cut-in voltage and breakdown voltage of p+-i-n+ diode under forward-biased stress and reverse-biased stress are 1.0volt and 60.0volt, respectively. The LTPS diodes under forward-biased stress not only sustain higher ESD stress but also turn on more quickly. Once the LTPS p+-i-n+ diode turns on under reverse-biased stress by avalanche mechanism, it burns out easily.

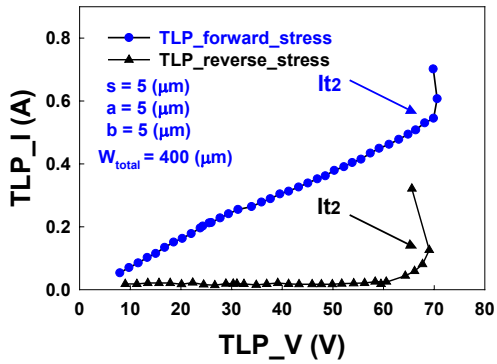



**Fig. 2** The TLP_IV curves of LTPS diodes under forward- and reverse-biased TLP stress.

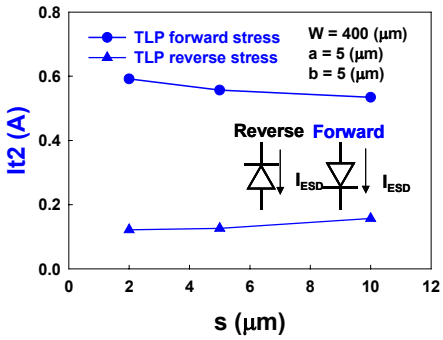



**Fig. 3** The dependence of TLP-measured It2 on the layout parameters in LTPS diodes under forward and reverse stress.

The It2 of LTPS diodes related to the "s" region is shown in Fig. 3. When the "s" increases, the It2 under forward-biased stress slightly decreases due to higher turn-on resistance. The It2 of LTPS diodes under forward-biased stress is about 5 times larger than that under reverse-biased stress. Further, the other layout parameters for ESD consideration are "a" and "b" region which are the distance between the contact and gate metal in p+ and n+ side respectively. In Fig. 4, the It2 increases with the "a" space shrinking. This is due to the lower turn-on resistance in shorter "a" region. The reason is the same as the relationship between It2 and "b" region, as that shown in Fig. 5. To realize LTPS diodes as ESD clamp devices, the optimum layout structure of LTPS diodes should be designed with shorter "a" and "b", and the "s" value of LTPS diodes shall be traded off for the consideration of not only ESD robustness but also the low leakage current.

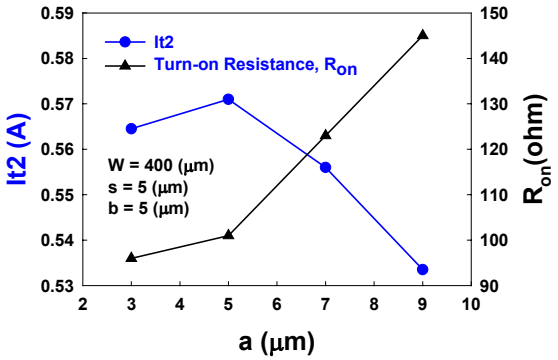



**Fig. 4** The dependence of TLP measured It2 and turn-on resistance on the layout parameter of "a" of LTPS diode.

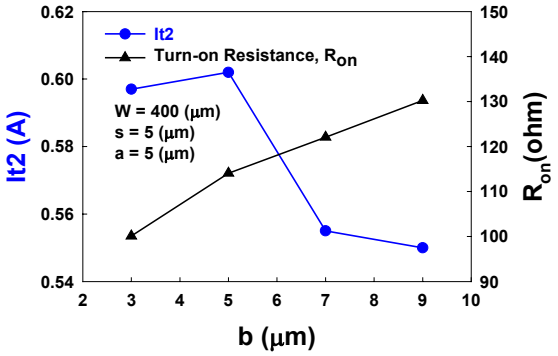



**Fig. 5** The dependence of TLP measured It2 and turn-on resistance on the layout parameter of "b" of LTPS diode.

### *It2 of LTPS TFT Devices*

The measured TLP I-V curves of n-channel TFT devices under forward-biased and reverse-biased stress are shown in Fig.6. When the LTPS TFT device is under forward-biased stress, it turns on at less than 30volt, which is less than that under reverse-biased stress, ~75volt. Moreover, the It2 of n-channel TFT under forward-biased stress is lower than that

under reverse-biased stress. This result is quite different to that seen in the CMOS devices.

The relationship between the It2 and the length "x" is shown in Fig. 7. The circuit connection of gate electrode for forward and reverse TLP stress is shown in the inserted picture of Fig. 7. The body pickups are floated in this measurement. The It2 of LTPS TFT device under reverse-biased stress is about 3 times larger than that under forward-biased TLP stress. The reason is due to floating body of TFT device under forward-biased stress has no real diode-forward path in polysilicon film. Although the TFT under forward-biased stress will turn on earlier, the large gate bias makes the ESD current overcrowding in channel surface. To solve this problem, the layout structure of TFT device should be further improved in the future. The It2 of LTPS TFT under reverse-biased stress is above 0.6A, but the high secondary breakdown voltage (Vt2), is as high as 102volt, which has a danger to damage the gate oxide. Therefore, the slow turn-on speed and the large turn-on voltage of the TFT devices under reverse-biased stress should be improved by substrate-triggered or gate-driven techniques [9].

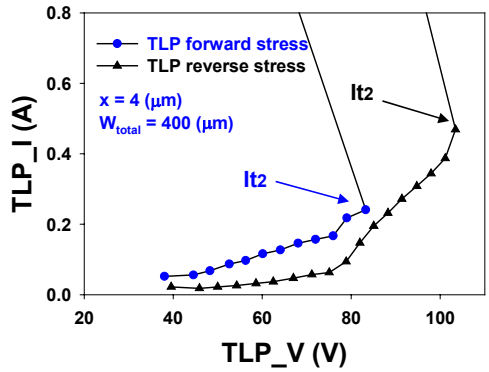



**Fig. 6** The TLP_IV curves of LTPS TFT device under forward-biased and reverse-biased stress.

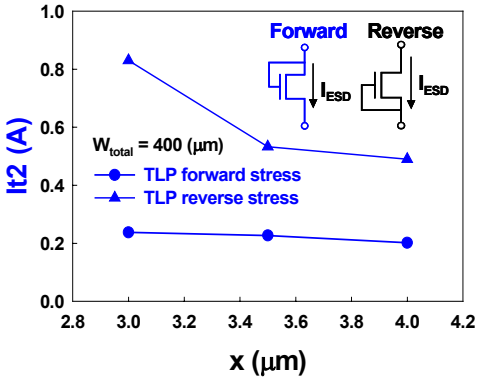
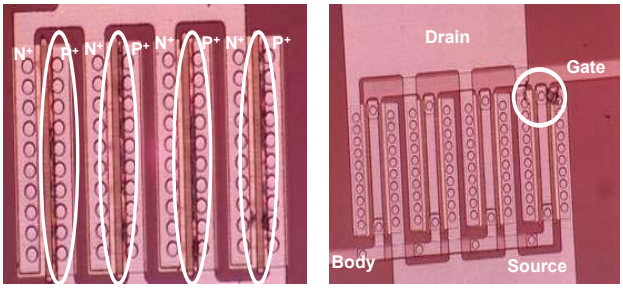



**Fig. 7** The dependence of TLP-measured It2 on the layout parameter "x" in LTPS TFT devices under forward-biased and reverse-biased stress.

*Failure Spots*

The failure spot of LTPS diode under forward bias is shown in Fig. 8(a). The failure spots identify the uniformly turn-on under forward TLP stress of LTPS diode. The burned-out region is uniformly located at each finger of p+ side due to the higher electric field at p+-i junction. The It2 will be improved by graded p-type doping profile at p+-i junction. The failure spot of LTPS TFTs under forward stress is shown in Fig. 8(b). The gate region near the corner has been burned out firstly. That is to say that LTPS TFT device under forward TLP stress has a serious non-uniformly turn-on effect. The reason is that the symmetry structure of LTPS TFT device has a floating body effect so that there is no parasitic junction diode from body to drain. When TFT device operates under forward TLP stress, the lager gate bias induces serious hot-carrier injection into gate electrode and then the gate burns out.




**(a)** **(b)**

**Fig. 8** The failure spots of (a) LTPS diode under forward stress and (b) LTPS TFTs under forward stress.

*Shifting of I-V Curves after TLP Stress*

There is an interesting phenomenon. If the LTPS diode and TFT device are stressed by TLP until the negative resistance happened, the failure spot region of LTPS diode will become open, then may make diode operate normally again, but that of LTPS TFT is not recoverable.

Fig. 9 shows the breakdown voltage ($V_{BD}$) and the cut-in voltage ($V_{cut-in}$) of LTPS diode under forward -biased stress. The failure spots of LTPS diode reduce the effective channel width after forward-biased stress. The LTPS diode with a 5-μm "a" region has a $V_{BD}$ of 44.8volt and a $V_{cut-in}$ of 0.62volt before TLP stress, where the $V_{BD}$ and $V_{cut-in}$ is defined at the current of 1μA. After the TLP stress, the failure spot is visible from OM system, and the $V_{BD}$ and $V_{cut-in}$ of LTPS diode becomes to 44.6volt and 0.56volt, respectively. Furthermore, the LTPS diode after first TLP stress has been measured again by TLP system and the other TLP_IV curve was obtained, as those shown in Fig. 10. The turn-on resistance and It2 under first TLP forward-biased stress are 123.5ohm and 0.55A, respectively. The secondly-measured TLP I-V curve of LTPS diode has a higher turn-on resistance of 294.1ohm and a lower

It2' of 0.28A due to the reduction of effective channel width after TLP forward-biased stress. After the second TLP stress, the LTPS diode was fully opened from drain to source. This phenomenon also supports the point that the LTPS diode was easily burned out to open not to short under TLP forward-biased stress.

On the other way, the shifts of $V_{BD}$ and $V_{cut\text{-}in}$ of LTPS TFT devices under forward-biased TLP stress were shown in Fig. 11. The TFT device with "x" region of 5μm has a $V_{BD}$ of 55.3volt and a $V_{cut\text{-}in}$ of 1.2volt before forward-biased stress. After TLP forward-biased stress, the $V_{BD}$ and $V_{cut\text{-}in}$ become 39.4volt and 12.3volt, respectively. The $V_{cut\text{-}in}$ after TLP stress is 10 times larger than that before TLP stress, and the $V_{BD}$ shifts more than 15volt. This is due to the shift of threshold voltage under hot carrier injection.

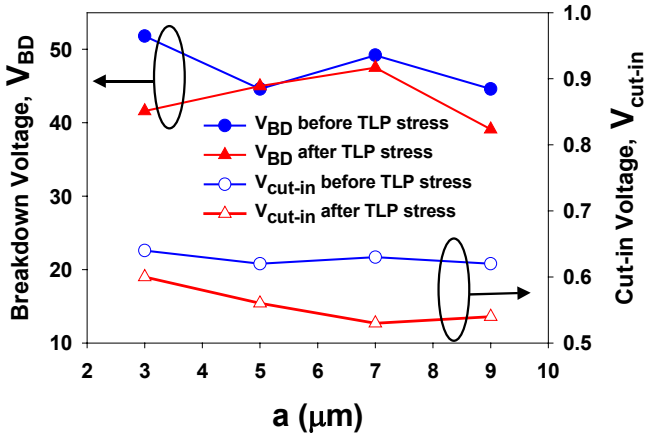



**Fig. 9** The shifts of $V_{BD}$ and $V_{cut\text{-}in}$ of LTPS diodes after forward-biased TLP stress.

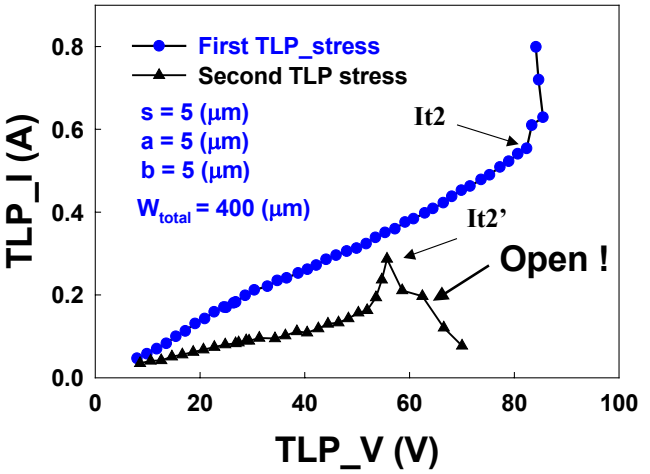



**Fig. 10** The TLP I-V curves of LTPS diodes between first TLP stress and second TLP stress.

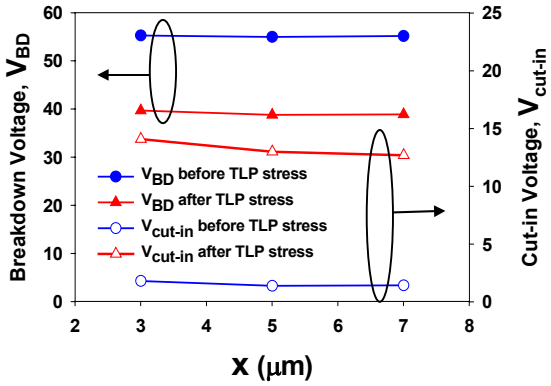



**Fig. 11** The shifts of $V_{BD}$ and $V_{cut\text{-}in}$ of LTPS TFT devices after forward-biased TLP stress.

## CONCLUSION

The ESD robustness of LTPS diodes and LTPS TFT devices with different layout parameters has been investigated in this paper. The experimental data shows that both the LTPS diode with a shorter "s" and LTPS TFT with a shorter channel length achieve higher ESD robustness. The TFT device under forward-biased stress is not robust due to its floating body. In summary, the LTPS diode with low-triggered voltage and higher ESD robustness under forward-biased stress will be a good device for ESD protection. The TFT device should be improved not only the layout structure but also the extra biased techniques to improve the drawback of high turn-on voltage.

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