Optimization of Broadband RF Performance and ESD Robustness by π-model Distributed ESD Protection Scheme

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Abstract − Large electrostatic discharge (ESD) protection devices close to the I/O pins, beneficial for ESD protection, have an adverse effect on the performance of broadband RF circuits for impedance mismatch and bandwidth degradation. A new proposed ESD protection structure, π-model distributed ESD (π-DESD) protection circuit, composed of one pair of ESD devices near the I/O pin, the other pair close to the core circuit, and a coplanar waveguide with under-grounded shield (CPWG) connecting these two pairs, can successfully achieve both excellent ESD robustness and good broadband RF performance. Cooperating with the active power-rail ESD clamp circuit, the experimental chip in a 0.25-μm CMOS process can sustain the human-body-model (HBM) ESD stress of 8kV.

I. Introduction

The continuous scaling of CMOS technology and the rapid increase of operation frequency in radio-frequency (RF) ICs has caught a high challenge to on-chip ESD protection design. To fulfill the requirement of RF performance, the ESD protection device in such RF applications was often designed with small device size to reduce its parasitic capacitance [1], and placed close to the I/O pins. However, for the RF systems demanding wider frequency bandwidths, the small-size ESD protection scheme still causes degradation to RF performance. Recently, the distributed ESD protection scheme has shown good broadband RF performance [2]-[5]. In [2], the gate-grounded NMOS device was used with series N-well resistor in its drain, beneficial for uniform turn-on behavior during ESD events, to achieve high ESD level. However, the large thermal noise contributed from the N-well resistor limited its applications in higher frequency RF systems. To improve the impedance match over a wider range of frequencies, a distributed ESD (DESD) protection scheme had been reported in Fig. 1 [3]-[5]. A four-stage DESD protection scheme with ESD devices (p-diodes and n-diodes) of equal small size was calculated to provide a good impedance match over a broad frequency range, but the ESD robustness was neither mentioned nor verified in those reports.

In this paper, a new π-model distributed ESD (π-DESD) protection scheme is proposed to achieve both of great broadband RF performance and excellent ESD robustness for broadband RF circuits. An experimental chip realized in a 0.25-μm CMOS process has been designed and measured to prove its performance. As comparing to the distributed ESD protection scheme [3]-[5], this new proposed π-DESD protection scheme has achieved better RF performance and much higher ESD robustness (>8kV, HBM).

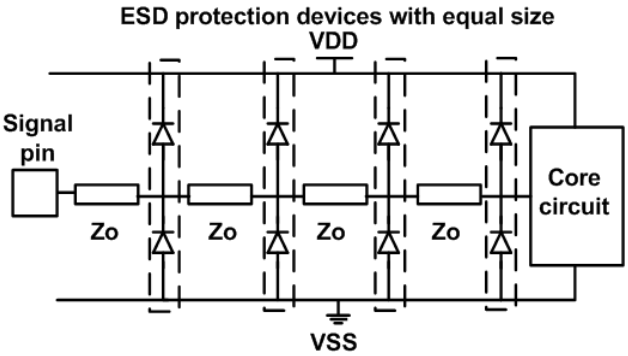


Figure 1: The distributed ESD (DESD) protection scheme with equal-size diodes in four ESD stages [3]-[5].

II. π-model Distributed ESD Protection Scheme

A. Design Concept

The traditional ESD protection scheme has limitation to provide both high ESD robustness and broadband RF performance. From the perspective of ESD protection, the ESD protection devices were often designed with large device sizes and placed near the signal pins, as that shown in Fig. 2. But, for broadband RF performance consideration, the ESD protection devices are preferred to be divided into many small units with the same device size and connected by transmission lines (T-lines) or inductors, as that shown in Fig. 1.

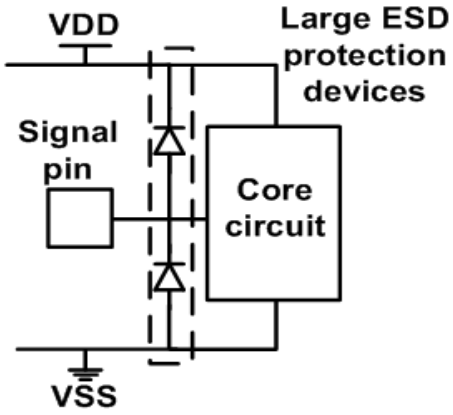


Figure 2: The traditional ESD protection design with large ESD device close to the signal pin to sustain ESD stress.

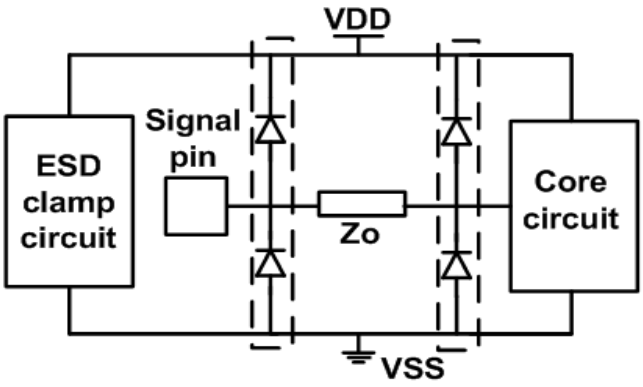


Figure 3: The new proposed π-model distributed ESD (π-DESD) protection scheme.

The dilemma can be overcome by the new proposed π-model distributed ESD (π-DESD) protection scheme, as that illustrated in Fig. 3. Acting as a π model in ac analysis, the π-DESD protection is composed of two pairs of ESD protection devices, where one is close to the signal pin and the other is near the internal circuit. A specially designed T-line is used to connect these two pairs. By using the new proposed π-DESD protection scheme, the impedance match for RF signals can be optimized to have a better RF performance. With a larger ESD device size close to the I/O pad in the π-DESD protection scheme, it can sustain a higher ESD level than that with a smaller ESD device size in the four-stage distributed ESD protection scheme.

B. Matching Analysis with Smith Chart

S parameters are the important indexes in RF system to show the frequency response. Starting with a standard 50-Ω system which has been commonly used in RF systems, the equivalent ac models of the traditional equal-size distributed ESD (ES-DESD) protection scheme (shown in Fig. 1) [3]-[5], and the new proposed π-DESD protection scheme (shown in Fig. 3) are illustrated in Figs. 4(a) and 4(b), respectively. In each circuit, the ESD protection devices are modeled as capacitors. It had been demonstrated that the coplanar waveguide with grounded shield (CPWG) can provide excellent RF performance for frequencies over 10 GHz [6], [7]. So, the on-chip CPWG is used in this work with the specified characteristic impedance (Zo) to match the parasitic capacitances generated from ESD devices.

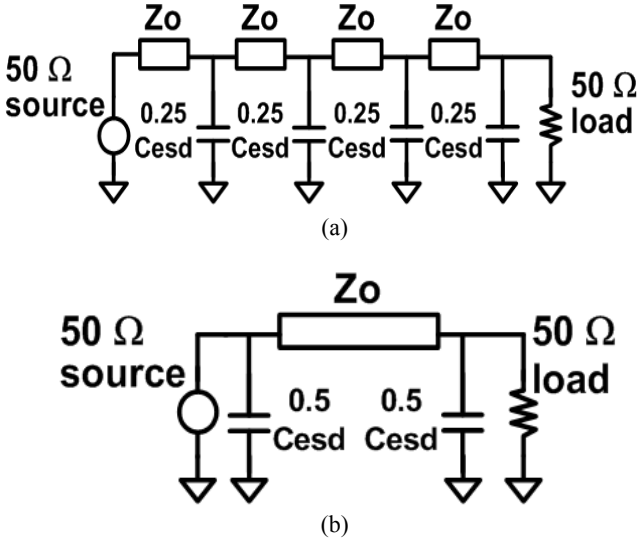


Figure 4: The equivalent RF circuit models of (a) the ES-DESD protection scheme and (b) the new proposed π-DESD protection scheme.

The ESD protection devices in RF circuit should be chosen without contributing large resistances and capacitances for the noise and match concerns. Q factors are often used to evaluate the qualities of the ESD protection devices. Diodes have been commonly used for ESD protection in RF systems due to their low parasitic capacitances [8], as comparing to other ESD devices, such as the gate-grounded NMOS. In this work, the shallow-trench-isolation (STI) diodes are employed due to their high Q value [8] and good ESD robustness under forward-biased condition. Initially, the total ESD capacitance (Cesd) was assumed to be 200 fF, a value sufficient to reach the HBM ESD level of 2kV [9]. The corresponding layout dimension for the ESD diodes to generate the parasitic capacitance of 200 fF can be estimated from the CMOS process parameters with consideration of the both bottom-plate and the side-wall capacitances. The characteristic impedance (Zo) of on-chip CPWG is chosen at 70 Ω, when considering the layout dimension of the metal line and the distance from the top metal layer to the p-type substrate in a given 0.25-μm CMOS process.

Simulations on the S parameters over the frequency range of 1 ~ 15 GHz are performed on these two ESD protection schemes. By using the microwave circuit simulator ADS, the reflection parameter S11 and the transmission parameter S21 under the neglect of the loss along CPWG can be calculated. The S11, related to the impedance match, is the main consideration to compare these two ESD protection schemes in Fig. 4. The matching principles explained in the Smith charts, with the operating frequency at 10 GHz, are shown in Figs. 5(a) and 5(b) for the ES-ESD and π-DESD protection schemes, respectively. The length of each CPWG has been optimized to reach the desired impedance match for each circuit. The center point of Smith chart is normalized to 50 Ω. The serial number labeled on each point indicates the matching procedure along the ESD devices and CPWG from the internal core circuit (modeled as 50-Ω load) to the external 50-Ω source at the input node.

Fig. 5(a) shows the S11 locus of the four-stage equal-size ESD protection scheme of Fig. 4(a), which has a final matching result back to the real axis of the Smith chart, but not the original center point. With the final point coming back to the original center point in Fig. 5(b), a more excellent impedance matching result can be achieved by the new proposed π-DESD protection scheme of Fig. 4(b). The concept of the π-DESD match in Fig.5(b) is quite different from that of the ES-DESD match in Fig.5(a). The ES-DESD protection scheme tunes the impedance back to the real axis on Smith chart after each shunt parasitic capacitor by the CPWG. The π-DESD protection scheme, deliberately, employs a single section of CPWG to tune the S11 (impedance) crossover the real axis, but it can finally return back to the original center point (50 Ω) with co-design of the parasitic capacitance in the first-pair ESD diodes.

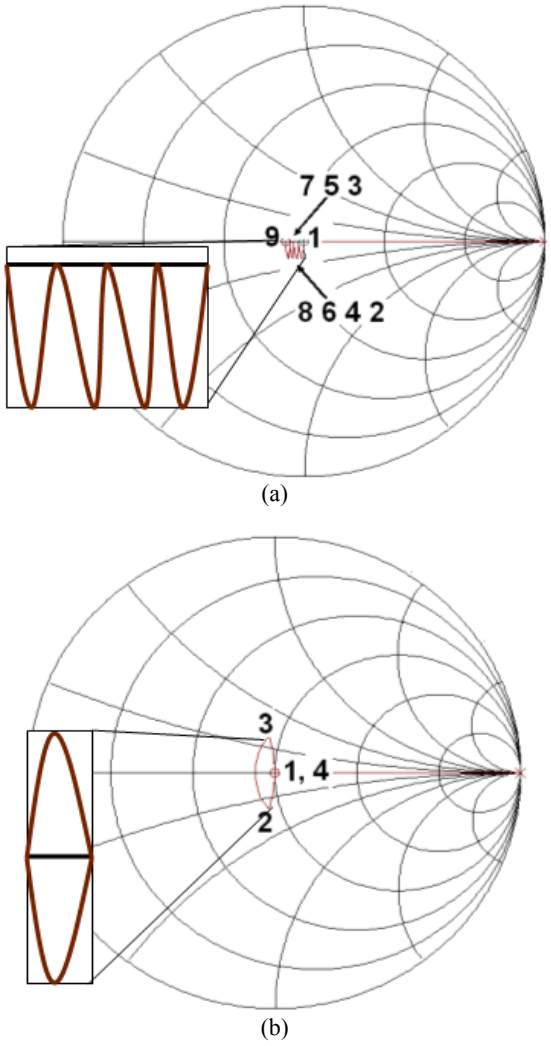


Figure 5: The matching procedures explained on Smith chart for (a) the ES-DESD protection scheme and (b) the new proposed π-DESD protection scheme.

C. Consideration on ESD Robustness

During ESD events, the RF input pin could be applied with positive or negative ESD voltage with the VDD or VSS pin relatively grounded. So, there

are four modes of ESD stresses on the RF input pin, which are the positive-to-VSS (PS), negative-to-VSS (NS), positive-to-VDD (PD), and negative-to-VDD (ND) ESD-stress modes. The ESD level for an input/ output pin is often defined as the lowest ESD level among the four modes of ESD stresses. Hence, the on-chip ESD protection design should provide effective ESD discharging paths for the four modes of ESD stresses. The turn-on efficient power-rail ESD clamp circuit with RC-based ESD detection circuit has been applied to ensure the ESD protection devices operating in the forward-biased condition [10]-[12], under the four ESD-stress modes on the I/O pad. In this work, the turn-on efficient power-rail ESD clamp circuit is also used to cooperate with the π-DESD protection scheme to make sure the ESD diodes operating in the forward-biased condition during ESD stresses.

To further estimate ESD robustness, the resistive-ladder model on the ES-DESD protection scheme is employed and shown in Fig. 6. The large values of the series resistance from CPWG (Rc) and the resistance from ESD device (Resd) will degrade ESD tolerance of the ES-DESD protection scheme, due to the huge power across them during ESD events. In the new proposed π-DESD protection scheme, the first pair of ESD diodes is directly connected to the pad with half of the total ESD device size. So, the π-DESD protection scheme has a lower Resd, as comparing to that of the four-stage ES-DESD protection scheme under the same total size of ESD diodes. Moreover, the new proposed π-DESD protection scheme has no first series resistance of CPWG (Rc) connecting from the first pair of ESD diodes to the pad. Without the first stage of Rc and with the reduced Resd, the new proposed π-DESD protection scheme can provide more efficient current path to discharge ESD current from the pad to ground. Therefore, it will have a better ESD robustness than that of the ES-DESD protection scheme.

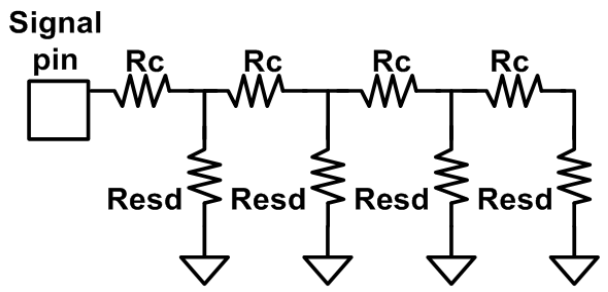


Figure 6: The resistive-ladder model of ES-DESD protection scheme during ESD stress.

III. Chip Implementation

To investigate ESD robustness and RF performance of the new proposed π-DESD protection scheme, the experimental test chip has been designed and fabricated in a 0.25-μm CMOS technology with 5 metal layers. The CPWG employed the top-metal layer (metal_5) as the signal line and the bottom-metal layer (metal_1) as the grounded shield. The thickness of the signal line and the height between the signal line and grounded shield are fixed by the given CMOS process parameters. Hence, the only way to adjust the characteristic impedance (Zo) of the CPWG is to change the width of the signal line and the spacing between the signal line and the coplanar ground line. The ES-DESD and π-DESD protection schemes with the total parasitic capacitance 200 fF of ESD diodes and the active VDD-to-VSS ESD clamp circuits have been implemented and shown in Figs. 7(a) and 7(b), respectively.

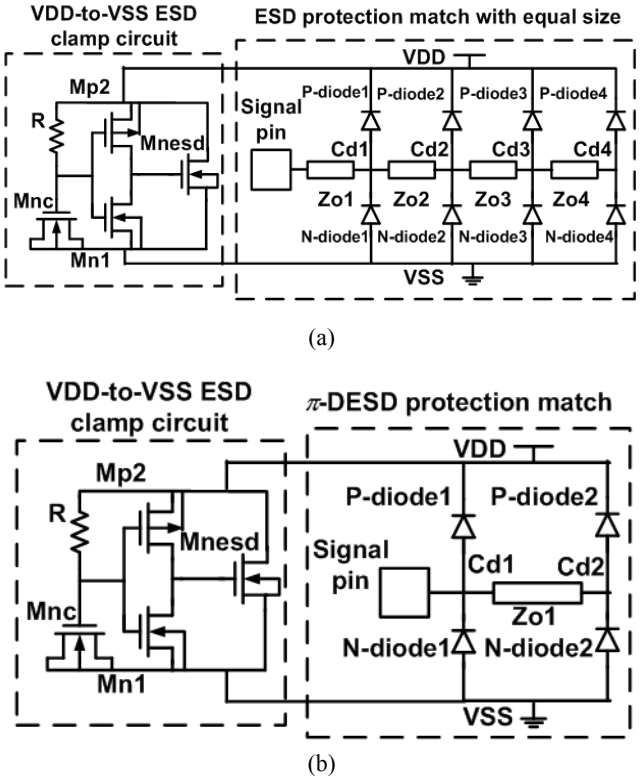


Figure 7: (a) The ES-DESD protection scheme, and (b) the new proposed π-DESD protection scheme, cooperating with the active power-rail ESD clamp circuit for RF signal pad.

The impedance of 70 Ω is chosen with the signal-line width of 5.5 μm and the spacing of 7.4 μm to save layout area and to make the resistive

ladder effect more obvious. Based on the fixed dielectric constant and process parameters, the length of CPWG to compensate the shunt capacitance from ESD diodes can be determined. The STI p-diodes and n-diodes are chosen to shunt the ESD stress to VDD and VSS, respectively. A single unit of p- or n-diode with the layout dimension of 5.5×1.2 μm^2 contributes a parasitic capacitance of ~25 fF in the given 0.25-μm CMOS process. To have a larger parasitic capacitance, more of the diode units are connected in parallel. The component parameters and the lengths of the CPWG used in the fabricated ESD protection circuits are listed in Table 1. The die photos of the ES-DESD protection circuit and the π-DESD protection circuit with the VDD-to-VSS ESD clamp circuit are shown in Figs. 8(a) and 8(b), respectively.

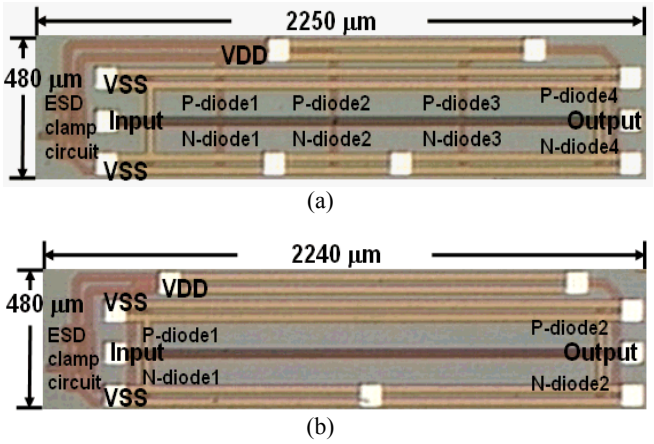


Figure 8: Die photos of (a) the ES-DESD protection circuit, and (b) the π-DESD protection circuit, with the active VDD-to-VSS ESD clamp circuit.

Table 1: The component parameters used in the fabricated ESD protection circuits.

Match type	ES-DESD	π-DESD
Cd1 (fF)	50	100
Cd2 (fF)	50	100
Cd3 (fF)	50	
Cd4 (fF)	50	
Zo1 (Ω)	70 (L=381 μm)	70 (L=1792 μm)
Zo2 (Ω)	70 (L=424 μm)	
Zo3 (Ω)	70 (L=482 μm)	
Zo4 (Ω)	70 (L=566 μm)	

IV. Experimental Results

The S parameters of these two ESD protection schemes have been measured on wafer with two-port G-S-G probes from 1 to 15 GHz. The 20-GHz S-parameter measurement system (HP85122A) is used to characterize the circuit behavior. The voltage supply of VDD (VSS) is 2.5 V (0 V), and the input DC bias is 1.0 V. The source and load resistances to the fabricated ESD protection circuits are kept at 50 Ω. The parasitic effects from the input and output pads have been de-embedded through the reference open pads to obtain the pure S parameters of the ESD protection circuits. The measured RF performances (S11 and S21) of the fabricated ES-DESD and π-DESD protection schemes in a 0.25-μm CMOS process are shown in Figs. 9(a) and 9(b), respectively.

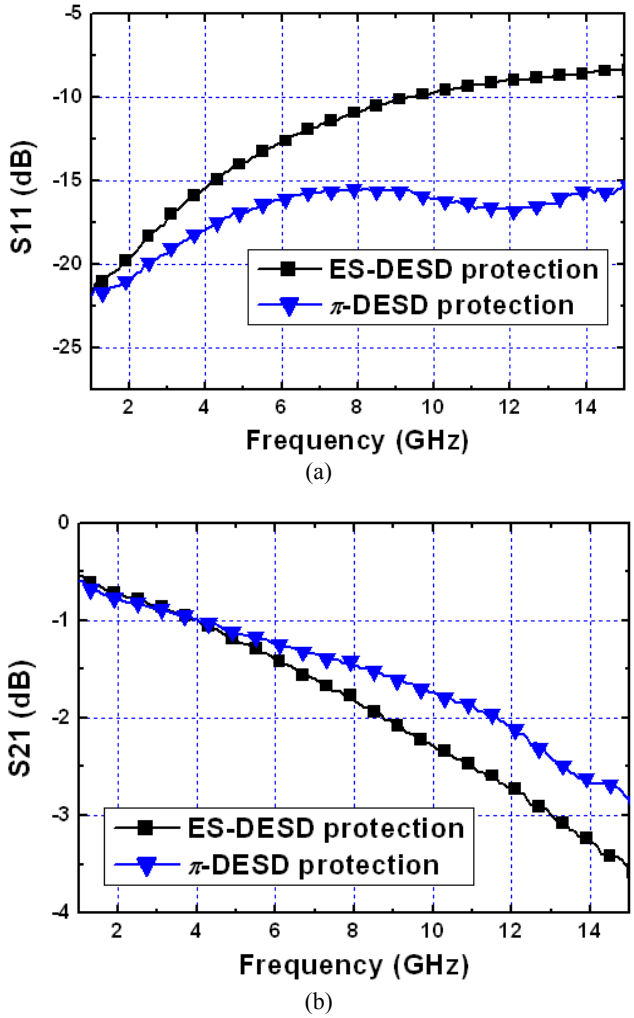


Figure 9: The measured results on (a) S11, and (b) S21, of the fabricated ES-DESD and π-DESD protection schemes.

Table 2: HBM ESD levels of the fabricated ESD protection circuits.

Match type	ES-DESD	π-DESD
ND-mode (kV)	5.5	> 8.0
PS-mode (kV)	5.5	> 8.0

The S11 of π-DESD protection scheme is much better than that of ES-DESD protection scheme over the frequency from 1 to 15 GHz. Besides, the S21 of π-DESD protection scheme is also better than that of ES-DESD protection scheme when the frequency up to 10 GHz, which results from the better impedance match in the π-DESD protection scheme. The CPWG used in the ES-DESD protection scheme with a longer total length will also cause larger signal loss to degrade its RF power gain (S21). According to the experimental results in Fig. 9, the π-DESD protection scheme indeed achieves a better broadband RF performance than that of the ES-DESD protection scheme.

The human-body-model (HBM) ESD test results of the fabricated ES-DESD and π-DESD protection schemes, under the failure criterion of 30% I-V curve shifting at 1-μA current, are summarized in Table 2, which includes the negative-to-VDD (ND-mode) and positive-to-VSS (PS-mode) ESD stresses. Typically, the ND- and PS-modes of ESD stresses are the weakest modes in ESD protection circuit for the I/O pin with diodes as ESD protection devices. The typical shifting I-V curves of the fabricated ESD protection schemes before and after the ESD stresses are shown in Figs. 10(a) and 10(b), under the PS-mode and ND-mode ESD stress, respectively. With the well experience on ESD failure analysis, the curve shifting in Fig. 10 can be judged from the junction leakage on the ESD protection diodes.

The Mnesd in the active VDD-to-VSS ESD clamp circuit for both ES-DESD and π-DESD protection schemes is realized with the same device dimension (W/L) of 520μm/0.35μm in the test chip. The ES-DESD protection scheme can sustain the HBM ESD level of 5.5kV, but that of π-DESD protection scheme can be improved up to >8kV, with the help of active VDD-to-VSS ESD clamp circuit. Without the VDD-to-VSS ESD clamp circuit, both of these two ESD protection schemes have a very low ESD level (~0.6kV). This has also verified the effectiveness of the active VDD-to-VSS ESD clamp circuit to improve ESD robustness of RF circuits, which are protected by the diodes with small device sizes to reduce the parasitic effect on RF signals. Comparing the HBM ESD levels in Table 2, the new proposed π-DESD protection scheme actually provides better ESD levels in both ND- and PS-modes ESD stresses than those of the ES-DESD protection scheme.

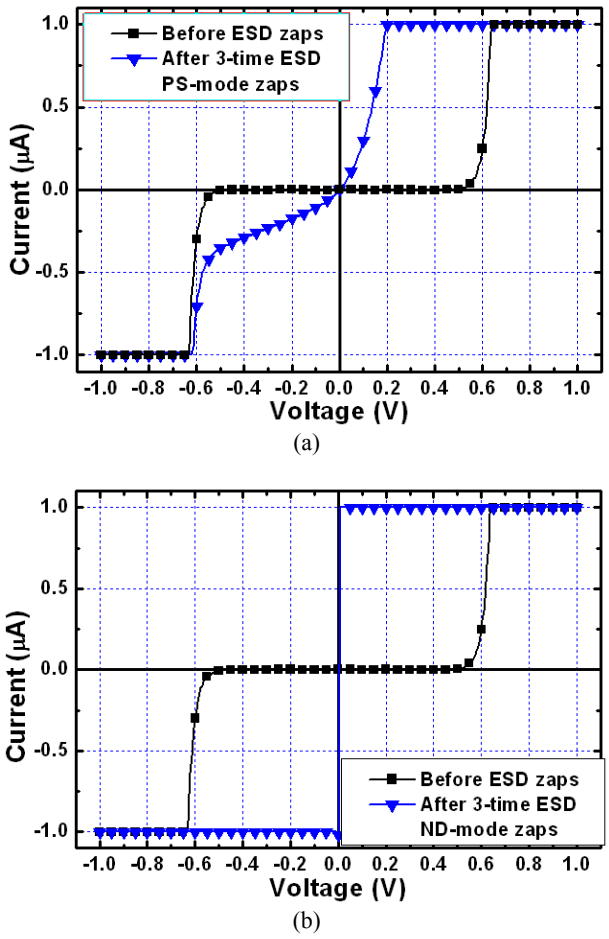
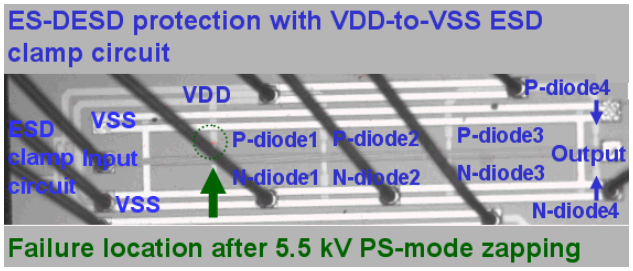


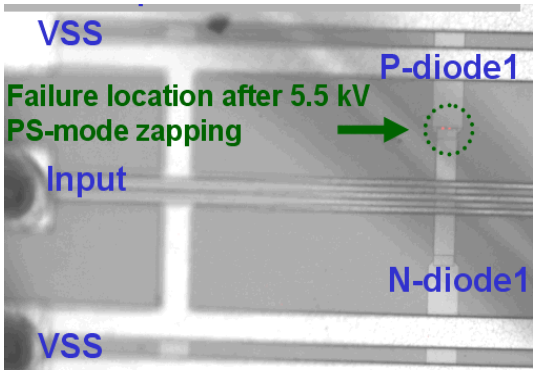
Figure 10: I-V curves of the input diodes before and after ESD stress. The curves are measured with both VDD and VSS relatively grounded to verify ESD failure on the ESD diodes. (a) Under the positive-to-VSS (PS-mode) ESD stress, and (b) under the negative-to-VDD (ND-mode) ESD stress.

In order to make sure that the ESD result is consistent with the principle of the resistive-ladder model in Fig. 6, the failed circuits after ESD stresses have been de-layered to find the failure location. The EMMI (photon emission microscope) pictures on the ES-DESD protection circuit with VDD-to-VSS ESD clamp circuit after 5.5-kV PS-mode ESD stress are shown in Fig. 11(a) with the whole view, and in Fig. 11(b) with the zoomed-in location on the damaged site. The EMMI pictures have confirmed that the ESD damage (indicated by the arrow) is located on

the p-diode junction of the first ESD stage with a shining area after the PS-mode ESD stress. The evidence in Fig. 11 has proved that the concept of the resistive-ladder model is correct. The first ESD stage is the weakest location of ESD protection along the ES-DESD ESD protection scheme. Hence, the new proposed π-DESD ESD protection scheme with a relatively larger diode size in the first ESD stage (but kept the same total capacitance of all ESD diodes) can actually achieve a better ESD robustness that that of ES-DESD ESD protection scheme.



(a)



(b)

Figure 11: The EMMI pictures to show the location of ESD damages in the ES-DESD protection circuit with the active VDD-to-VSS ESD clamp circuit after the HBM 5.5-kV PS-mode ESD stress. (a) The whole view of the ES-DESD circuit. (b) The zoomed-in view of the damaged location on the p-diode at the first ESD stage.

V. Conclusion

A new π-model distributed ESD protection scheme with better broadband RF performance and great ESD level have been proposed and verified in a 0.25-μm CMOS process. Comparing to the equal-size distributed ESD protection scheme, the new proposed π-model distributed ESD protection scheme has presented better co-design results on both RF impedance match and ESD protection. With the help of active VDD-to-VSS ESD clamp circuit, the device sizes of ESD protection diodes in the RF input pin can be further reduced to decrease the parasitic capacitance from ESD devices for achieving better RF circuit performance in the higher frequency band. Hence, this new broadband ESD protection scheme is more useful for ESD design in broadband RF systems.

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