Latchup Test-Induced Failure within ESD Protection Diodes in a High-Voltage CMOS IC Product

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Abstract – An EOS-like latchup failure occurred in a high-voltage IC product during latchup test and was identified within ESD diodes themselves. A parasitic npn bipolar formed by ESD protection diodes was trigger-activated and produced large current to result in EOS failure. This was verified by electrical measurement from TLP and curve-tracer as well as physical failure analysis. Corresponding layout solutions were proposed and solved this anomalous latchup failure successfully. Therefore ESD protection diode should be laid carefully for true latchup-robust design.

I. Introduction

Diode structure has been extensively adopted as protection against ESD stress for a long time, and is a major branch among elementary ESD protection devices. Diodes possess excellent forward characteristics as high forward breakdown current (around 50mA/um) [1] and low Ron. On the other hand, their reverse-bias application is much disqualified for ESD protection use as their early failure at small reverse current and causing other devices to breakdown earlier below diode avalanche voltage [2]. Therefore, for 1.5um process and below, primary ESD protection structure has evolved into relying heavily on parasitic bipolar structures like MOS and field-oxide devices exploiting their snapback characteristics.

With gradually demanding area and RC-delay restriction for I/O pad protection, continual use of parasitic bipolar devices is is limited. Diodes, when aided by efficient Vdd-Vss power clamp circuits, can now utilize their exceptional forward-conduction characteristic to full extent without having to operate in reverse breakdown region [3][4]. Thus, they provide solution to above- mentioned ESD protection issues and have regained favor as whole-chip ESD design complexity increases. Another unparalleled advantage with diode protection is that unlike parasitic bipolar structure in which SCR structure can be formed between pull-up and pull-down ESD protection devices, diodes are generally considered latchup-free [5] because there are no nodes to form SCR-like regenerative loop.

However, general belief that ESD diodes are not prone to failure during latchup test was proved incorrect with this study. In this paper we report an EOS-like failure occurred during latchup testing. From a series of failure analyses, the anomalous latchup failure was confirmed to be within ESD protection diodes themselves. Later we perceived there was parasitic bipolar triggered by latchup injection current to achieve forward active state, and large collector current during bipolar activation resulted in metal electrical overstess (EOS) issues. Transmission-line pulsing (TLP) and curve-tracer measurement obtained holding voltage of this parasitic bipolar to be smaller than maximum operating voltage and therefore was capable to turn on given suitable trigger condition. Removing this parasitic bipolar path eliminated this latchup failure and thus justified the veracity of our study. Last, relationship between failure threshold and applied voltage was also explored.

II. Failure Characterization and Possible Failure Mechanisms

This product is a dual-power (Vddd=3.3V, Vdda=9V), high voltage IC with 9V as maximum operating voltage. I/O ESD protection is comprised of P+/N-well pull-up and N+/P-sub pull-down diodes. Complete ESD protection scheme is achieved combining gate-triggered high-voltage PMOS (HVPMOS) as ESD power clamp circuit for whole-chip ESD protection as shown in Fig. 1. In addition, N+/P-sub power-ground diode exists for each power pin. The product qualified 3kV HBM ESD and +/-100mA current trigger test as JEDEC Standard No.78 Latchup Test.

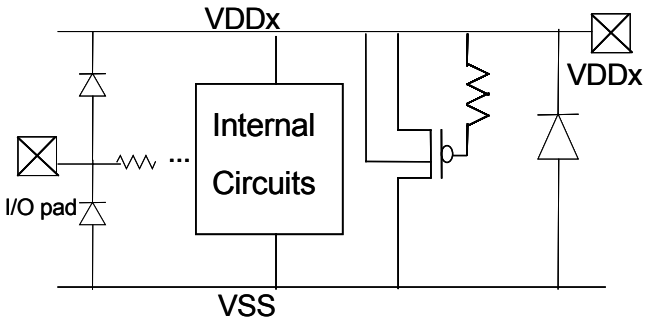


Figure 1: Circuit schema of product-level ESD protection schemes. Diodes form I/O and power pin ESD protection while gate-resistor PMOSs form power clamping devices.

With subsequent marginal latchup test, failure was noticed to occur at –150mA trigger test with large latchup current occurring at 9V power (Vdda) with magnitude that varied from 200 to 500mA and post-trigger Vdda standby leakage increasing from sub-mA to several milliamps. Pin group test was given and discovered negative trigger test on a high-voltage pin next to Vdda (referred to as pin A throughout this paper) resulted in latchup failure. It's worth mentioning that of all 10 layout-identical pins, only pin A caused failure. Table I recorded average Vdda power pin current (Idda) during subsequent wafer-level negative trigger test on pin A for both non-epi and 7um-epi wafers.

Since latchup failure was mostly induced by parasitic SCR turn-on due to substrate current triggering from I/O injection, layout review was first performed to observe relationship between injector (pull-down diode of pin A in this case) and most suspicious latchup path. As a result, there was no parasitic SCR path present for at least within 300um range of pin A's pull-down diodes. Optical microscope (OM) inspection of failed sample was performed and revealed burnt mark indicating metal explosion at power-ground diode of Vdda as shown in Fig. 2. To author's knowledge, most latchup failure in high-voltage product would be metal fusing at the path where latchup event occurs. This is because of relatively long overstress time [2] during latchup event and high power dissipation of high-voltage devices resulted in aluminum melting due to its relatively low melting point. But diode would not form SCR and also latchup path in itself. Therefore it is hard to explain metal fusing at Vdda power-ground diode.

Table I: Average Idda vs. injection current level of pin A

Neg. injection current level from pin A (mA)	-100	-120	-140	-400
Non-epi wafer	16.1	18.3	21.2	N/A*
7um-epi wafer	10.2	11.1	12	36.2

*: Latchup failure occurred before Idda can be recorded

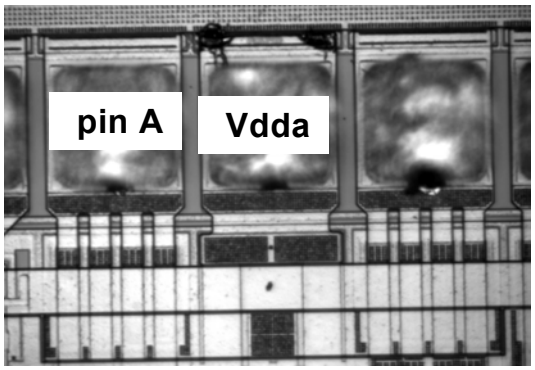


Figure 2: Optical microscope inspection on latchup-failed sample. Clear burn mark at Vdda power-ground diode was observed.

Emission Microscopy (EMMI) was performed subsequently for further analysis. Hot spot caught during pin A trigger and Vdda latchup event was right at Vdda power-ground diode as shown in Fig. 3, same as seen on OM. This meant that large latchup current not only existed at Vdda power, but also concentrated at its power-ground diode which explained metal fusing from OM inspection.

Two possible failure mechanisms could be inferred from Table I and Fig. 3. The first involved parasitic guard band formed by N+ cathode of Vdda power-ground diode since it was connected to high voltage. This node acted as minority carrier guard band for injected electrons from pin A. If the metal width or number of contacts of this parasitic guard band was not large enough, current densities formed by the collected injected carriers might be high enough to

cause contact spiking or metal melting of this diode. After reviewing layout, damage at contact or metal was not likely as its size and number of contacts were considered. Furthermore, higher current-bearing capabilities at Vdda (see Table I) of 7um-epi samples without damaging this diode could not be explained with this speculation. Also, it couldn't explain the change in Idda in which large current (200~500mA) occurred first during latchup event and receded to small leakage current after second power-up. Occurrence of contact spiking was independent with substrate type and corresponding induced leakage should be invariant with time.

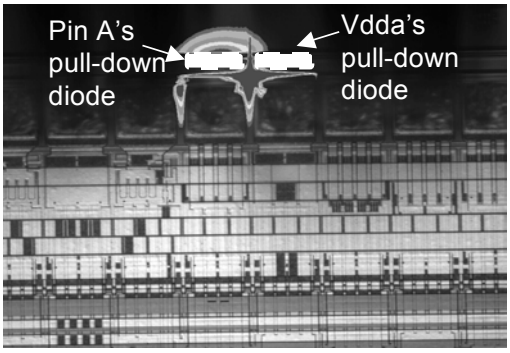


Figure 3: EMMI hot spot during negative trigger of pin A and subsequent latchup-test failure event.

In subsequent wafer-level latchup test we observed change of Vdda power-ground diode in accordance with negative triggering pin A. In our observation, diode explosion always accompanied with large latchup-like current surge at Vdda beyond certain current trigger threshold, implying latent device turn-on event. Therefore, the second hypothesis involved parasitic device activation with aid of trigger from pin A. Since no parasitic SCR was involved with Vdda power-ground diode layout, regeneration of SCR path was not possible. According to EMMI hot spot inspection, a parasitic npn bipolar could be identified between pin A's power-ground diode(N) /P+ Vss pickup(P)/ Vdda's power-ground diode(N) as shown in Fig. 4. In this paper, we used BV_{CEB} to define collector-emitter breakdown voltage with specific base bias. Under normal operation this parasitic npn remained cutoff. However, during negative latchup test of pin A the emitter-base junction was forward biased and the parasitic bipolar operated in forward-active region. With further injection from emitter and increase in base current this parasitic bipolar might finally reach self-biased condition [1]. If the collector voltage, BV_{CEB}, under such condition was smaller than Vdda, large collector current would be produced once the device was triggered into self-biased region This is because Vdda was fixed at 9V by a power supply. EOS-like failure would occur to metal or contacts due to second-scale of stress time in latchup test. With this hypothesis, not only sudden surge of Idda during pin A trigger test and subsequent power-up Idda leakage can be explained, but also different LU testing results between non- and 7um-epi wafers due to degraded bipolar characteristics with epi wafers. Sudden surge of Idda during "latchup event" was actually the exhibition of large collector current beyond holding point.

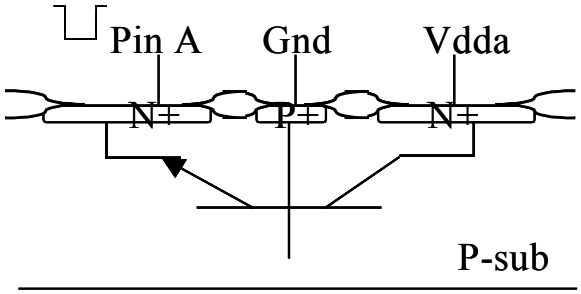


Figure 4: Cross-sectional diagram illustrating the parasitic npn bipolar formed by pin A's pull-down diode, P+ pickup, and Vdda power-ground diode.

III. Experiments and Electrical Measurements

In order to jusify the veracity of our hypothesis, we used Focused Ion Beam (FIB) to remove the Vdda power-ground diode as well as the collector of this parasitic npn bipolar. The sample was then latchup tested again. Injection level of pin A could now be raised up dramatically to larger than -400mA without any failure. Another FIB cross-sectional view on failed sample, as shown in Fig. 5, revealed metal melting at both collector and base nodes, validating bipolar activation assumption that almost all power in high current operating mode was generated within collector-base region [1]. From above FIB experiments the activation of parasitic bipolar leading to anomalous latchup failure was confirmed.

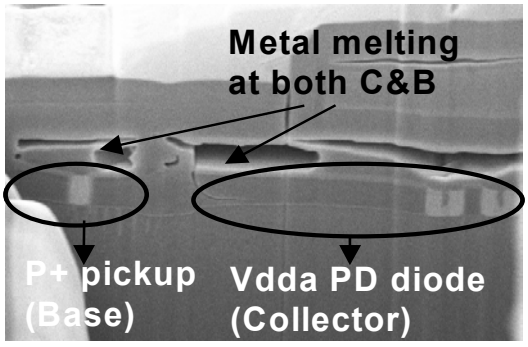
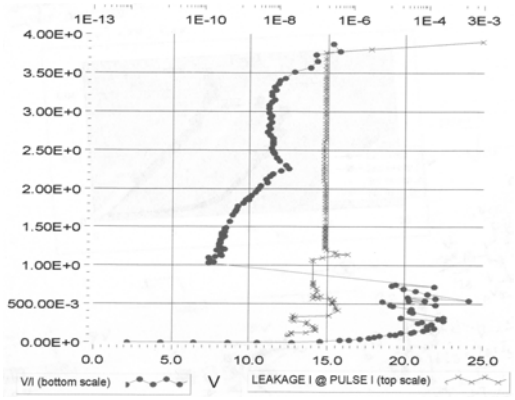
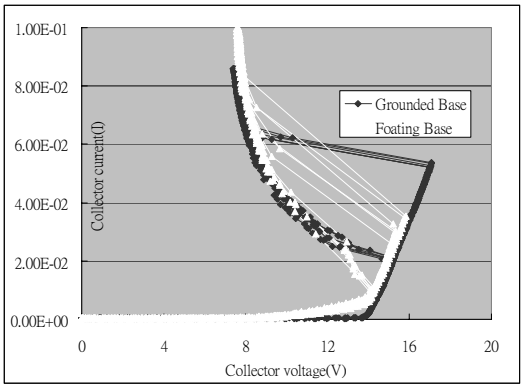


Figure 5: FIB cross section of the parasitic npn bipolar damaged by latchup testing. Metal melting above collector and base was observed.

In order to further determine the possibility of the parasitic bipolar to reach and retain holding state, relationship between holding voltage (V_{hold}) and power supply voltage (V_{power}) need to be explored. If V_{hold} is larger than maximum operating voltage V_{power}, there's no permissible condition for bipolar activation and self-biased operation to occur. Therefore BV_{CEB} of this parasitic npn at self-biased region was measured. The measurement was carried out with Transmission Line Pulsing (TLP) and Tektronix 370A curve tracer as shown in Fig. 6(a) and 6(b). Both measurements led to similar BV_{CEB} around 7.5V which was significantly smaller than Vdda, implying self-biased operation did exist if accompanied with sufficient trigger conditions.



(a)



(b)

Figure 6: I-V curves of parasitic npn bipolar measured with (a) TLP and (b) curve tracer. Both led to similar BV_{CEB}.

In another electrical test, a 30-ohm of series resistor was also added between Vdda pad and 9V power supply as a "voltage limiter". The purpose is to limit pad voltage and verify the integrity of Vdda's power-ground diode for reduced V_{power} condition and the result was also drastic improvement in pin A's trigger level. With increased injection as can be seen on Table II, Vdda nodal voltage actually decreased and therefore the activation of this parasitic npn was prohibited with existence of the series resistor.

From experiments and measurements performed above, the parasitic npn activation formed by ESD diode was confirmed to be failure origin of EOS-like latchup failure.

Table II. Nodal voltage of Vdda vs. Pin A's injection levels

Injection Level (mA)	-200	-300	-400	-600
Idda(mA)	20.4	28.2	36.2	47
Nodal voltage of Vdda (V)	8.3	8	7.8	7.5

IV. Results and Discussion

In order to eliminate this latchup-test failure while retaining same ESD protection, bipolar-gain spoiling and decoupling method should be applied. This could be achieved by splitting P+ pickup ring of this parasitic npn bipolar into two and separating them with field oxide, as shown in Fig. 7. It should be noted particularly that though adding guard rings were frequently used in bipolar decoupling and spoiling, adding N+ guard ring would not improve but only aggravate this type of failure because another collector was introduced. Therefore, adding only P+ guard ring connected to ground was allowed. Another method was to replace the Vdda power-ground diode with PMOS power clamp structure in which no significant snapback behavior was observed. This further improved ESD robustness between power and ground in both polarities. Both methods were proved to completely resolve the problem in subsequent revision.

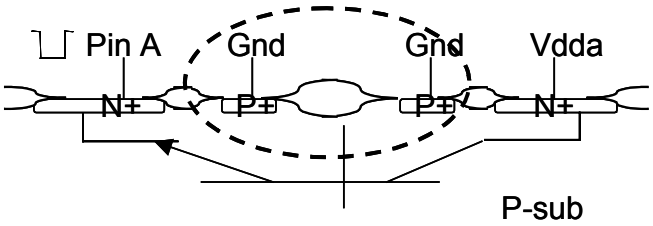


Figure 7: Cross section of modified diode structure. Original P+ pickup was splitted into two and seperated with field oxide (dashed circle).

In chip-level ESD reliability, layout consideration is important because ultimate ESD robustness is highly affected by existence of parasitic devices [6]. Specific rules must be followed during layout phase in order to avoid unexpected ESD failure. The same issue also applies regarding latchup reliability with more and

more failure mechanisms involving parasitic devices in recent years [7][8].

The anomalous latchup-testing failure at ESD protection diode and parasitic bipolar action in this case stemmed from elevated operating voltage, further enabled by current injection in latchup test. An ordinary logic IC product has operating voltage below 5V and I/O ESD devices are usually well guarded by double guard rings. Therefore BV_{CEB} of parasitic bipolars are substantially larger than maximum operating voltage and parasitic device-induced latchup failure is not likely to occur. With increasing operating voltage in high-voltage application, however, these latent latchup-test failures might become more prevalent. Hence, as operating voltage is elevated, persistant and careful examination on product layout is required to aviod forming of parasitic bipolar structures that can become active and reach self-biased operation under certain trigger conditions. This mechanism is especially important if signal latchup is to be considered alongside of JEDEC No.78 Standard [8]. In another similar product with higher operating voltage, we faced latchup-test failure in high-voltage input pins with much lower failure threshold (less than -50mA). The failure symptum and mechanism after physical analysis revealed same as parasitic npn bipolar activation. In short, this type of failure was not restricted to power pins but applicable to all high-voltage nodes.

ESD protection device layouts near pad region often share same pickup (as ESD diodes in this study) with adjacent pins in order to save I/O layout area. This introduced parasitic bipolars and failure hazards during latchup test. Therefore relation between BV_{CEB} of parasitic devices and pickup or guard ring layout should first be exploited during process development stage. Making corresponding BV_{CEB} higher than V_{power} should be taken as an additional consideration in determining proper pickup ring width in ESD layout rules. This is especially important in high-voltage applications.

As stated above, in another similar product with higher operating voltage a much lower failure threshold was observed. Based on this observation, testkey with npn parasitic device was designed to explore dependency of injection current threshold with collector voltage at failure events. The measured result was shown in Table III. Drastic drop in failure current threshold with collector voltage larger than 16V was observed. This suggested although failure threshold was expected to lower with elevated collector voltage, severe degradation occurred only above certain voltage levels. This trend is consistent with previous conclusion that turning on and self-biased operation of parasitic npn bipolar is possible only when V_{power} is larger than BV_{CEB}.

Table III. Collector voltage (Vpower) vs. failure threshold of a npn test structure simulating anomalous latchup-test failure

Collector voltage (V)	13	14	15	16	17	18
Failure injection threshold (mA)	>-200	>-200	>-200	-40	-17	-13

Reviewing Fig. 5, damage in the form of metal melting was observed, different from common EOS failure symptoms as contact spiking and/or oxide rupture. This was due to long latchup stress time that resulted in isothermal condition where heat produced at collector-base junction could finally distribute evenly and cause aluminum to melt due to its lower melting point. In contrast, failure of contact spiking and metal melting were observed with high-current TLP test. This illustrated that metal melting was an EOS failure due to heat produced by parasitic bipolar in self-biased region operation. The device now acted like a voltage-controlled current source and high current would appear at collector since it was biased by power supply.

V. Conclusion

An EOS-like latchup failure within ESD diode was first proposed in this paper. The observed failure was in the form of metal melting in power pin ESD diode during negative trigger of an adjacent pin. Our experiments revealed that failure originated from activation of a parasitic npn bipolar device formed by power-ground diodes. This bipolar was turned on with emitter-base junction forward-biased in negative latchup current test. Because BV_{CEB} of this parasitic npn bipolar was smaller than operating voltage it could operate in self-biased region and result in high current if suitable trigger condition exists. TLP and curve-tracer measurement results provided further evidence. Both bipolar spoiling and removing this parasitic bipolar path resolved this anomalous latchup failure. From above results, implementation of suitable guard ring protection and considering parasitic bipolar path was necessary even with diodes. It was especially important with gradually prevailing high-voltage circuits and applications. Last, testkey measurement was given and abrupt degradation latchup trigger characteristic with increasing applied voltage was observed.

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