Design on Latchup-Free Power-Rail ESD Clamp Circuit in High-Voltage CMOS ICs

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Abstract - The holding voltage of the high-voltage ESD protection devices in snapback breakdown condition has been found to be much smaller than the power supply voltage. Such characteristics will cause the high-voltage CMOS ICs susceptible to the latchup-like danger in the real system applications, especially while these devices are used in the power-rail ESD clamp circuit. A new latchup-free design on the power-rail ESD clamp circuit with stacked-field-oxide structure is proposed and successfully verified in a 0.25-μm 40-V CMOS process to achieve the desired ESD level. The total holding voltage of the stacked-field-oxide structure in snapback breakdown condition can be larger than the power supply voltage. Therefore, latchup or latchup-like issues can be avoided by stacked-field-oxide structures for the IC applications with VDD of 40V.

I. Introduction

High-voltage transistors in smart power technologies have been extensively used for display driver ICs, power supplies, power management, and automotive electronics. The electrostatic discharge (ESD) reliability is an important issue for high-voltage transistors with applications in these products. In smart power technology, high-voltage MOSFET, silicon controlled rectifier (SCR) device, and bipolar junction transistors have been used as on-chip ESD protection devices [1]-[6]. The earlier publications focused on analyzing and improving ESD robustness of the ESD protection devices in high-voltage CMOS processes [1]-[6]. However, the latchup or latchup-like failure from such ESD protection devices under normal circuit operating condition was not considered in these earlier reports, especially while the devices are used in the power-rail ESD clamp circuit.

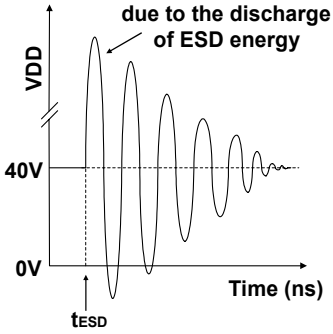
In general CMOS ICs, the VDD-to-VSS ESD clamp circuits across the power lines of CMOS ICs had been used to effectively increase ESD robustness of the chip [7]. When the ESD protection device is used in the power-rail ESD clamp circuit, the device is expected to be kept off in normal circuit operating condition. During ESD stress conditions, the ESD protection device should be triggered on to discharge ESD current. If the holding voltage of the ESD protection device in power-rail ESD clamp circuit is smaller than the power supply voltage, the ESD device may be triggered on by the system-level electromagnetic compatibility (EMC)/ESD transient pulses to cause a very serious "latchup" or "latchup-like" failure in CMOS ICs. This phenomenon often leads to IC function failure or even destruction by burning out [8], [9].

With the wide applications of high-voltage CMOS technology in the LCD driver ICs (typically, gate driver with 40V, and source driver with 12V, for 14.1-inch notebook LCD panel), the system-level EMC/ESD reliability has been requested up to 20kV of air-discharge ESD gun zapping. The system-level EMC/ESD test on LCD panel of notebook by an ESD gun (Standard IEC 61000-4-2 [10]) is shown in Fig. 1(a). During the system-level ESD test, the power lines of driver ICs in the LCD panel of notebook can be coupled with an overstress voltage even up to several hundred volts [11], as that shown in Fig. 1(b). Especially, the driver ICs with tape carrier package (TCP) are directly attached to the LCD panel. No room is available for the IC with on-board de-coupling discrete components to shunt the ESD-zapping transient voltage away from the driver ICs. So, the transient voltage seen by the circuits in the driver ICs is quite large during such system-level EMC/ESD zapping.

In this paper, the I-V characteristics of ESD protection devices fabricated in a 0.25-μm 40-V CMOS process under transmission line pulsing (TLP) stress are found to have a very low holding voltage. The susceptibility of the ESD protection devices to the noise transient or glitch on the power lines during

normal circuit operating condition are investigated by the transient latchup (TLU) test [12]. A new latchup-free design on the power-rail ESD clamp circuit with stacked-field-oxide structure is proposed and verified in a 0.25-μm 40-V CMOS process to achieve the desired ESD level.

(a)



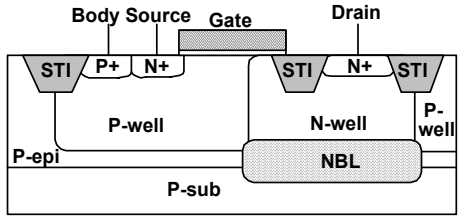
(b)

Figure 1: (a) The system-level EMC/ESD test on LCD panel of notebook by an ESD gun. (b) The transient overshooting/ undershooting voltage waveform on the VDD pin of the driver ICs during system-level EMC/ESD test.

II. High-Voltage ESD Protection Devices

A. TLP Characteristics

The lateral diffused MOS (LDMOS) device, SCR device, and field-oxide (FOD) device fabricated in a 0.25-μm 40-V CMOS process are studied in this work. The layout parameters of such ESD protection devices are drawn according to the foundry's ESD rules with the silicide-blocking mask. To investigate the turn-on behaviors of such ESD protection devices during high ESD current stress, transmission line pulse (TLP) generator with a pulse width of 100ns and a rise time of ~10ns is used to measure the snapback I-V curves of the devices [13]. The cross-sectional views and TLP-measured I-V characteristics of high-voltage gate-grounded nMOS (GGNMOS) device, SCR device, FOD device, and gate-VDD pMOS (GDPMOS) are shown in Fig. 2 - Fig. 5, respectively.



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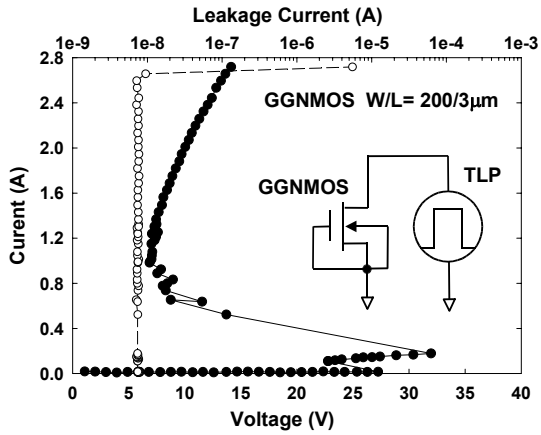
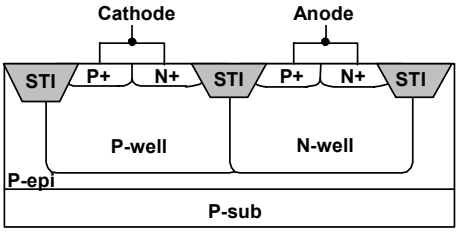


(b)

Figure 2: The (a) cross-sectional view, and (b) TLP-measured I-V characteristic, of high-voltage GGNMOS device fabricated in a 0.25-μm 40-V CMOS process.



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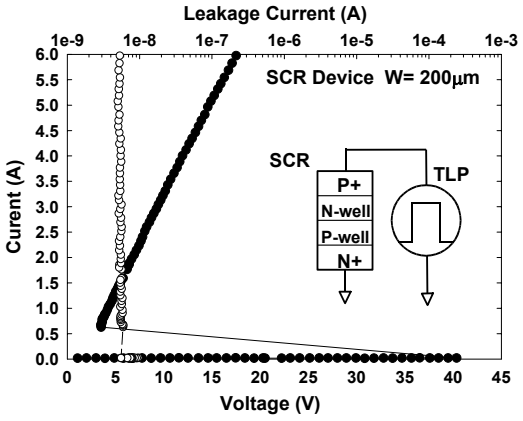
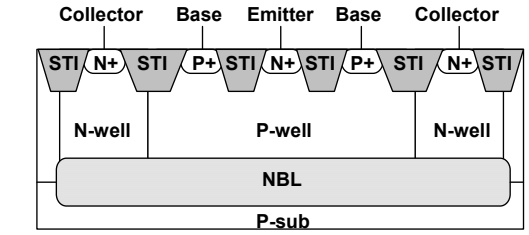
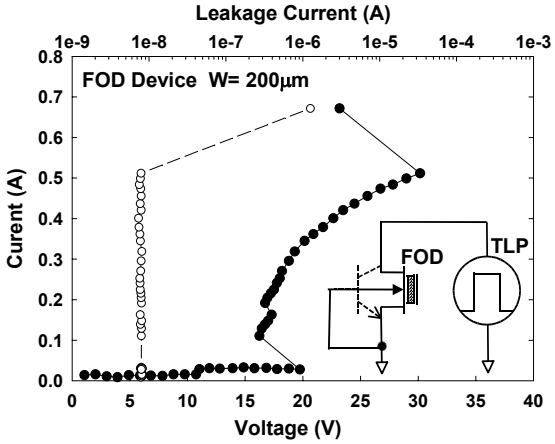


(b)

Figure 3: The (a) cross-sectional view, and (b) TLP-measured I-V characteristic, of high-voltage SCR device fabricated in a 0.25-μm 40-V CMOS process.

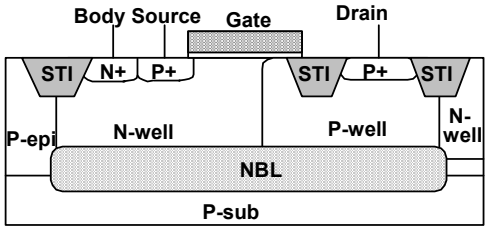


(a)



(b)

Figure 4: The (a) cross-sectional view, and (b) TLP-measured I-V characteristic, of high-voltage FOD device fabricated in a 0.25-μm 40-V CMOS process.



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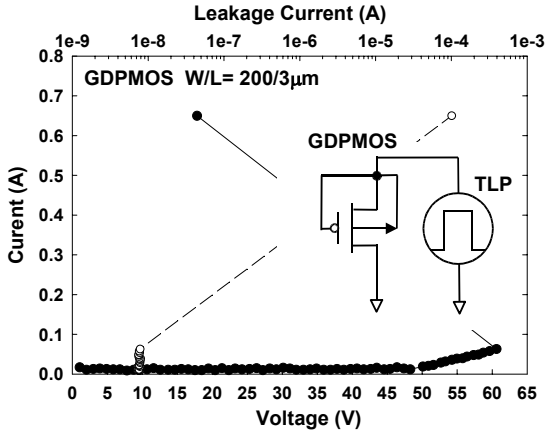


(b)

Figure 5: The (a) cross-sectional view, and (b) TLP-measured I-V characteristic, of high-voltage GDPMOS device fabricated in a 0.25-μm 40-V CMOS process.

For high-voltage GGNMOS device in Fig. 2(a), the double-snapback characteristic is found. As shown in Fig. 2(b), after the first snapback voltage at 27.2V (52V in DC), the device snaps back to 23V, from where the voltage strongly increases again. Then, the device goes into the second snapback, and the voltage drops to only ~7V. The turn-on resistance of the first snapback state is much larger than that of the second snapback state. The double-snapback characteristic of the GGNMOS device is related to turn-on behavior of the parasitic bipolar transistor and the occurrence of Kirk effect (base push-out effect) [5], [14]. The second breakdown current (It2) of GGNMOS device with 200-μm channel width is 2.7A. For high-voltage SCR device in Fig. 3(a), the characteristic of very low holding voltage and high ESD robustness is found. As shown in Fig. 3(b), the holding voltage of SCR device is only ~4V and the It2 current of SCR device with 200-μm width is over 6A. For high-voltage FOD device structure shown in Fig. 4(a), the device is isolated by the n+ buried layer (NBL) from the p-type substrate. The spacing from collector diffusion to emitter diffusion of FOD device is 6μm in this study. As shown in Fig. 4(b), the trigger voltage is 19.7V (50V in DC), and the holding voltage is ~16V. The It2 current of FOD device with 200-μm width is 0.5A. The difference on trigger voltage of the device measured by DC (HP4155) and TLP is caused by transient-coupling effect. The TLP is designed with a rise time of 10ns to simulate the HBM ESD event. The dV/dt transient voltage at the zapping node could be coupled into the device through the parasitic capacitance in the drain/bulk junction to lower the trigger voltage.

For high-voltage GDPMOS device in Fig. 5(a), no snapback characteristic is found, and therefore the holding voltage of the device is larger than the supply voltage of 40V. Due to the inefficient parasitic p-n-p bipolar gain, the It2 current of FOD device with 200-μm channel width is only 0.06A, as that shown in Fig. 5(b). Therefore, GDPMOS is not suitable for on-chip ESD protection device in high-voltage CMOS ICs due to too low ESD robustness.

B. Transient Latchup Test

Transient latchup (TLU) test is used to investigate the susceptibility of the ESD protection devices to the noise transient or glitch on the power lines during normal circuit operating condition. The measurement setup for TLU test is shown in Fig. 6. The positive or negative charging voltage (Vcharge) on the energy storage capacitor (C1) generating the transient is used to trigger the device into the latch state [12]. A supply voltage of 40V was used and the trigger source was

connected directly to the device-under-test (DUT). The small resistance (R1) is used to protect the DUT, when the DUT is triggered on into the latch state. In addition, the diode (D1) is used to avoid the damage to the power supply during TLU test. The voltage waveform on the DUT (at Y node) under TLU test is monitored in this experiment. The measured voltage waveforms on high-voltage GGNMOS device, SCR device, and FOD device under TLU test are shown in Fig. 7 - Fig. 9, respectively.

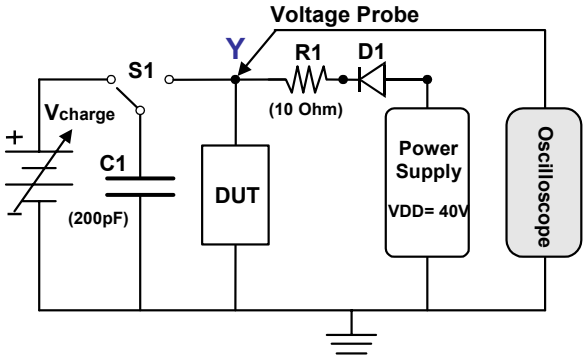


Figure 6: The measurement setup for transient latchup (TLU) test.

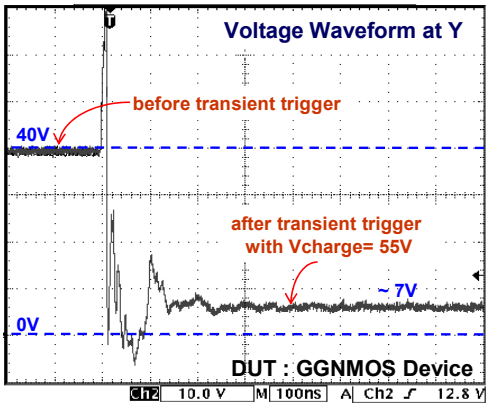


Figure 7: The measured voltage waveform on the high-voltage GGNMOS device under TLU test.

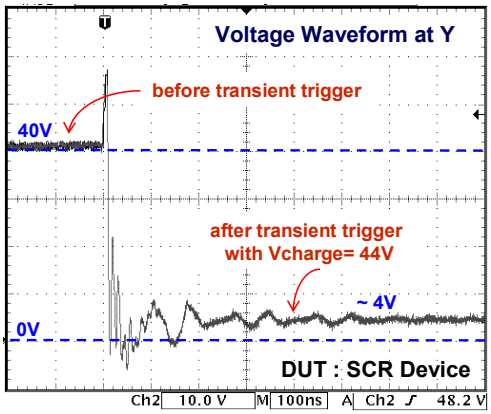
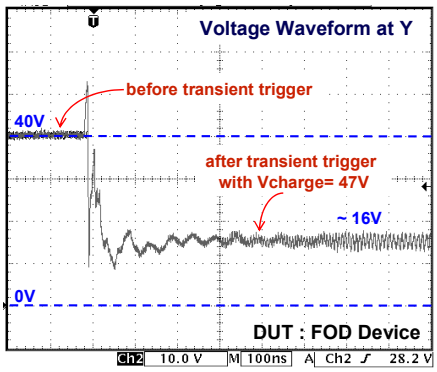


Figure 8: The measured voltage waveform on the high-voltage SCR device under TLU test.



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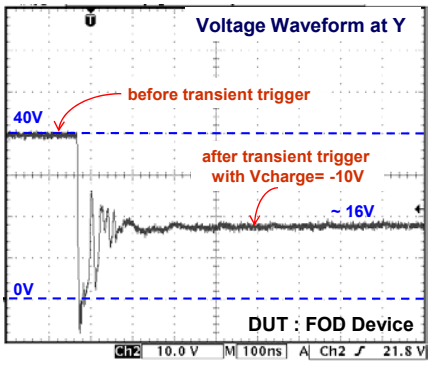


(b)

Figure 9: The measured voltage waveforms on the high-voltage FOD device under TLU test with (a) positive charging voltage, and (b) negative charging voltage.

From the measured results, the devices are initially kept off before the transient trigger, therefore the voltage waveforms are kept at 40V. After the transient trigger, the snapback characteristic in the device can be triggered on to generate a low-holding-voltage state. The clamped voltage level of the devices in snapback breakdown condition is consistent with the holding voltage measured by TLP stress. In Fig. 7, the clamped voltage level of high-voltage GGNMOS device is ~7V due to the transient triggering with the capacitor charging voltage of 55V. The GGNMOS device is triggered on into the second snapback state directly by the transient pulse. Although high-voltage nMOSFET has been widely used as the common ESD protection device in the high-voltage CMOS ICs, the latchup-like issue between the power rails will occur, when the high-voltage nMOSFET is triggered by the noise transient on the power lines. In Fig. 8, the clamped voltage level of high-voltage SCR device is only ~4V due to the transient triggering with the capacitor charging voltage of only 44V. Although SCR device has the advantage of high ESD robustness, the latchup issue in high-voltage CMOS ICs becomes worst. Figs. 9(a) and (b) show the measured voltage waveforms of high-voltage FOD device under TLU test with positive and negative

charging voltages, respectively. Both positive and negative charging voltages can trigger the FOD device into the latch state. The clamped voltage level of FOD device is ~16V due to the transient triggering with the capacitor charging voltage of 47V or -10V. For negative charging voltage, the parasitic diode between the power-rail may be turned on initially and then turned off quickly due to the transient of supply voltage. Finally, the FOD device is triggered into the holding state. Latchup-like issue is the concern by using single FOD device as the power-rail ESD clamp in high-voltage CMOS ICs.

From the power dissipation view, the device with a lower holding voltage is helpful to sustain much higher ESD current. However, the device may be triggered on by the noise transient or glitch on the power lines during normal circuit operating condition, especially under the system-level EMC/ESD zapping test. Because the holding voltages of high-voltage ESD protection devices are much smaller than the power supply voltage, such characteristics will cause the high-voltage CMOS ICs to be susceptible to the latchup or latchup-like danger in the real-system applications, which often have high noise or transient glitch issues.

III. Design of Latchup-Free Power-Rail ESD Clamp Circuits

The NMOS and SCR devices have higher It2 than that of FOD device, but their holding voltages (~7V in NMOS, ~4V in SCR) are far away from the 40-V operating voltage level. Such ESD protection devices with low holding voltage in power-rail ESD clamp circuits will cause serious latchup failure to high-voltage CMOS ICs. To overcome the latchup or latchup-like issue between the power rails in high-voltage CMOS ICs, a new stacked-field-oxide structure has been designed to increase the total holding voltage in snapback breakdown condition. The stacked-field-oxide structure with two cascaded FOD devices has been verified in a 0.25-μm 40-V CMOS process. The I-V characteristic and ESD robustness of stacked-field-oxide structure has been investigated by the TLP stress. The susceptibility of stacked-field-oxide structure to the noise transient during normal circuit operating condition has also been performed by the TLU test. Finally, a latchup-free power-rail ESD clamp circuit with stacked-field-oxide structure is proposed and verified.

A. TLP Characteristics

The measurement setup of single FOD device and stacked-field-oxide structure under TLP stress is shown in Fig. 10(a). The TLP-measured I-V characteristics of these devices with different device widths are compared in Fig. 10(b). From the measured results, the holding voltage of stacked-field-oxide structure in snapback breakdown condition is double of that of single FOD device. Therefore, the holding voltage of stacked-field-oxide structure can be linearly increased by increasing the numbers of cascaded FOD devices. The It2 currents of single FOD device and stacked-field-oxide structure as a function of device channel width are compared in Fig. 11. The It2 current of stacked-field-oxide structure is linearly increased while the device channel width increases. In addition, the It2 current of stacked-field-oxide structure is only slightly degraded as compared with that of single FOD device. The relation between the It2 and HBM ESD level, V_{ESD}, can be approximated as

$$V_{ESD} \cong (1500 + R_{ON}) \times It2, \quad (1)$$

where R_{ON} is the dynamic turn-on resistance of the device under test. From Fig. 11, the stacked-field-oxide structure with ~650μm for each FOD device width can sustain typical 2-kV (It2= ~1.33A) HBM ESD stress. Therefore, the required ESD specification of stacked-field-oxide structure can be achieved by adjusting the device width.

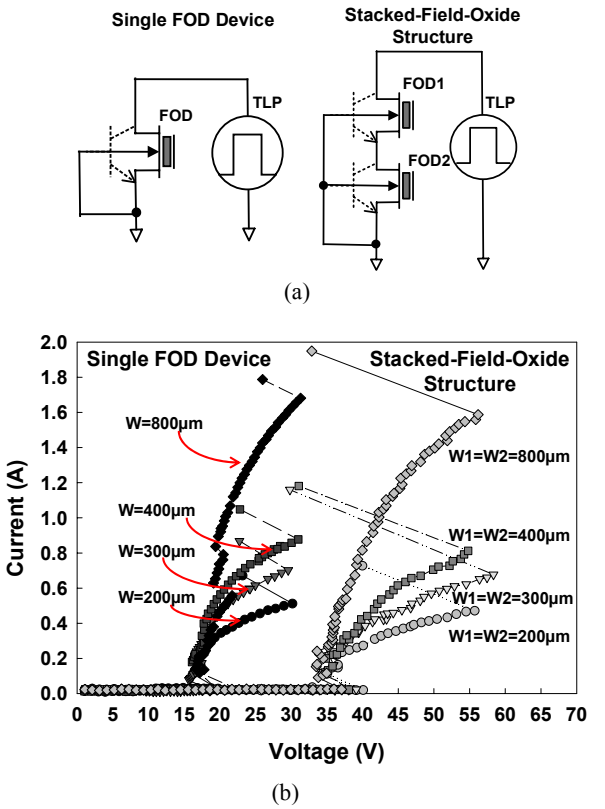


Figure 10: (a) The measurement setup of single FOD device and stacked-field-oxide structure under TLP stress. (b) The TLP-measured I-V characteristics of these devices with different device widths.

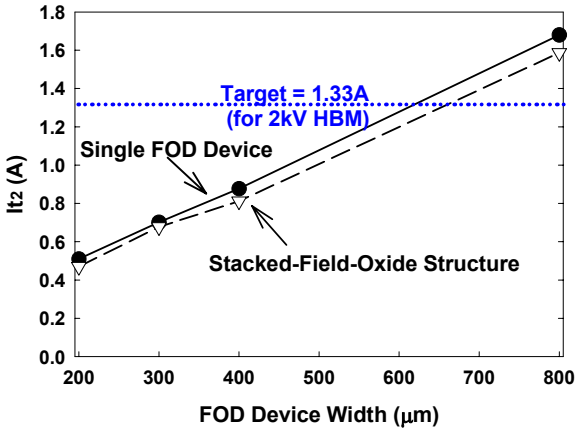


Figure 11: It2 currents of single FOD device and stacked-field-oxide structure as a function of device channel width.

The trigger voltage of stacked-field-oxide structure is increased as compared with that of single FOD device. The substrate-triggered technique can be applied to lower the trigger voltage of the device to ensure effective ESD protection [15]-[17]. The TLP-measured I-V curves of the stacked-field-oxide structure with different substrate-triggered currents (Itrig) are shown in Fig. 12. From the measured results, the trigger voltage of the stacked-field-oxide structure is decreased while the substrate-triggered current is increased. The trigger voltage can be reduced to only 17V when the substrate-triggered current is 10mA. Therefore, the trigger voltage of stacked-field-oxide structure can be effectively reduced lower than that of internal circuits by substrate-triggered technique. Moreover, the It2 level of the stacked-field-oxide structure with substrate-triggered current can be improved.

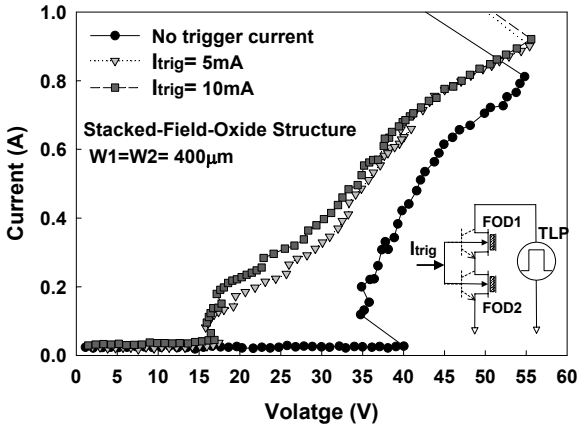
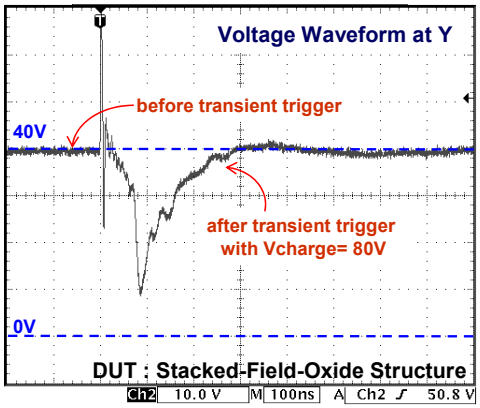


Figure 12: The TLP-measured I-V curves of the stacked-field-oxide structure with different substrate-triggered currents.

B. Transient Latchup Test

The measured voltage waveforms of stacked-field-oxide structure under TLU test with the transient triggering of positive and negative charging voltages are shown in Figs. 13(a) and (b), respectively. From the observed voltage waveforms, the stacked-field-oxide structure is triggered on due to the transient triggering with the capacitor charging voltages of 80V or -50V. But, the clamped voltage waveform quickly comes back to the original supply voltage level of 40V, without keeping in the latch state. The measured result is consistent with TLP-measured I-V curves, as those shown in Fig. 10(b). The total holding voltage of stacked-field-oxide structure with two cascaded FOD devices is near the supply voltage of 40V. After the stacked-field-oxide structure is triggered on during the TLU test, the clamped voltage level can quickly restore to the supply voltage. Therefore, no latchup or latchup-like issue is occurred. In addition, a higher capacitor charging voltage is needed to trigger on the stacked-field-oxide structure during the TLU test. Therefore, the latchup immunity of stacked-field-oxide structure to the noise transient on the power lines in high-voltage CMOS ICs has been significantly increased.



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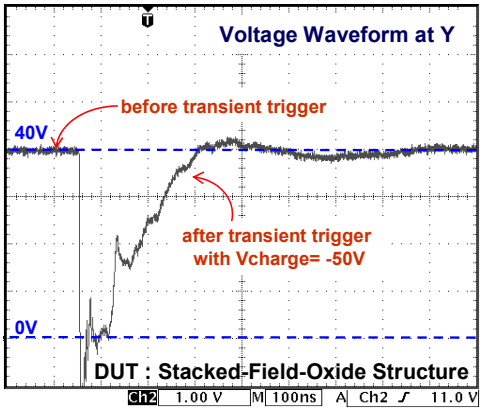
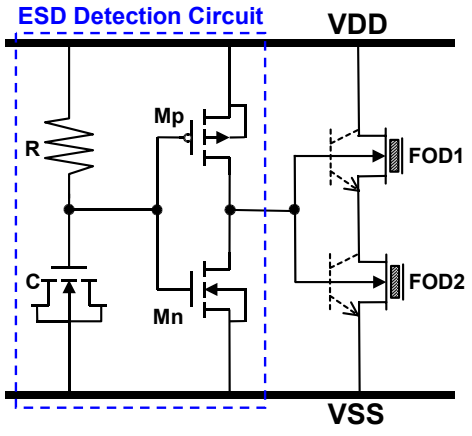


(b)

Figure 13: The measured voltage waveforms on the stacked-field-oxide structure under TLU test with (a) positive charging voltage, and (b) negative charging voltage.

C. Latchup-Free Power-Rail ESD Clamp Circuits

The proposed power-rail ESD clamp circuits with two cascaded FOD devices and three cascaded FOD devices in high-voltage CMOS ICs are shown in Figs. 14(a) and (b), respectively. The substrate-triggered technique is achieved by the RC-based ESD detection circuit [15]. The turn-on voltage of stacked FOD devices can be decreased to fast discharge the ESD current during ESD stress by the substrate-triggered technique. The latchup immunity of stacked-field-oxide structure to the noise transient can be highly increased. By adjusting different numbers or different types of stacked ESD devices in the power-rail ESD clamp circuits, the total holding voltage of the stacked-device structure can be designed higher than the supply voltage. Therefore, the transient-induced latchup issue can be successfully overcome without modifying the high-voltage CMOS process. Latchup-free power-rail ESD clamp circuit can be achieved for the IC applications with VDD of 40V.



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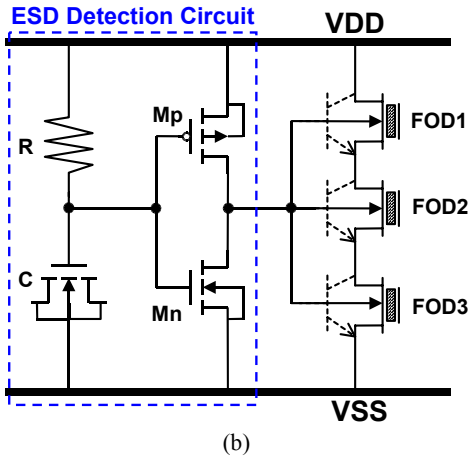

(b)

Figure 14: The proposed power-rail ESD clamp circuits in high-voltage CMOS ICs with (a) two cascaded FOD devices, and (b) three cascaded FOD devices.

IV. Conclusion

Latchup or latchup-like issue of ESD protection devices in high-voltage CMOS ICs has been clearly investigated by TLP stress and TLU test. The low holding voltage of ESD protection devices will cause the high-voltage CMOS ICs susceptible to the latchup or latchup-like danger during normal circuit operating condition. By adjusting different numbers or different types of stacked ESD devices in the power-rail ESD clamp circuits, the total holding voltage of the stacked-device structure can be designed higher than the supply voltage without using extra process modification. For the IC applications with VDD of 40V, a new latchup-free power-rail ESD clamp circuit with stacked-field-oxide structure has been designed and successfully verified in a 0.25-μm 40-V CMOS process to meet the desired ESD level.

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