

1.3

Test Structures to Verify ESD Robustness of On-Glass Devices in LTPS Technology

Ming-Dou Ker, Chih-Kang Deng, Sheng-Chieh Yang*, and Yaw-Ming Tasi*

Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics
National Chiao-Tung University, Hsinchu, Taiwan

*Advanced Technology Research Center, Toppoly Optoelectronics Corporation, Miaoli, Taiwan

Abstract—Different test structures used to investigate the electrostatic discharge (ESD) robustness of on-glass device in Low Temperature Poly-Si (LTPS) process are proposed in this paper. The transmission line pulse generator (TLPG) is used to monitor the I-V behaviors of on-glass devices in the high-current region, and to evaluate the robustness of those LTPS devices during ESD stress condition. Finally, a successful ESD protection design with P^+ -i- N^+ diodes and a VDD-to-VSS ESD clamp circuit integrated on a LCD panel has been demonstrated with a machine-model (MM) ESD level of up to 275 V, whereas the traditional one only can sustain 100 V MM ESD stress.

INTRODUCTION

LTPS TFT devices have been widely used in active matrix liquid crystal display (AMLCD), because the electron mobility of the LTPS TFT device is about 100-times larger than that of the conventional amorphous silicon (α -Si) TFT device [1]. Moreover, LTPS technology is progressing toward system on panel (SOP) applications, which is expected to integrate the AMLCD with all control circuits on a glass substrate in near future.

Since the large glass insulating layer, where thin-film devices are fabricated on, has a low thermal conductivity, the heat generated by large ESD current cannot be dissipated easily. On the other hand, the yield is an important issue of production consideration. When the large glass is delivered or assembled in the factory, this insulator material of glass could accumulate large static charges, which would be discharged to damage the circuit on the glass. For this reason, ESD reliability of LTPS devices will become more serious, when more circuits are integrated onto the panel.

Some studies related to ESD degradation of TFT devices had been reported [2]-[7]. At the device level, the transmission line pulse generator (TLPG) with a pulse width of 100 ns has been widely used to evaluate ESD robustness of the TFT devices [5]. In this work, the test structures of three LTPS diodes and two LTPS TFT devices are designed and fabricated in a LTPS process. The ESD robustness of such LTPS devices with different test structures and geometry layout parameters are characterized by measuring their secondary breakdown current I_{t2} with TLPG system.

TEST STRUCTURES OF ON-GLASS DEVICES

In the LTPS process, a buffer oxide and an α -Si:H film were deposited on glass substrate by PECVD system, and then XeCl excimer laser was used to crystallize this α -Si film. After defining active islands, an ion doping was carried out to form P^+ , N^+ , and P^+ regions. Double gate insulator layer film, SiO_x and SiN_x , were deposited by PECVD, and then the Mo gate-metal was deposited and patterned. Subsequently, the LDD region of TFT device and the N^- region of LTPS diode were formed by N^- ion doping process. Moreover, hydrogenation was used to improve the device performance. All LTPS devices, including diodes and FETs, were finished after contact holes and metal pads formations.

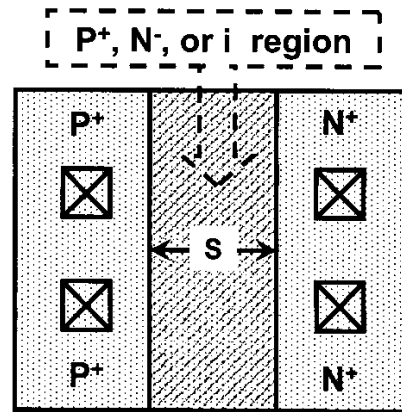


Fig. 1. The layout top-view of three different diodes.

The layout top-view of test structures on three different diodes is shown in Fig. 1. Those diodes are named as the P^+ - P^- - N^+ diode, the P^+ - N^- - N^+ diode, and the P^+ -i- N^+ diode, which are formed by different doping types in the center region. The symbol "i" means intrinsic, which is formed by gate-metal shading. The layout parameter of diodes for ESD consideration is the spacing S , which varies from 2 μm to 10 μm in those test structures. The P^+ and N^+ contacts of LTPS diode have a clearance of 5 μm to the center region. Fig. 2 shows the test structures of TFT devices to verify their ESD robustness. One is the conventional NMOS TFT device with a LDD structure shown in Fig. 2(a), and the other is the source-side body contact (SSBC) TFT device with a P^+ body pickup in the

source shown in Fig. 2(b). All LTPS devices are drawn in finger style, and the total widths of diode and TFT device are 400 μm and 600 μm , respectively. The channel length of such TFT devices in the test structures is varying from 3 μm to 15 μm to verify its impact on ESD robustness.

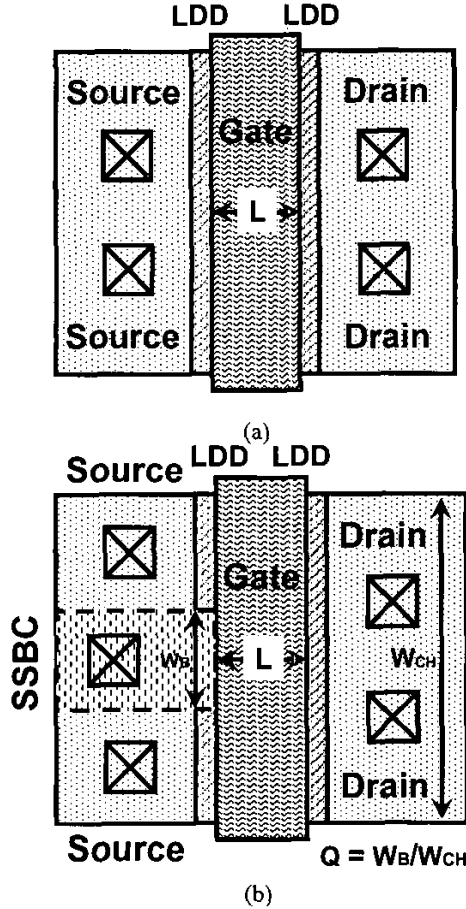


Fig. 2. The layout top-view of (a) conventional NMOS TFT device, and (b) SSBC TFT device.

RESULTS AND DISCUSSION

A. TLP I-V Characteristics of LTPS Diodes

Transmission line pulse (TLP) generator can provide a precise high-voltage and high-current waveforms in a very short period. This high-current pulse simulated the ESD event has been widely used to quality the ESD robustness of protection devices or circuits. In this paper, the TLP generator is also used to investigative the turn-on behaviors of thin-film devices, including LTPS TFTs and LTPS diodes, during high ESD current stress. Those devices are zapped with step-by-step increasing TLP stresses to obtain relative TLP currents through on the devices. Fig. 3 plots the TLP I-V curves of different diodes with a spacing of 5 μm in the center region under forward-biased condition. The diode under forward TLP stress means a positive current with 100

ns pulse width injected from the P^+ node to N^+ node. The It_2 value is defined, when the TLP I-V curve at the beginning of secondary breakdown point with a negative resistance, or the visible damage can be seen on the device from the microscope.

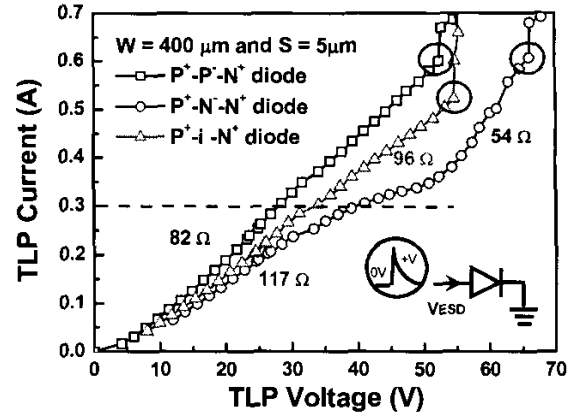


Fig. 3. The TLP I-V curves of three different diodes under forward-biased condition.

In Fig. 3, the $P^+-P^--N^+$ diode has the smallest turn-on resistance and the highest It_2 value among those three kinds of diodes. Compared with the P^+-i-N^+ diode, its It_2 value is smaller than that of the $P^+-P^--N^+$ diode, because the P^+-i-N^+ diode has a higher turn-on resistance during high ESD current stress. Peculiarly, the TLP I-V curve of $P^+-N^--N^+$ diode is skew when the TLP current is larger than 0.3 A, and its turn-on resistance will reduce sharply. This result may attribute to the unsettled process in this work. The N^- doping in our LTPS process is only designed for LDD formation in NMOS TFT device, which is very shallow and light to prevent from the kink effect [8]. In the low current region, that is smaller than 0.3 A, the turn-on resistance of $P^+-N^--N^+$ diode which has no gate-metal in the center region is larger than the others which have gate-metal coupling to enhance turn-on efficiency. In the high current region, that is larger than 0.3 A, the electron current is dominated in the $P^+-N^--N^+$ diode with a 5- μm spacing, whose turn-on resistance is smaller than the other two kinds of diodes.

The dependences of It_2 on the spacing S of three different LTPS diodes under forward TLP stress are shown in Fig. 4, where the width of diodes is kept at 400 μm . When the spacing S is increased from 2 μm to 10 μm , the It_2 value of those diodes is decreased gradually. The It_2 of diode under forward TLP stress increases with the spacing S shrinking, as shown in Fig. 4. When the spacing S is smaller than 5 μm , the $P^+-P^--N^+$ diode and the $P^+-N^--N^+$ diode have higher It_2 than that of the P^+-i-N^+ diode due to the smaller turn-on resistance in the center region.

On the other hand, the It_2 of $P^+-N^--N^+$ diode falls sharply, when the spacing S is larger than 5 μm . It can be attributed to the large power dissipation of $P^+-N^--N^+$ diode with a

long spacing S . Because there is a resistance transition region of the $P^+-N^--N^+$ diode in the TLP $I-V$ curve (from $177\ \Omega$ to $54\ \Omega$), as shown in Fig. 3, a large voltage will drop on the $P^+-N^--N^+$ diode in this transition region. The longer spacing S of $P^+-N^--N^+$ diode will cause more voltage dropping on this device with more power dissipation, which degraded its ESD robustness.

The It_2 of diode under reverse TLP stress is much smaller than that under forward TLP stress. The diode under reverse TLP stress starts to conduct the TLP current by junction breakdown. The breakdown voltage of the diode with a spacing S of $5\ \mu\text{m}$ is about $40\ \text{V}$, and it increases with the spacing S increasing. Large power dissipation will occur on the reverse-biased diode, which has a lower It_2 value. In summary, the diode should be suitably designed to conduct the ESD current under forward-biased condition for achieving a good ESD robustness.

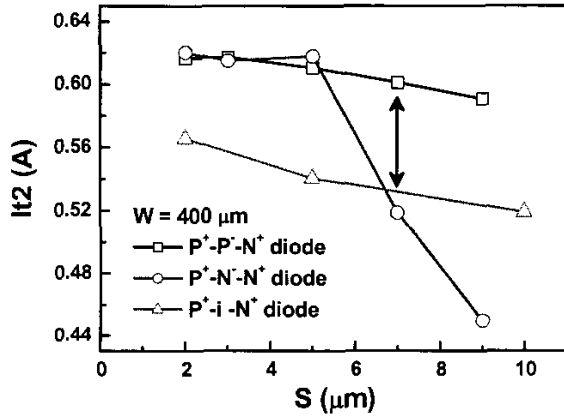


Fig. 4. The relations between It_2 and the spacing S of different diodes under forward TLP stress.

B. TLP $I-V$ Characteristics of LTPS TFTs

The characteristics of TFT devices fabricated on glass are investigated. The TFT device has three terminals, which are drain, source, and gate. If the TFT device is used as an ESD protection device in the input or output pads, it must work on off-state when the panel circuits are under normal circuit operation. Thus, the gate of this ESD protection TFT device should be connected to its source.

When a TLP (ESD) current is injected from drain to source with a gate of TFT device connected to source, the TFT device is under reverse TLP stress. On the contrary, when a TLP (ESD) current is injected from source to drain, the TFT device is under forward TLP stress. The SSBC TFT device has a P^+ body contact in the source side which is inserted a diode in the TFT device, as shown in Fig. 2(b). Because the source is grounded under normal circuit operation, the extra P^+ region in source region does not cause malfunction in the SSBC device.

The relations between It_2 and different channel lengths

in the test structures of SSBC and conventional TFT devices under reverse TLP stress are compared in Fig. 5, where the channel widths are kept at $600\ \mu\text{m}$. The schematic symbol of TFT device under reverse TLP stresses is inserted in Fig. 5. With increase of the channel length, from $3\ \mu\text{m}$ to $15\ \mu\text{m}$, the It_2 values of those devices are decreased. On the other hand, the It_2 values of SSBC TFT devices are higher than those of conventional TFT devices. When a TFT device is subjected to large voltage or current stress, it will generate large electron hole pairs in the channel to cause serious degradation of the TFT device. Nevertheless, the SSBC TFT device with a P^+ body contact in the source side can absorb hot holes generated in channel to alleviate the device degradation. Consequently, when a TFT device is under reverse high ESD current stress, the SSBC TFT device can obtain a higher It_2 value than that of conventional TFT device. The source body contact efficiency decreases with the channel length increasing. For this reason, the It_2 of SSBC TFT device with a long channel length of $15\ \mu\text{m}$ is almost the same as that of conventional TFT device under reverse TLP stress.

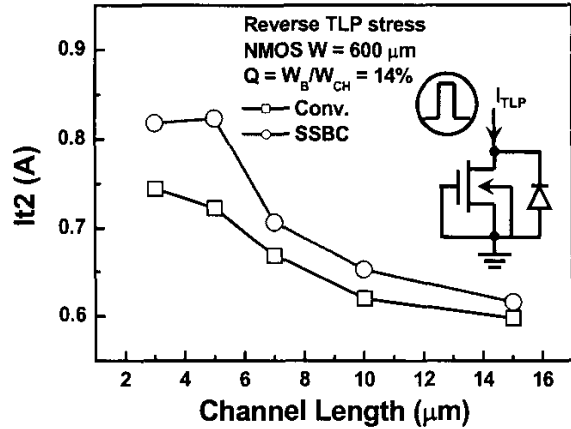


Fig. 5. The dependence of It_2 on channel length of conventional TFT and SSBC TFT under reverse TLP stress.

The It_2 of SSBC TFT device compared with that of conventional TFT device with different channel lengths under forward TLP stress are shown in Fig. 6, where the channel widths are also kept at $600\ \mu\text{m}$. The schematic symbol of TFT device under forward TLP stresses is also inserted in Fig. 6. A short-channel device has a higher It_2 due to its lower turn-on resistance. On the other hand, under forward TLP stress, the channel of TFT device is turned on to discharge TLP current. So, it has a higher It_2 compared with that under reverse TLP stress, as shown in Figs. 5 and 6. Moreover, the It_2 values of SSBC TFT devices are larger than those of conventional TFT devices under forward TLP stress due to the source-side body contact, which creates a parasitic diode path under forward TLP stress. Therefore, the SSBC TFT device with a forward-biased diode path can sustain higher ESD current under forward TLP stress. Furthermore, the device with a shorter channel length has

higher electrical field near the drain and the gate insulator under forward TLP stress. High energy carriers crowding in channel surface will cause a lower I_{t2} , especially in the conventional TFT device with a channel length of 3 μm . Because the forward diode efficiency decreases with the channel length increasing, the I_{t2} of SSBC TFT device with a long channel length of 15 μm is also almost the same as that of conventional TFT device under forward TLP stress.

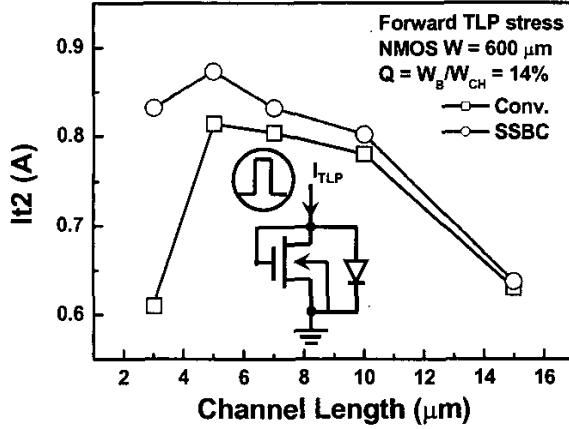


Fig. 6. The dependence of I_{t2} on channel lengths of conventional TFT and SSBC TFT under forward TLP stress.

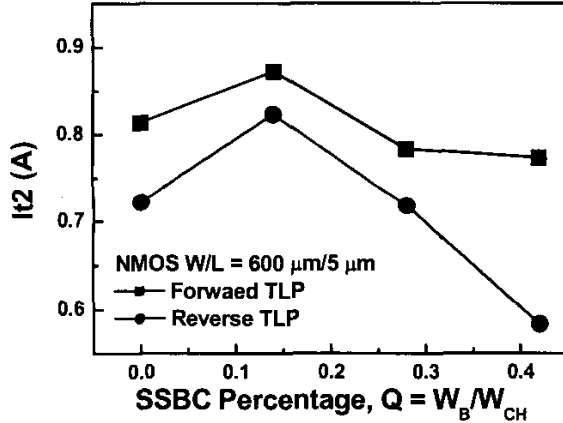


Fig. 7. The dependence of I_{t2} on channel lengths of SSBC percentage in the test structure under forward and reverse TLP stresses.

After understanding the TLP characteristics of SSBC TFT device, the dependences of source body contact are studied. The SSBC percentage is defined as $Q = W_B/W_{CH}$, where the W_B is total source side body width and the W_{CH} is channel width, as shown in Fig. 2(b). In Fig. 7, the SSBC NMOS device with a Q of 14 % in source region gains the best I_{t2} under forward and reverse TLP stresses. When the Q is increased from 14 % to 42 %, the I_{t2} of SSBC device decreased from 0.81 A to 0.56 A under reverse TLP stress, and from 0.87 A to 0.76 A under forward TLP stress. The SSBC device with a higher Q value will approach to a

$P^+-P^-N^+$ diode structure, which has a low I_{t2} value, especially under reverse TLP stress.

C. Whole-Panel ESD Protection Design

A new whole-panel ESD protection design with P^+-i-N^+ diodes and a VDD-to-VSS ESD clamp circuit is shown in Fig. 8. The ESD protection diode is drawn with a dimension (W/L) of 1246 $\mu\text{m}/4 \mu\text{m}$. The VDD-to-VSS ESD clamp circuit contains an ESD detection circuit (RC-inverter) and an ESD clamp device (MESD). When a positive-to-VSS (PS) ESD stress at the input pad, as shown in Fig. 8, the main ESD current flows through the P^+-i-N^+ diode to VDD power line by forward diode, and then the ESD current discharges through VDD-to-VSS ESD clamp to the ground. The ESD voltage pulse has a rise time about 10 ns. The voltage level of V_X increases much slower than the voltage level on the VDD power line Positive-to-VSS ESD stress, because the RC circuit has a time constant in the order of microseconds (μs). Due to the delay of the voltage increase on the node V_X , the Mp device is turned on by ESD energy and it raises the voltage of the node V_G to turn on MESD. Thus, the ESD detection circuit can turn on MESD to discharge ESD current during the positive-to-VSS ESD stress, but to keep MESD off in normal circuit operation condition [7].

The panel should be tested under at least four modes of ESD zapping conditions on each pin, including positive-to-VSS (PS), negative-to-VDD (ND), positive-to-VDD (PD), and negative-to-VSS (NS) ESD zapping modes. Because the diode under reverse ESD stress has the weakest I_{t2} value, this new ESD protection design can discharge the ESD current through a forward diode path to achieve a higher ESD robustness among the four ESD-zapping modes.

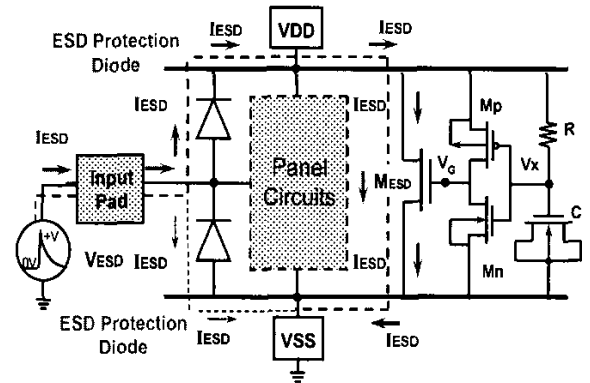


Fig. 8. A new successful ESD protection design on a LCD panel with P^+-i-N^+ diodes and a VDD-to-VSS ESD clamp circuit.

On the contrary, the conventional ESD protection design, which has a gate-VDD LTPS PMOS (GDPMOS) and a gate-ground LTPS NMOS (GGNMOS) as ESD protection devices, but no VDD-to-VSS clamp circuit is shown in Fig. 9. The dimensions of GGNMOS and GDPMOS are drawn

as $800\ \mu\text{m}/6\ \mu\text{m}$ and $1200\ \mu\text{m}/6\ \mu\text{m}$, respectively. When the input pin of this panel is under positive ESD zapping related to VSS (PS mode), the ESD current discharges by only one path, as shown by dashed line in Fig. 9. The ESD energy will be released from input pin to VSS as soon as the drain junction breakdown of GGNMOS. By the breakdown mechanism to discharge ESD energy, both ESD robustness and turn-on speed of device are poor. The worse ESD robustness can be expected in the conventional ESD protection design.

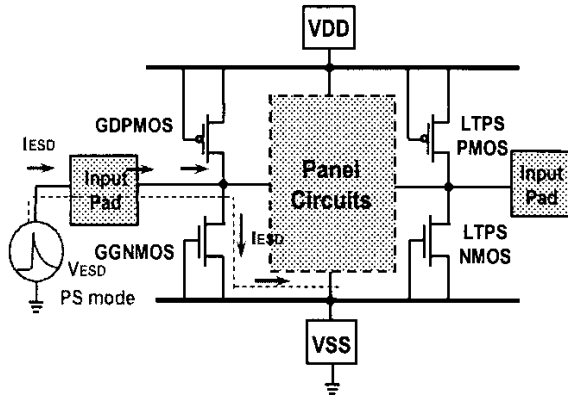


Fig. 9. The conventional ESD protection design for LCD panel with a GGNMOS and a GDPMOS at the I/O pad.

TABLE I
COMPARISON ON THE MACHINE-MODEL (MM) ESD ROBUSTNESS
BETWEEN THE CONVENTIONAL AND THE NEW PROPOSED
ESD PROTECTION DESIGN ON LCD PANELS

ESD Protection Design	MM ESD Zapping Level			
	Positive-to-VCC	Negative-to-VCC	Positive-to-VSS	Negative-to-VSS
Conventional Design (Fig. 9)	425V	325V	225V	100V
New Design (Fig. 8)	350V	375V	350V	275V

(Failure criterion: visible damage on protection circuit)

The ESD robustness of those two designs under Machine Model (MM) ESD stresses are compared in Table I. ESD robustness of the LCD panel with the new proposed design can be improved during the negative-to-VDD (ND), positive-to-VSS (PS), and negative-to-VSS (NS) ESD zapping conditions. Especially under the NS-mode, ESD robustness of new protection design has been greatly improved 175 % (from 100 V to 275 V). The ESD characteristics of P^+-i-N^+ diodes with a VDD-to-VSS clamp circuit are more reliable and robust than that of GDPMOS and GGNMOS. So, the whole panel ESD level of this new design can be up to 275 V in MM ESD stress. From the results of test structures, if the P^+-i-N^+ diodes and the ESD clamp device (MESD) were replaced by the $P^+-P^--N^+$ diode and the SSBC device, respectively, the ESD robustness of whole-panel can be further increased.

CONCLUSION

ESD robustness among different test structures of on-glass devices in LTPS process on panel has been investigated. The $P^+-P^--N^+$ diode under forward TLP stress has the highest ESD robustness. The TFT device under forward TLP stress is more robust than that under reverse TLP stress. Besides, the I_t2 of SSBC TFT device with a Q factor of 14 % is higher than that of conventional TFT device, no matter under forward or reverse TLP stresses. Finally, a whole-panel ESD protection design with P^+-i-N^+ diodes and VDD-to-VSS ESD clamp circuits has been successfully verified to have a good enough ESD robustness for system-on-panel applications.

REFERENCES

- [1] K. Yoneda, R. Yokoyama, and T. Yamada, "Development trends of LTPS TFT LCDs for mobile application," in *Proc. Symp. VLSI Circuits Dig.*, 2001, pp.14-16.
- [2] F. R. Libsch and H. Abe, "ESD: how much protection is need for AMLCDs," in *Dig. Tech. Papers, SID*, 1994, pp. 255-258.
- [3] S. Uchikoga *et al.*, "Deterioration mechanism of α -Si:H TFT caused by ESD," in *Proc. AM-LCD*, 1994, pp.128-131.
- [4] T. Yanagisawa, "Electrostatic damage and protection for TFT-LCD's," in *Dig. Tech. Papers, SID*, 1993, pp. 735-738.
- [5] N. T. Golo, F. G. Kuper, and T. J. Mouthaan, "Analysis of the electrical breakdown in hydrogenated amorphous silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 49, pp.1012-1018, Jun. 2000.
- [6] S.-C. Lee, B.-C. Jeon, K.-C. Moon, M.-C. Lee, and M.-K. Han, "Electrostatic discharge effects on polysilicon TFTs for AMLCD," in *Dig. Tech. Papers, SID*, 2002, pp. 212-215.
- [7] M.-D. Ker, T.-K. Tseng, S.-C. Yang, A. Shih, and Y.-M. Tasi, "Successful electrostatic discharge protection design for LTPS circuits integrated on panel," in *Dig. Tech. Papers, SID*, 2003, pp. 212-215.
- [8] J.-S. Yoo, C.-H. Kim, M.-C. Lee, M.-K. Han, and H.-J. Kim, "Reliability of low temperature poly-Si TFT employing counter-doped lateral body terminal," in *IEDM Tech. Dig.*, 2000, pp.217-220.