1.2

Characterization on ESD Devices with Test Structures in Silicon Germanium RF BiCMOS Process

Ming-Dou Ker, Woei-Lin Wu, and Chyh-Yih Chang*

Nanoelectronics & Gigascale Systems Laboratory, Institute of Electronics
National Chiao-Tung University, Hsinchu, Taiwan. E-mail: mdker@ieee.org
* Product and ESD Engineering Department, SoC Technology Center
Industrial Technology Research Institute, Hsinchu, Taiwan. E-mail: alexchang@itri.org.tw

ABSTRACT

Different electrostatic discharge (ESD) devices in a 0.35-μm silicon germanium (SiGe) RF BiCMOS process are characterized in detail by transmission line pulse (TLP) generator and ESD simulator for on-chip ESD protection design. The test structures of diodes with different p-n junctions and the silicon-germanium heterojunction bipolar transistors (HBTs) with different layout parameters have been drawn for investigating their ESD robustness. The human-body-model (HBM) ESD robustness of SiGe HBTs with the optional low-voltage (LV), high-voltage (HV), and high-speed (HS) implantations has been measured and compared in the experimental test chips.

INTRODUCTION

Silicon-germanium heterojunction bipolar transistor (HBT) has become a key technology for RF applications in giga-bit communication or wireless systems. ESD protection in SiGe technology plays an important role on the reliability of telecommunication systems [1]-[5]. In a SiGe RF BiCMOS process, with the consideration of Giga-HZ input signals, the SiGe heterojunction bipolar transistor is also used as the on-chip ESD protection device to protect itself. Therefore, the relation between ESD robustness and layout parameters of SiGe HBT should be characterized to achieve a good enough ESD protection design in such high-speed communication integrated circuits. Some successful ESD protection designs for RF IC applications had been reported by using the double diodes with the turn-on-efficient power-rail ESD clamp circuit [6], [7]. The relation between ESD robustness and layout parameters of diodes with different junctions in a given SiGe BiCMOS process should be characterized for ESD protection design. With the detailed experimental results, the on-chip ESD protection design for Giga-Hz RF circuits can be optimized with both considerations on RF performance and ESD robustness.

In this work, the test structures of SiGe HBT devices and diodes with different junctions or layout parameters have been fabricated in a 0.35-μm SiGe BiCMOS process to investigate their ESD robustness. The transmission line pulse (TLP) system and ESD simulator are used to investigate the robustness of SiGe devices under both the forward- and reverse-biased conditions.

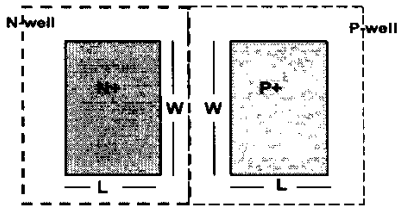
TEST STRUCTURES FOR DIODES AND HBTS

A. Diodes

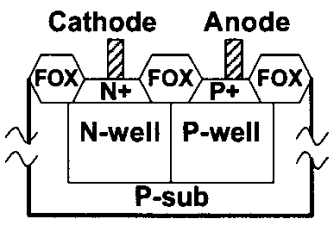
Five kinds of diodes including P-well/N-well diode, varactor diode (for voltage controlled capacitor), and vertical base-collector (VBC) diode with different implantation types such as local-collector, high-speed, or without implantation are investigated.

Fig. 1 shows the top view and cross-sectional view of the P-well/N-well diode, which is used as a reference for comparing with the other diodes of different structures. Fig. 2 shows the top view and cross-sectional view of varactor (VR) diode, where the attention will focus to the junction between P+ and N- (NEPI). Fig. 3 shows the top view and cross-sectional view of VBC diode with LC (local collector) implantation. The diode junction is formed between base poly (BP) and local collector region with NEPI. The LC (local collector) implantation under the base poly region is further changed as high-speed implantation, or even no implantation in these diode structures to compare their ESD robustness.

Among the test structures for investigation, the width (W) of diode junction is drawn in the range from 3 to 12 μm, and the length (L) of diode junction is drawn from 20 to 80 μm in this work. The width and length of the diode layout are also indicated in Fig. 1 ~ Fig. 3.



(a)



(b)

Fig. 1. (a) Top view, and (b) cross-sectional view, of p-well/n-well diode in a SiGe BiCMOS process.

0-7803-8262-5/04/$17.00©2004 IEEE 04CH37516

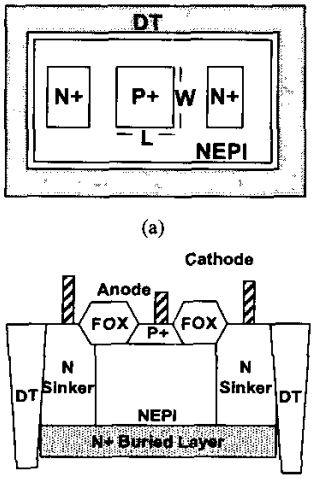


Fig. 2 (a) Top view, and (b) cross-sectional view, of varactor (VR) diode in a SiGe BiCMOS process.

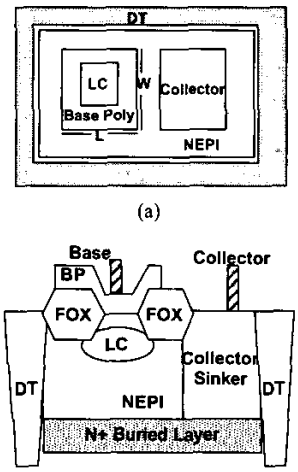


Fig. 3. (a) Top view, and (b) cross-sectional view, of vertical base-collector (VBC) diode in a SiGe BiCMOS process.

B. HBT Devices

Three kinds of SiGe HBT devices are studied in this work, which are the low-voltage (LV) SiGe NPN HBT (BV_{CEO} = 3.8 V, f_T = 47 GHz at V_{BC} = 1 V), the high-voltage (HV) SiGe NPN HBT (BV_{CEO} = 6 V, f_T = 30 GHz at V_{bc} = 1 V), and the high-speed (HS) SiGe NPN HBT (BV_{CEO} = 2.5 V, f_T = 70 GHz at V_{BC} = 1 V). To investigate ESD robustness of these SiGe HBTs, the experimental test chips had been fabricated in a 0.35-μm 3.3V/5V RF BiCMOS process. The dependences of emitter length, emitter width, and base resistance on the ESD robustness are investigated for all SiGe HBTs with LV, HV, or HS implantations. Moreover, the layout pattern of high-speed implantation is also drawn with different style to investigate its impact on ESD robustness.

Fig. 4 shows the cross-sectional view of a low-voltage SiGe NPN HBT. An N-type local collector (LC) implantation region is formed under the emitter poly and connecting to the N-type sinker through the bottom N+ buried layer. The N-type sinker is formed as the collector terminal. In the high-voltage SiGe NPN HBT for 5-V operation, the LC implantation is not performed to increase the breakdown voltage of base/collector junction. On the other hand, the LC implantation is replaced by a high-speed (HS) implantation with high concentration collector region to speed up the operating speed of the HBT device.

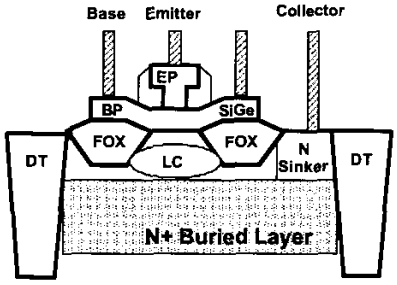


Fig. 4. The device cross-sectional view of low-voltage SiGe NPN HBT with local collector (LC) implantation.

EXPERIMENTAL RESULTS

A. Diodes

Fig. 5 shows the breakdown voltages, defined at the current of 1 μA under reverse-biased condition, of different diodes. From the experimental results, the junction between P-well and N-well has the highest breakdown voltage. In the varactor (VR) diode with a junction between P+ and NEPI (N–), this VR diode can work with good characteristics under forward and reverse biased conditions. In the VBC diode with a junction between base poly and the local collector, it also has good characteristics under forward and reverse biased conditions. All diodes under the normal power bias (Vdd = 3.3 V) has a leakage current less than 1 nA.

To observe the high current characteristics of ESD devices in SiGe BiCMOS process, transmission line pulsing (TLP) system with a pulse width of 100 ns is used to measure the second breakdown current, I_{t2}. [8], [9]. Three diodes, the P-well/N-well diode, VR diode, and VBC+LC diode, are zapped by the TLP to find their I_{t2}. Besides TLP test, the ESD simulator is also used to

measure ESD level of devices. The ESD stress is performed with a commercial KeyTek ZapMaster ESD simulator. The start voltage of human-body-model (HBM) ESD stress is 50 V. Each device under test is performed on 2 samples, at least.

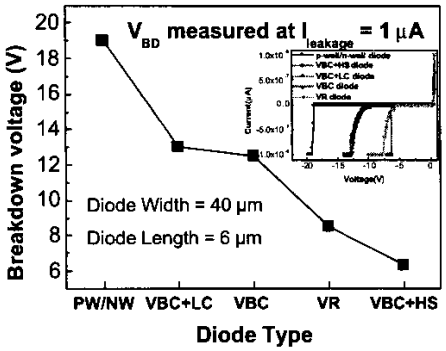
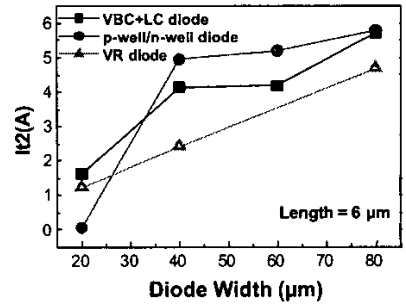
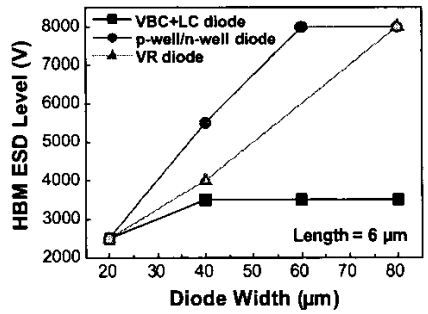


Fig. 5. The breakdown voltage of different diodes when its leakage current equals to 1 μA.



(a)



(b)

Fig. 6. Comparisons of (a) second breakdown current, and (b) HBM ESD robustness, among the P-well/N-well diode, the VR diode, and the VBC+LC diode with different layout widths under forward-biased condition.

The second breakdown current (It2) and HBM ESD robustness of the P-well/N-well diode, VR diode, and VBC+LC diode with different widths under forward-biased condition are shown in Fig. 6(a) and 6(b), respectively. The It2 and ESD robustness on the diode is increased when the diode width is increased, but that of the VBC+LC diode is not significantly improved when the diode width is further increased. Under forward-biased condition, the P-well/N-well diode has the highest It2 and ESD level, which is a reference for designing ESD protection circuit.

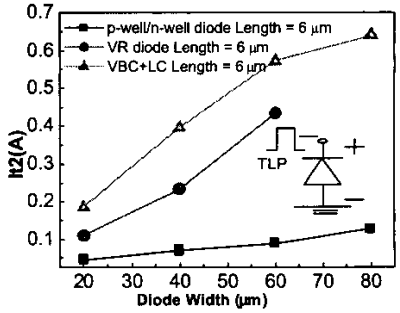


Fig. 7. Comparison of second breakdown current among the P-well/N-well diode, VR diode, and VBC+LC diode with different layout widths under reverse-biased condition.

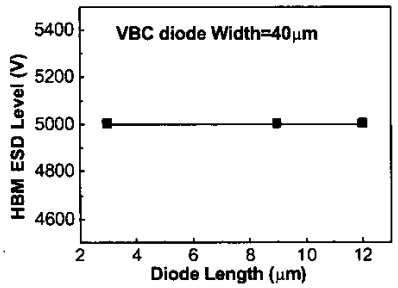


Fig. 8. HBM ESD robustness on the diode length of the VBC diode with a fixed width of 40 μm under the forward-biased condition.

Fig. 7 shows the second breakdown current (It2) of the P-well/N-well diode, VR diode, and VBC+LC diode with different layout widths under reverse-biased condition. In Fig. 7, the P-well/N-well diode, with a fixed length of 6 μm but different widths, has a very low second breakdown current. Although it has good ESD characteristics under forward-biased condition, it should be avoided in ESD protection circuit to operate such P-well/N-well diode to discharge ESD current in the reverse-biased condition. For the VR diode and VBC+LC diode with a fixed length of 6 μm but different widths, their second breakdown currents are almost proportion to their widths. Fig. 8 shows the dependence of HBM ESD robustness on the diode length of the VBC diode with a fixed width of 40 μm under the forward-biased condition. In Fig. 8, the ESD robustness of the

VBC diode is independent to the diode length. So, the VBC diode can be drawn with the minimum length for saving layout area to get the same ESD level.

B. NMOS in BiCMOS Process

NMOS device is usually used as the ESD clamp device in CMOS ICs, especially between the power rails with RC-based ESD-detection circuit [10]. The dependence of channel width on the HBM ESD robustness of gate-grounded NMOS in such a SiGe BiCMOS process is also investigated and shown in Fig. 9.

The gate-grounded NMOS device with a 200-μm channel width can sustain HBM ESD stress of 2kV to achieve an ESD robustness per channel width of 10V/μm. However, the gate-grounded NMOS with larger channel width shows saturation in ESD robustness, due to the non-uniform turn-on issue along the multiple fingers of NMOS layout. The additional gate-driven [11] or substrate-triggered [12] circuit techniques must be used to improve ESD level of the NMOS with larger device dimension.

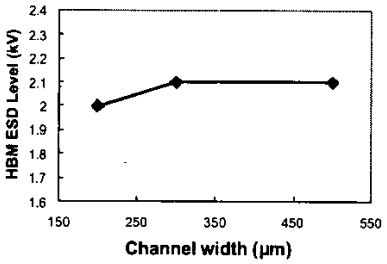


Fig. 9. HBM ESD robustness of gate-grounded NMOS devices in the RF BiCMOS process.

C. HBT with Different Emitter Lengths

Fig. 10 shows ESD robustness of the low-voltage SiGe HBTs with a fixed emitter width of 0.45μm but different emitter lengths. All the low-voltage SiGe HBT devices only pass 50-V HBM ESD stress when emitter width equals to 0.45μm. The similar results are also seen in the high-voltage SiGe HBTs with different emitter lengths, as that shown in Fig. 11. This may result from the too small emitter width and higher junction breakdown voltage. However, the high-speed SiGe HBTs with the lowest junction breakdown voltage have an increasing ESD robustness with the increase of emitter length, as that shown in Fig. 12, where the emitter width also equals to 0.45μm.

D. HBT with Different Emitter Widths

Fig. 13 to Fig. 15 show the ESD result versus the emitter width for the low-voltage, high-voltage, and high-speed SiGe HBTs under a fixed emitter length. In Fig. 13, the low-voltage SiGe HBT sustains higher ESD level when its emitter width is drawn larger than 0.45μm, and achieves 800-V ESD robustness when its emitter width equals to 1.5μm with emitter length of 20.3μm. This equals about 20V/μm, which is double of the ESD level of the gate-grounded NMOS in the same BiCMOS process. In Fig. 14, the high-voltage SiGe HBT shows a relatively low ESD level. Only 200-V ESD level can be sustained, when its emitter width equals to 1.5μm with emitter length of 20.3μm. Similarly, the ESD level increases, when the emitter width of high-speed SiGe HBT increases, as shown in Fig. 15. If the emitter width of SiGe HBT is fixed at 0.45μm, the order of ESD robustness is: LV SiGe HBT = HV SiGe HBT < HS SiGe HBT.

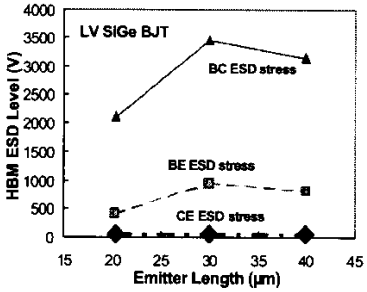


Fig. 10. HBM ESD robustness versus emitter length of the low-voltage SiGe HBT with emitter width of 0.45μm.

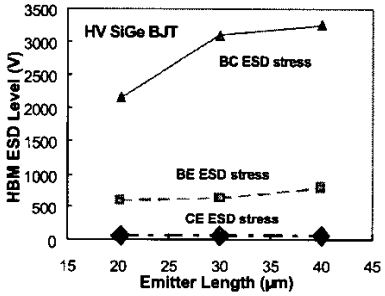


Fig. 11. HBM ESD robustness versus emitter length of the high-voltage SiGe HBT with emitter width of 0.45μm.

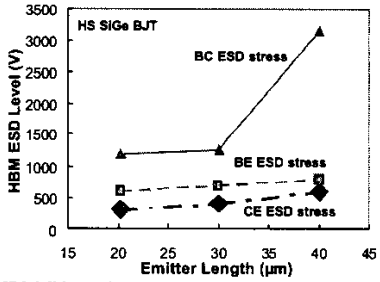


Fig. 12. HBM ESD robustness versus emitter length of the high-speed SiGe HBT with emitter width of 0.45μm.

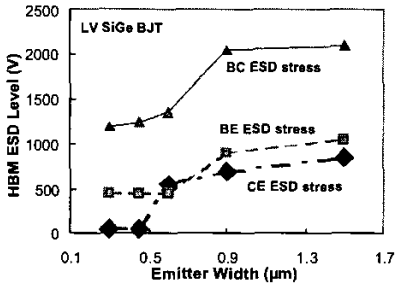


Fig. 13. HBM ESD robustness versus emitter width of the low-voltage SiGe HBT with emitter length of 20.3μm.

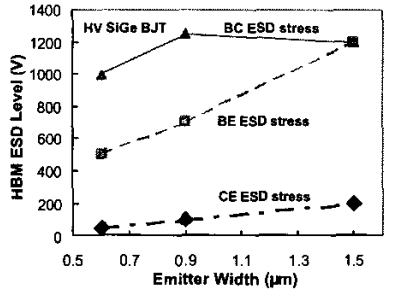


Fig. 14. HBM ESD robustness versus emitter width of the high-voltage SiGe HBT with emitter length of 20.3μm.

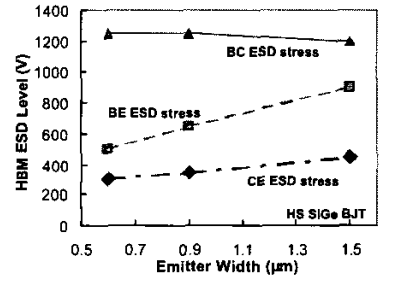


Fig. 15. HBM ESD robustness versus emitter width of the high-speed SiGe HBT with emitter length of 20.3μm.

However, when the emitter width of SiGe HBT is fixed at 1.5μm, the order of ESD robustness is: LV SiGe HBT > HS SiGe HBT > HV SiGe HBT. This is a very interesting phenomenon, and more analysis and experimental measurement will be performed in our future work to get a more clear insight.

E. HBT with Different Base Resistances

Fig. 16 shows the cross-sectional view of a multi-finger SiGe HBT with 4 emitter fingers. The emitter window is 20.3 μm × 0.9 μm. The base resistance can be minimum, when all base terminals (B1, B2, B3, B4, and B5) are connected together through the contact layer on its top. Table I shows the ESD robustness of the low-voltage SiGe HBT when all emitter nodes are grounded, where the ESD stresses are applied to the collector node with some base nodes are grounded, such as only node 1 grounded, others floating, or the node 1, 3 and 5 grounded, others floating. When all base terminals (B1, B2, B3, B4, and B) are connected together to ground, only 100-V HBM ESD stress is passed. The same result also appears when the base terminals B1, B3, B5 are connected to ground.

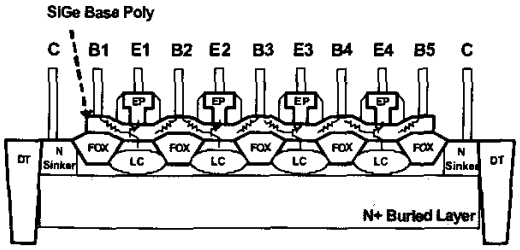


Fig. 16. The SiGe HBT with multi-finger device structure. Base resistance will increase if the base terminal is not all connected together through the contact on its top.

TABLE I

ESD ROBUSTNESS OF LOW-VOLTAGE SiGe HBT WITH DIFFERENT BASE NODES GROUNDED

Grounded Nodes	B12345	B135	B13	B1
HBM ESD	100	100	1800	N/A

TABLE II

ESD ROBUSTNESS OF LOW-VOLTAGE SiGe HBT WITH SOME EMITTER AND BASE NODE GOUNDED

Grounded Nodes	B1E1	B1E2	B1E3
HBM ESD	N/A	700	100

However, when only B1 and B3 are connected to ground, the ESD robustness increases to 1800-V. The floating on the base finger B5 significantly increases the ESD robustness of SiGe HBT. Table II shows the case of only one emitter and one base terminals connecting to ground. :The SiGe HBT with B1E2 grounded can sustain 700-V ESD stress. But, only 100-V ESD stress can be passed when B1E3 grounded. The above measured results show an interesting phenomenon, and more analysis and experimental measurement will be performed in our future work to get a clear explanation.

F. HBT with Different Implantation Patterns

Fig. 17 shows the designed patterns in the high-speed SiGe HBT devices with different high-speed implantation regions. K1 is the standard layout of the high-speed SiGe HBT with unit-square shape. K2, K3, K4, and K5 are designed in different shapes for

investigation. The emitter window equals to 20.3μm × 1.5μm. The ESD robustness degrades with the different designed patterns, as shown in Fig. 18. The standard layout has ESD robustness about 22 V/μm, but the other patterns (K2, K3, K4, and K5) degrade to about only 50%. Failure analysis with SEM pictures after ESD stress will be preformed to find failure location among the SiGe HBT devices with different layout patterns on high-speed implantation.

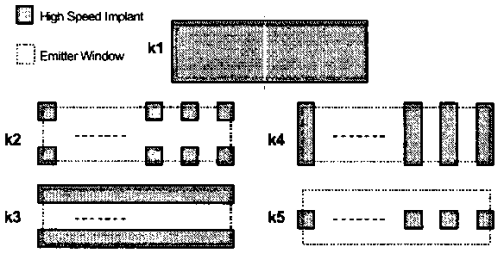


Fig. 17. The designed high-speed implantation patterns for HBT device. K1 is the standard layout with uni-square shape. K2, K3, K4, and K5 are designed to different shapes for investigation.

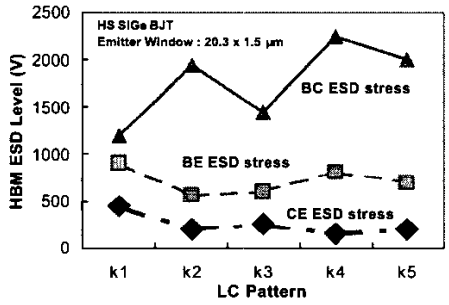


Fig. 18. HBM ESD robustness versus high-speed SiGe HBT with different high-speed implantation patterns.

CONCLUSION

The characteristics of diodes with different structures in the SiGe BiCMOS process have been investigated for using in ESD protection design. The diodes can work with good ESD robustness under forward-biased condition. The ESD robustness of SiGe hetrojunction bipolar transistor in the SiGe BiCMOS process has been also characterized. If the emitter width of SiGe HBT is fixed at 0.45μm, the order of ESD robustness is: LV SiGe HBT = HV SiGe HBT < HS SiGe HBT. However, when the emitter width of SiGe HBT is fixed at 1.5μm, the order of ESD robustness is: LV SiGe HBT > HS SiGe HBT > HV SiGe HBT. With the proper layout parameters, SiGe HBT can perform double ESD robustness than that of NMOS device in the same SiGe BiCMOS process.

REFERENCES

[1] S. Voldman *et al.*, "Electrostatic discharge characterization of epitaxial base silicon germanium heterojunction bipolar transistors," in *Proc. of EOS/ESD Symp.*, 2000, pp. 239-251.

[2] S. Voldman *et al.*, "Silicon germanium heterojunction bipolar transistor ESD power clamps and the Johnson limit," in *Proc. of EOS/ESD Symp.*, 2001, pp. 326-336.

[3] S. Voldman, "Variable-trigger voltage ESD power clamps for mixed voltage applications using a 120 GHz/100 GHz (f_t/f_{MAX}) silicon germanium heterojunction bipolar transistor with carbon incorporation," in *Proc. of EOS/ESD Symp.*, 2002, pp. 52-61.

[4] V. Vashchenko and P. hopper, "Simulation of Si-Ge BiCMOS ESD structures operation including spatial current instability mode," in *Proc. of IEEE Int. Conf. on Microelectronics*, vol. 2, 2002, pp. 745-748.

[5] V. D. Heyn, N. M Iyer, G. Groeseneken, K. Reynders, and P. Moens, "Effect of the n+ sinker in self-triggereing bipolar ESD protection structures," in *Proc. of EOS/ESD Symp.*, 2002, pp. 274-280.

[6] M.-D. Ker, W.-Y. Lo, C.-M. Lee, C.-P. Chen, and H.-S. Kao, "ESD protection design for 900-MHz RF receiver with 8-kV HBM ESD robustness," in *Digest of IEEE RFIC Symp.*, 2002, pp. 427-430.

[7] M.-D. Ker and C.-M. Lee, "Interference of ESD protection diodes on RF performance in giga-Hz RF circuits," in *Proc. of IEEE Int. Symp. on Circuits and Systems*, vol. 1, 2003, pp. 297-300.

[8] T. J. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," in *Proc. EOS/ESD Symp.*, 1985, pp. 49-54.

[9] J. Barth, J. Richner, K. Verhaege, and L. G. Henry, "TLP calibration, correlation, standards, and new techniques," in *Proc. EOS/ESD Symp.* , 2000, pp. 85-96.

[10] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuit for submicron CMOS VLSI," *IEEE Trans. on Electron Devices*, vol. 46, pp. 173-183, 1999.

[11] M.-D. Ker, C.-Y. Wu, T. Cheng, and H.-H. Chang, "Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC," *IEEE Trans. on VLSI Systems*, vol. 4, no. 3, pp. 307-321, 1996.

[12] M.-D. Ker, T.-Y. Chen, and C.-Y. Wu, "ESD protection design in a 0.18-μm salicide CMOS technology by using substrate-triggered technique," in *Proc. of IEEE Int. Symp. on Circuits and Systems*, vol. 4, 2001, pp. 754-757.